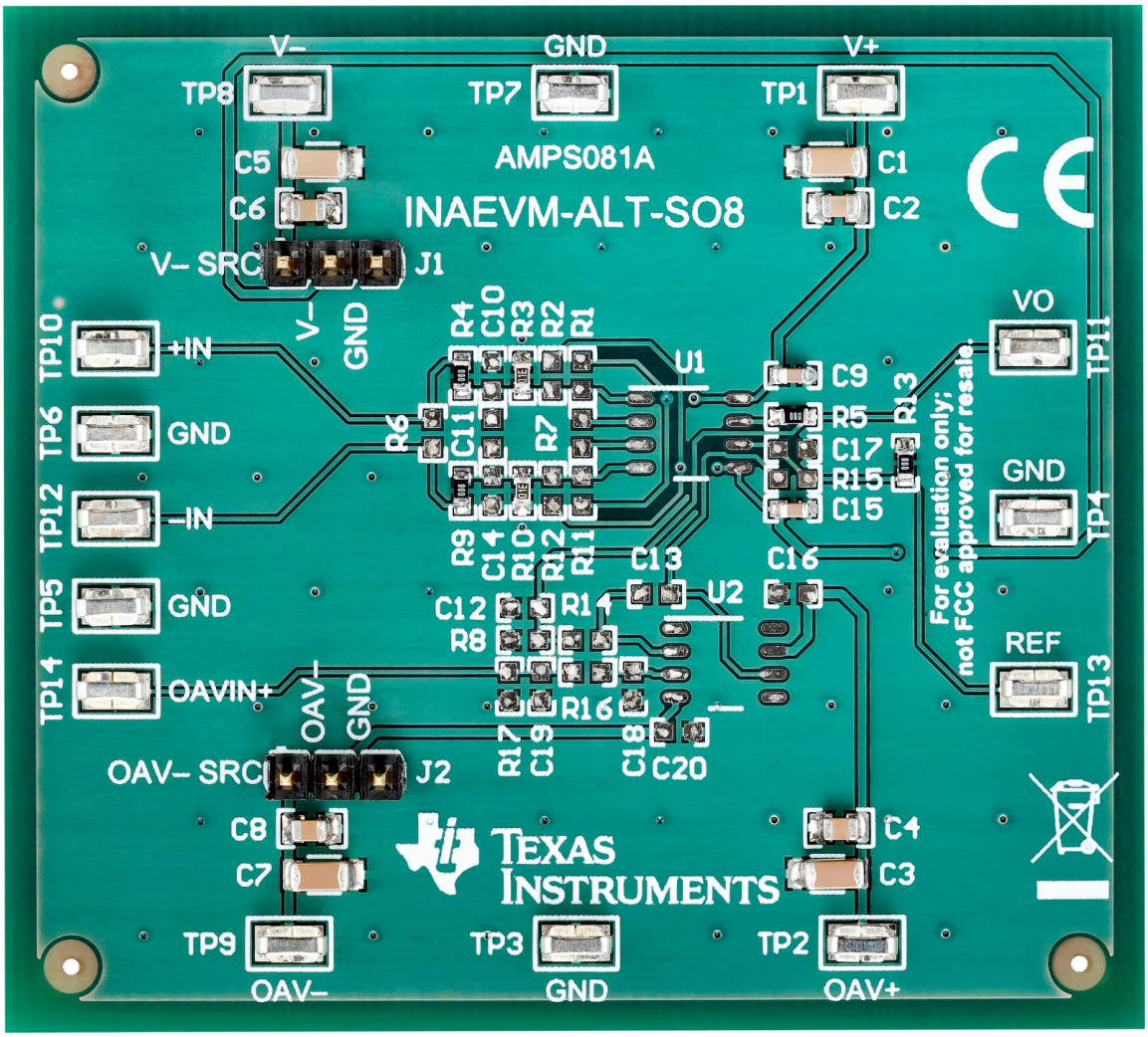
Universal Instrumentation Amplifier Evaluation Module: Alternate Pinout



This user's guide describes the characteristics, operation, and use of the INAEVM-ALT-SO8, a universal evaluation module (EVM) that is compatible with a variety of instrumentation amplifiers (INAs), specifically those with the resistor gain pins at pins 2 and 3. This EVM is compatible with the SOIC-8 (D) package, and is designed to evaluate the performance of the devices in both single-supply and dual-supply configurations. This document includes the schematic, printed circuit board (PCB) layout, and BOM. Throughout this document the terms evaluation board, evaluation module, and EVM are synonymous with the universal INAEVM-ALT-SO8.

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1 Overview

1.1 Features

This EVM is intended to provide basic functional evaluation of the instrumentation amplifiers with the pinout shown in Figure 1. The EVM provide the following features:

- Intuitive evaluation with the silkscreen schematic
- Easy access to nodes with surface-mount test points
- Reference voltage source flexibility
- Convenient input and output filtering

1.2 INA Pinout

The INAEVM-ALT-SO8 is evaluates INAs that have the pinout shown in Figure 1, specifically those with the gain resistor pins at positions 2 and 3.

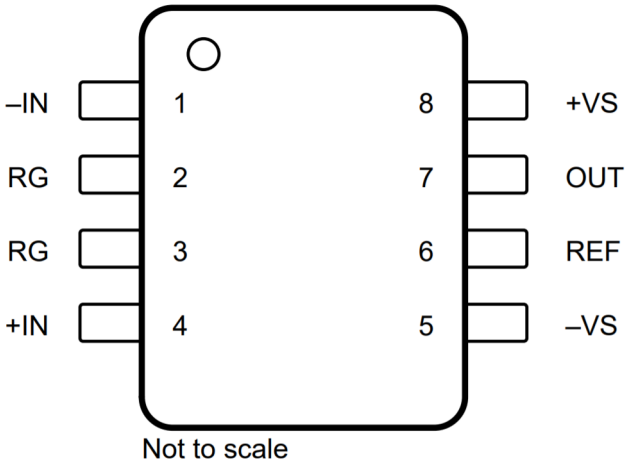

Figure 1. Universal INAEVM-ALT-SO8 Pinout

2 Quick Start

2.1 Dual-Supply Configuration

Figure 2 shows an example of how to set up the EVM for dual-supply operation.

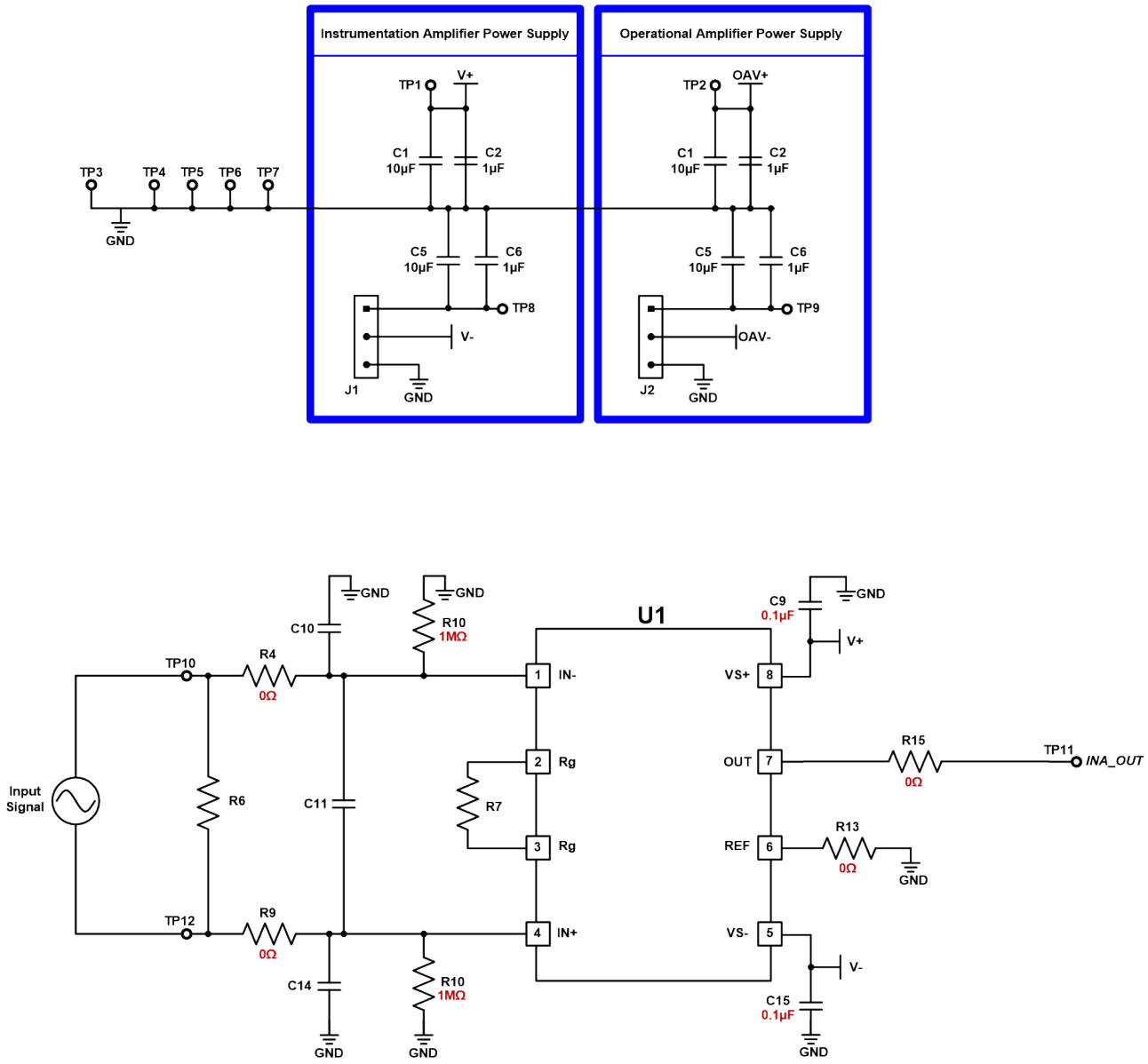

Figure 2. Dual-Supply Configuration

1. +VS to test point TP1
2. –VS to test point TP8
3. Install jumper shunt to position 1 and 2 on J1
4. Differential input signal connect to test points TP10 and TP12
5. Observe output at test point TP11

NOTE: C9 and C15 are prepopulated with 0.1-µF power-supply decoupling capacitors. See the respective device data sheet for additional power-supply decoupling information.

2.2 Single-Supply Configuration

2.2.1 Direct Reference Connection

Figure 3 shows an example of how to set up the EVM for single-supply operation with a direct voltage connection to the reference pin.

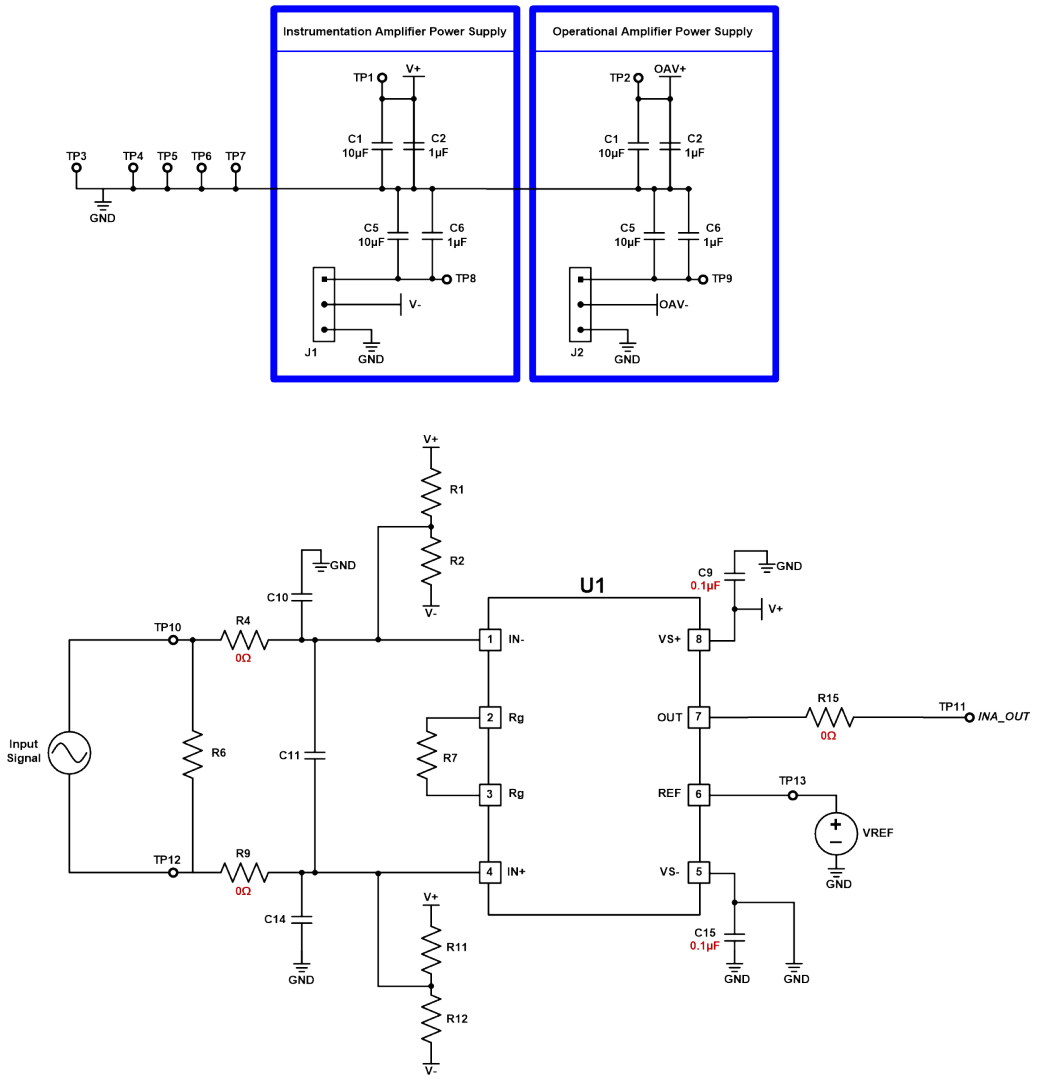

Figure 3. Single-Supply Configuration, Direct Reference Connection

1. +VS to test point TP1
2. GND to test point TP8
3. Install jumper shunt to positions 2 and 3 on J1
4. Remove resistor R13
5. Reference voltage to test point TP13
6. Differential input signal to test points TP10 and TP12
7. Observe output at test point TP11

NOTE: C9 and C15 are prepopulated with 0.1-µF power-supply decoupling capacitors. It is not required to remove C15 for proper single-supply operation. See the respective device data sheet for additional power-supply decoupling information.

2.2.2 Buffered-Reference Voltage Connection

A buffered-reference configuration is useful when the source impedance is high (for example, a voltage divider). Buffering a high-impedance source with an operational amplifier provides a low-impedance source and preserves common-mode rejection. Figure 4 shows an example of how to set up the EVM for single-supply operation with a buffered-reference voltage connection.

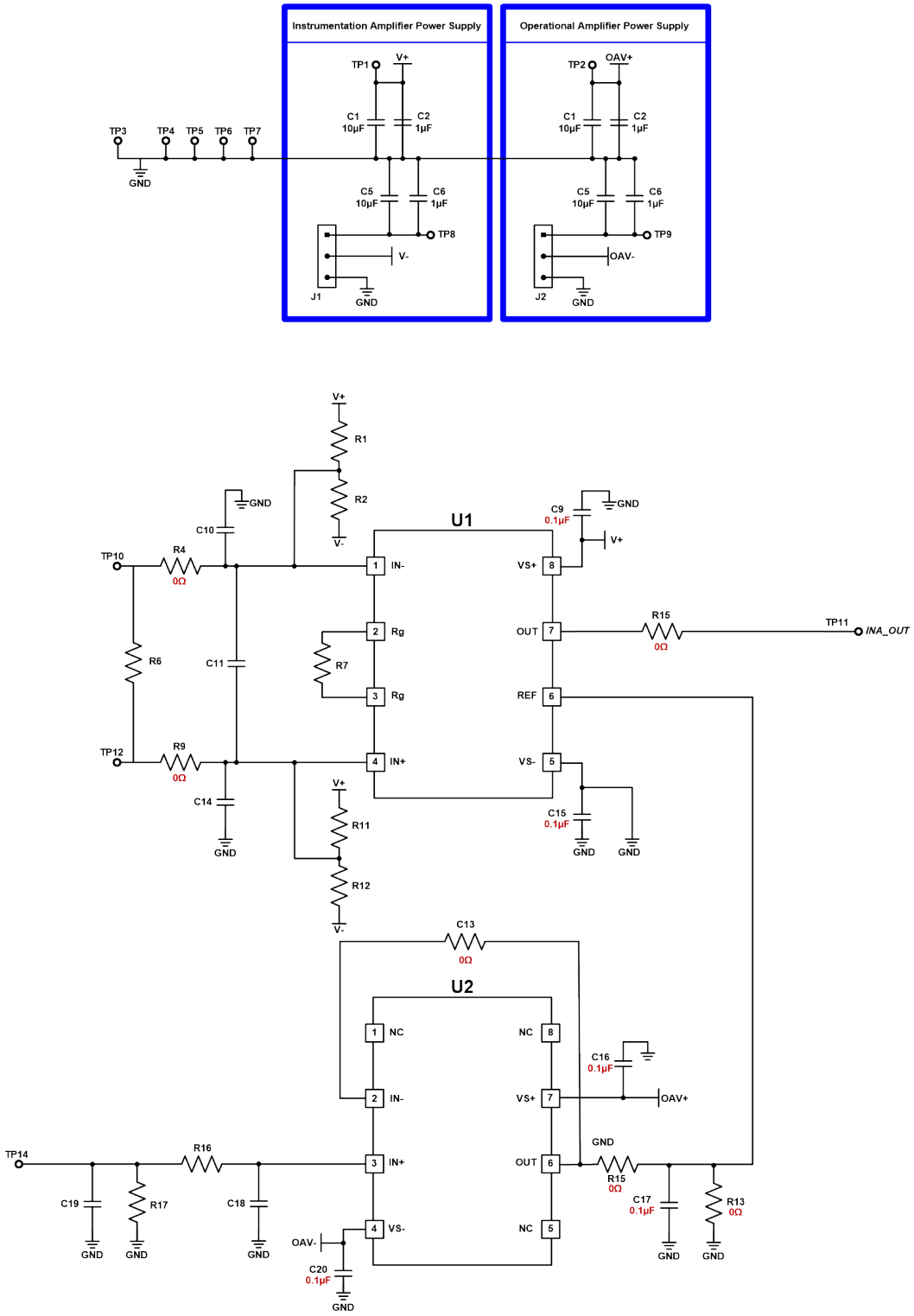

Figure 4. Single-Supply Configuration, Buffered Reference Connection

1. +VS to test point TP1
2. +OAV to test point TP2
3. GND to test points TP8 and TP9
4. Install jumper shunt on positions 2 and 3 on J1 and J2
5. VREF to test point TP14
6. Make sure that resistor R13 is not populated
7. Populate C13 with a 0-Ω resistor. The capacitor and resistor have the same footprint
8. Differential input signal to test points TP10 and TP12
9. Observe output at test points TP11

NOTE: C9 and C15 are prepopulated with 0.1-µF power-supply decoupling capacitors. It is not required to remove C15 for proper single-supply operation. See the respective device data sheet for additional power-supply decoupling information.

3 EVM Components

3.1 Power

Power is applied to the device with test points TP1 and TP8. For the unpopulated device (U2), power is applied using test points TP2 and TP9.

3.2 Inputs

Inputs are applied to the device using test points TP12 and TP10. The inputs for U2 are applied through test points TP14 and TP11.

3.2.1 Input Filtering

R4, R9, and C10, C11, C14 provide the ability to apply common-mode and differential-mode filtering to the inputs. The cutoff frequencies for the filters are shown in Equation 1 and Equation 2.Make C11 approximately ten times larger than C10 and C14. These calculations presume R4 = R9 and C10 = C14.

Common-mode cutoff frequency:

$$f_{c-cm} = \frac{1}{2\pi \times R4 \times C10} \tag{1}$$

Differential-mode cutoff frequency:

$$f_{c-dm} = \frac{1}{2\pi \times (R4 + R9)\left(C11 + \frac{C10}{2}\right)} \tag{2}$$

3.3 Output

Access the output of the device with test point TP11.

3.3.1 Output Filtering

R5 and C12 provide the ability to apply a single-pole RC output filter. The cutoff frequency of the output filter can be calculated as shown in Equation 3.

$$f_{c-o} = \frac{1}{2\pi \times R5 \times C12} \tag{3}$$

3.4 Reference

There are multiple methods of applying a reference voltage to the device. A straightforward approach is to apply a voltage to test point TP13 with U2 and R13 not populated. If a buffered voltage is desired, U2 can be populated with an operational amplifier in an appropriate SO-8 package and pinout. If the reference voltage is GND, R5 is populated with a 0-Ω resistor.

3.5 Miscellaneous

C1, C2, C5, and C6 are the populated bypass capacitors for the device, U1. Similarly, C3, C4, C7 and C8 are populated to provide supply bypassing for U2.

4 Schematic, PCB Layout, and Bill of Materials

4.1 Schematic

The schematic for the PCB for the SOIC-8 EVM is shown in Figure 5 and Figure 6.

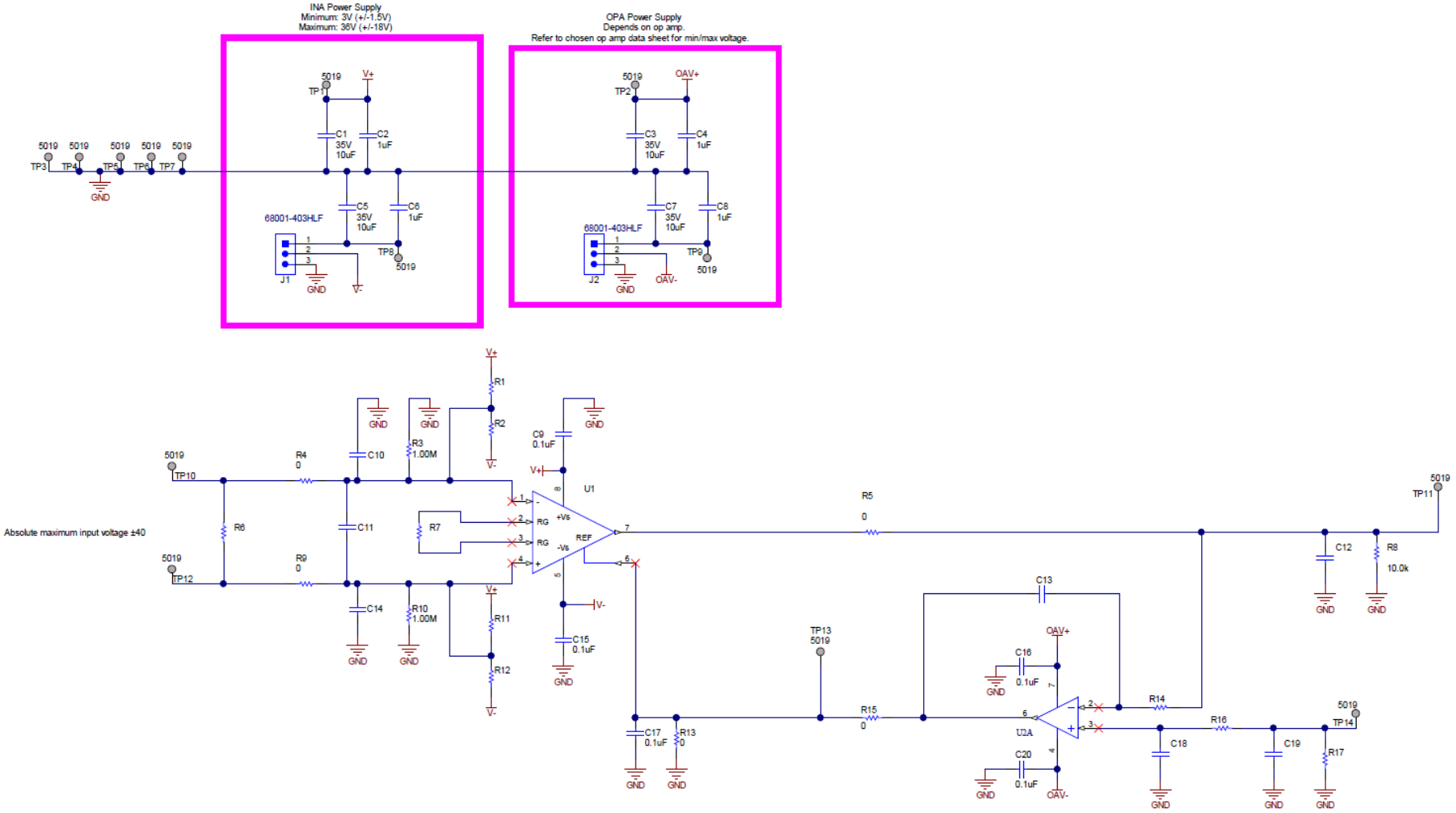

Figure 5. Universal INAEVM-ALT-SO8 Schematic (1)

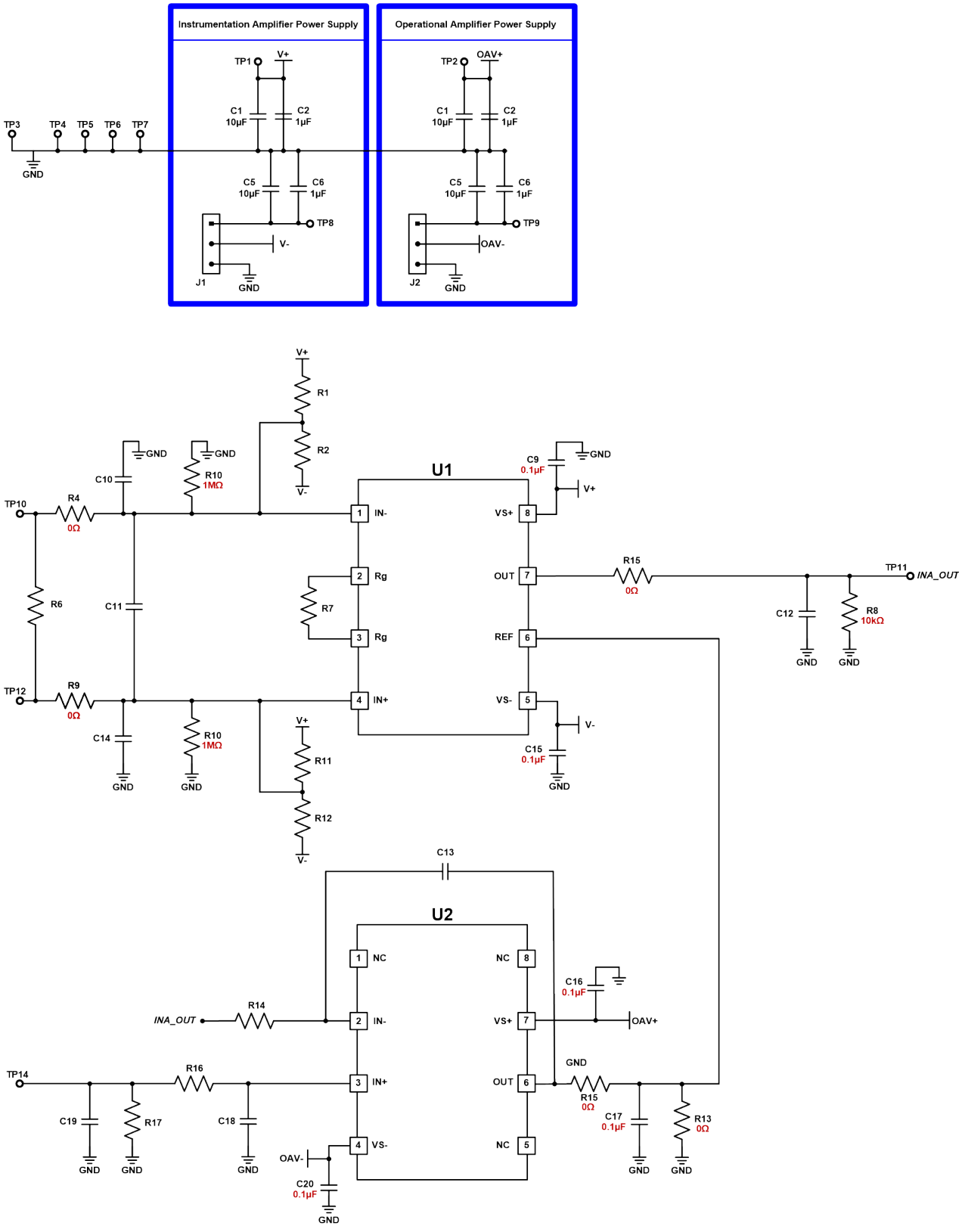

Figure 6. Universal INAEVM-ALT-SO8 Schematic (2)

4.2 PCB Layout

The component PCB layout for the SOIC-8 EVM is shown in Figure 7.

NOTE: Figure 7 is intended to show how the board is laid out; it is not intended to be used for manufacturing PCBs.

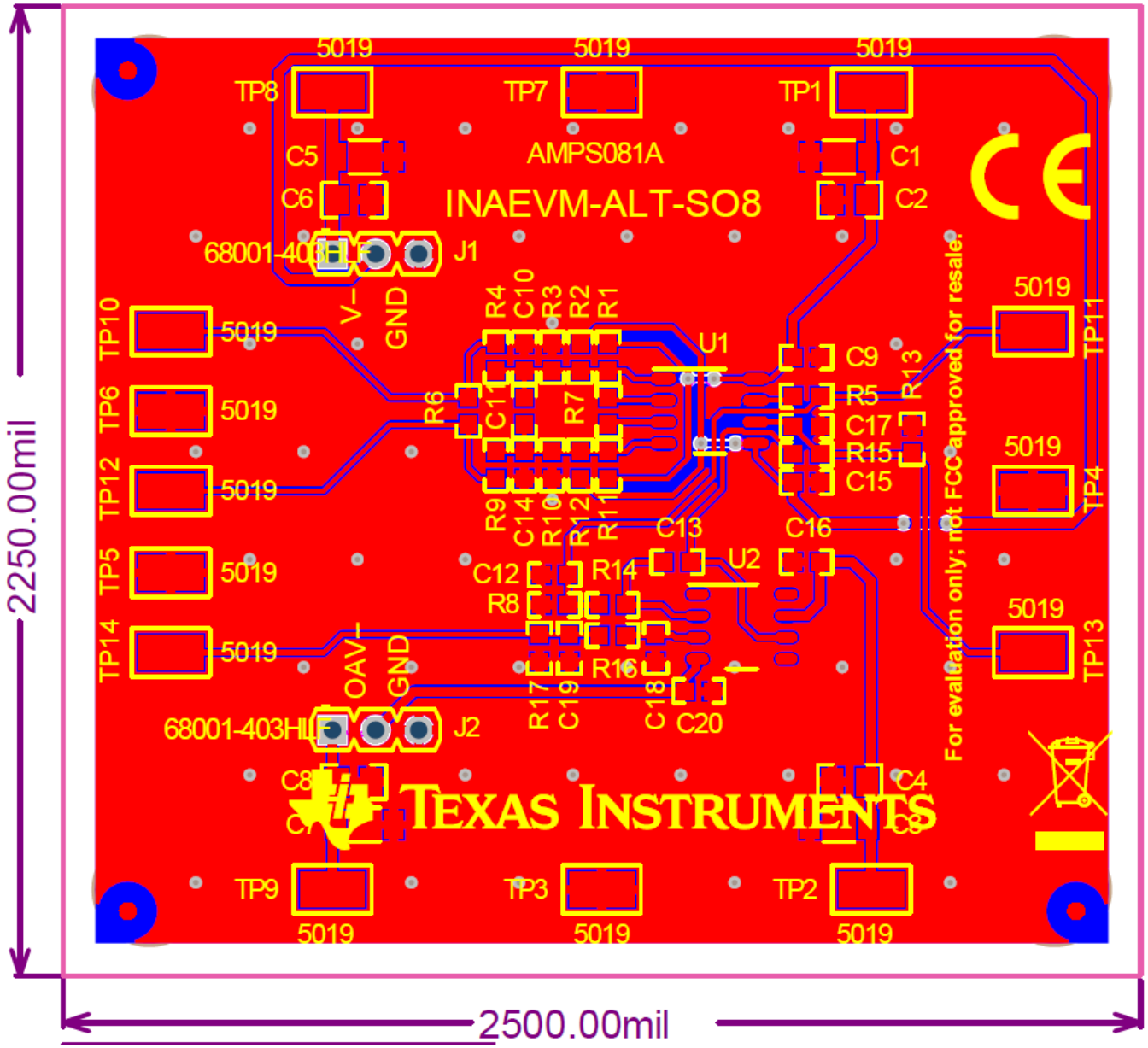

Figure 7. Universal INAEVM-ALT-SO8 PCB

4.3 Bill of Materials

Table 1 provides the parts list for the EVM.

Table 1. Universal INAEVM-ALT-SO8 Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C1, C3, C5, C7	4	10 µF	CAP, CERM, 10 uF, 35 V, +/- 10%, X7R, 1206	1206	C3216X7R1V106K160AC	TDK
C2, C4, C6, C8	4	1 µF	CAP, CERM, 1 uF, 100 V, +/- 10%, X7S, 0805	0805	C2012X7S2A105K125AB	TDK
C9, C15	2	0.1 µF	CAP, CERM, 0.1 uF, 100 V, +/- 10%, X7S, AEC-Q200 Grade 1, 0603	0603	CGA3E3X7S2A104K080AB	TDK
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.25 X 0.075, Clear	75x250 mil	SJ5382	3M
J1, J2	2		Header, 2.54mm, 3x1, Tin, TH	Header, 2.54mm, 3x1, TH	68001-403HLF	FCI
R3, R10	2	1.00 MΩ	RES, 1.00 M, 1%, 0.125 W, 0603	0603	MCT06030C1004FP500	Vishay/Beyschlag
R4, R5, R9, R13	4	0	RES, 0, 5%, 0.1 W, 0603	0603	MCT06030C1004FP500	Vishay/Beyschlag
SH-J1, SH-J2	2	1 x 2	Shunt, 100mil, Gold plated, Black	Shunt	382811-6	AMP
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14	14		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone

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