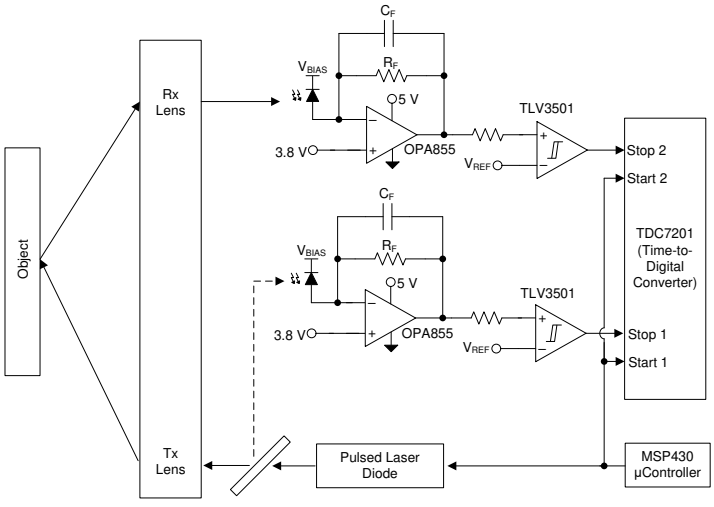
OPA855 8GHz Gain Bandwidth Product, Gain of 7V/V Stable, Bipolar Input Amplifier

1 Features

- High gain bandwidth product: 8GHz
- Decompensated, gain ≥ 7V/V (stable)
- Low input voltage noise: 0.98nV/√Hz
- Slew rate: 2750V/µs
- Low Input capacitance:
  - Common-mode: 0.6pF
  - Differential: 0.2pF
- Wide input common-mode range:
  - 0.4V from positive supply
  - 1.1V from negative supply
- $3V_{PP}$ total output swing
- Supply voltage range: 3.3V to 5.25V
- Quiescent current: 17.8mA
- Package: 8-pin WSON
  - Bare die
- Temperature range: –40°C to +125°C

2 Applications

- Optical time domain reflectometry (OTDR)
- 3D scanner
- Laser distance measurement
- Solid-state scanning LIDAR
- Optical ToF position sensor
- Drone vision
- Industrial robot LIDAR
- Vacuum robot LIDAR
- Silicon photomultiplier (SiPM) buffer amplifier
- Photomultiplier tube post amplifier



High-Speed Time-of-Flight Receiver

3 Description

The OPA855 is a wideband, low-noise operational amplifier with bipolar inputs for wideband transimpedance and voltage amplifier applications. When the device is configured as a transimpedance amplifier (TIA), the 8GHz gain bandwidth product (GBWP) enables high closed-loop bandwidths at transimpedance gains of up to tens of kilohms.

The following graph shows the bandwidth and noise performance of the OPA855 as a function of the photodiode capacitance when the amplifier is configured as a TIA. The total noise is calculated along a bandwidth range extending from dc to the calculated frequency (*f*) on the left scale. The OPA855 package has a feedback pin (FB) that simplifies the feedback network connection between the input and the output.

The OPA855 is optimized to operate in optical time-of-flight (ToF) systems where the OPA855 is used with time-to-digital converters, such as the TDC7201. Use the OPA855 to drive a high-speed analog-to-digital converter (ADC) in high-resolution LIDAR systems with a differential output amplifier, such as the THS4541 or LMH5401 devices.

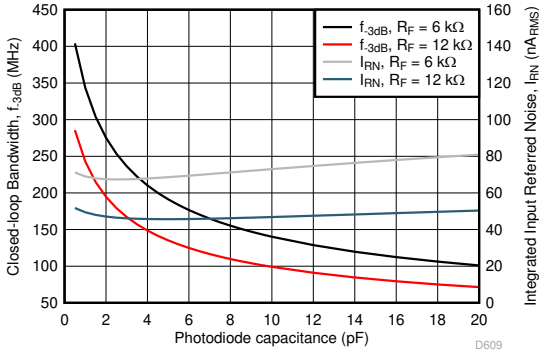
Package Information

PART NUMBER(1)	PACKAGE(2)	PACKAGE SIZE(3)
OPA855	DSG (WSON, 8)	2mm × 2mm

Device Information

PART NUMBER(1)	PACKAGE(2)	DIE SIZE (NOM)
OPA855	Bare die	0.751mm × 0.705mm

(1) See the *Device Comparison Table*.
(2) For more information, see Section 12.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Photodiode Capacitance vs Bandwidth and Noise

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4 Device Comparison Table

DEVICE	INPUT TYPE	MINIMUM STABLE GAIN (V/V)	VOLTAGE NOISE (nV/√Hz)	INPUT CAPACITANCE (pF)	GAIN BANDWIDTH (GHz)
OPA855	Bipolar	7	0.98	0.8	8
OPA856	Bipolar	1	0.9	1.1	1.1
OPA858	CMOS	7	2.5	0.8	5.5
OPA859	CMOS	1	3.3	0.8	0.9
LMH6629	Bipolar	10	0.69	5.7	4

5 Pin Configuration and Functions

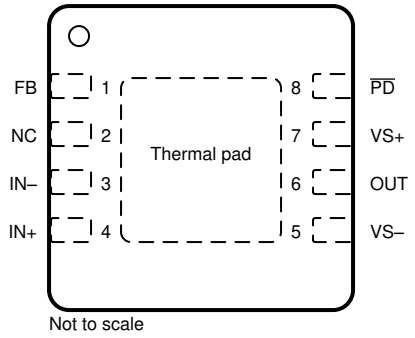


**Figure 5-1. DSG Package,
8-Pin WSON With Exposed Thermal Pad
(Top View)**

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
FB	1	Input	Feedback connection to output of amplifier
IN–	3	Input	Inverting input
IN+	4	Input	Noninverting input
NC	2	—	Do not connect
OUT	6	Output	Amplifier output
$\overline{PD}$	8	Input	Power down connection. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal operation.
VS–	5	—	Negative voltage supply
VS+	7	—	Positive voltage supply
Thermal pad		—	Connect the thermal pad to VS–

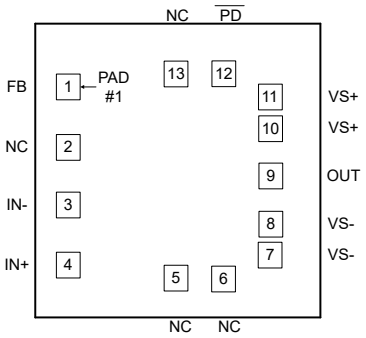


Figure 5-2. Bare Die Package

Table 5-2. Bond Pad Functions

PAD		TYPE	DESCRIPTION
NAME	NO.		
FB	1	Input	Feedback connection to output of amplifier
IN–	3	Input	Inverting input
IN+	4	Input	Noninverting input
NC	2,5,6, 13	—	Do not connect
OUT	9	Output	Amplifier output
$\overline{PD}$	12	Input	Power down connection. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal operation.
VS–	7,8	—	Negative voltage supply
VS+	10,11	—	Positive voltage supply
Backside		—	Connect to VS–

Table 5-3. Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION
381 µm	Silicon with backgrind	Wafer backside is electrically connected to VS–	AlCu

Table 5-4. Bond Pad Coordinates of Bare Die Version in Microns

PAD NUMBER	PAD NAME	X-MIN	Y-MIN	X-MAX	Y-MAX
1	FB	14.5	537.4	79.5	602.4
2	NC	14.5	379	79.5	444
3	IN–	14.5	227	79.5	292
4	IN+	14.5	68.6	79.5	133.6
5	NC	296.725	34.825	361.725	99.825
6	NC	421.725	34.825	486.725	99.825
7	VS–	545.5	93.8	610.5	158.8
8	VS–	545.5	178.8	610.5	243.8
9	OUT	545.5	303	610.5	368
10	VS+	545.5	427.2	610.5	492.2
11	VS+	545.5	512.2	610.5	577.2
12	$\overline{PD}$	421.325	571.175	486.325	636.175
13	NC	297.125	571.175	362.125	636.175

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Total supply voltage (V_{S+} – $V_{S–}$)		5.5	V
V_{IN+}, $V_{IN–}$	Input voltage	($V_{S–}$) – 0.5	(V_{S+}) + 0.5	V
V_{ID}	Differential input voltage		1	V
VOUT	Output voltage	($V_{S–}$) – 0.5	(V_{S+}) + 0.5	V
I_{IN}	Continuous input current		±10	mA
I_{OUT}	Continuous output current(2)		±100	mA
T_J	Junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* can cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device can not be fully functional, and this can affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Long-term continuous output current for electromigration limits.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage (V_{S+} – $V_{S–}$)	3.3	5	5.25	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA855 DSG (WSON) 8 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	80.1	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	100	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	45	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	6.8	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	45.2	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	22.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at V_{S+} = 5 V, V_{S-} = 0 V, G = 7 V/V, R_F = 453 Ω, input common-mode biased at midsupply, R_L = 200 Ω, output load is referenced to midsupply, and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 100 mV_{PP}		2.5		GHz
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		850		MHz
GBWP	Gain-bandwidth product			8		GHz
	Bandwidth for 0.1-dB flatness			200		MHz
SR	Slew rate (10%–90%)	V_{OUT} = 2-V step		2750		V/µs
t_r	Rise time	V_{OUT} = 100-mV step		0.17		ns
t_f	Fall time	V_{OUT} = 100-mV step		0.17		ns
	Settling time to 0.1%	V_{OUT} = 2-V step		2.3		ns
	Settling time to 0.001%	V_{OUT} = 2-V step		2600		ns
	Overshoot or undershoot	V_{OUT} = 2-V step		5%		
	Overdrive recovery	2 × output overdrive		3		ns
HD2	Second-order harmonic distortion	f = 10 MHz, V_{OUT} = 2 V_{PP}		90		dBc
		f = 100 MHz, V_{OUT} = 2 V_{PP}		65		
HD3	Third-order harmonic distortion	f = 10 MHz, V_{OUT} = 2 V_{PP}		86		dBc
		f = 100 MHz, V_{OUT} = 2 V_{PP}		74		
e_n	Input-referred voltage noise	f = 1 MHz		0.98		nV/√Hz
e_i	Input-referred current noise	f = 1 MHz		2.5		pA/√Hz
z_O	Closed-loop output impedance	f = 1 MHz		0.15		Ω
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain(1)		70	76		dB
V_{OS}	Input offset voltage(1)	T_A = 25°C	–1.5	±0.2	1.5	mV
$\Delta V_{OS}/\Delta T$	Input offset voltage drift	T_A = –40°C to 125°C		0.5		µV/°C
I_B	Input bias current (2)	T_A = 25°C	–18.5	–12	–5	µA
$\Delta I_B/\Delta T$	Input bias current drift	T_A = –40°C to +125°C		–0.08		µA/°C
I_{BOS}	Input offset current(1)	T_A = 25°C	–1	±0.1	1	µA
$\Delta I_{BOS}/\Delta T$	Input offset current drift	T_A = –40°C to +125°C		1		nA/°C
CMRR	Common-mode rejection ratio(1)	V_{CM} = ±0.5 V referred to midsupply	90	100		dB
INPUT						
	Common-mode input resistance			2.3		MΩ
C_{CM}	Common-mode input capacitance			0.6		pF
	Differential input resistance			5		kΩ
C_{DIFF}	Differential input capacitance			0.2		pF
V_{IH}	Common-mode input range (high)(1)	CMRR > 80 dB, V_{S+} = 3.3 V	2.7	2.9		V
V_{IL}	Common-mode input range (low)(1)	CMRR > 80 dB, V_{S+} = 3.3 V		1.1	1.3	V
V_{IH}	Common-mode input range (high)(1)	CMRR > 80 dB	4.4	4.6		V
V_{IH}	Common-mode input range (high)	T_A = –40°C to +125°C, CMRR > 80 dB		4.3		V
V_{IL}	Common-mode input range (low)(1)	CMRR > 80 dB		1.1	1.3	V
V_{IL}	Common-mode input range (low)	T_A = –40°C to +125°C, CMRR > 80 dB		1.3		V

6.5 Electrical Characteristics (continued)

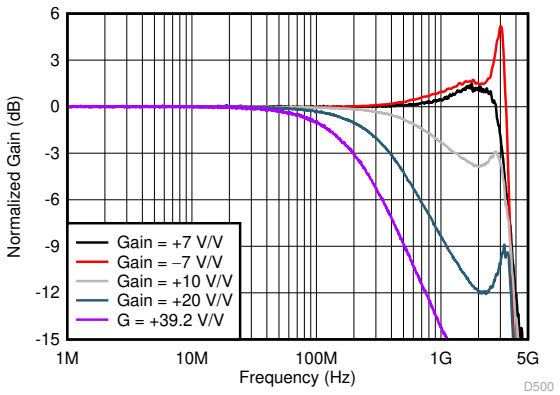
at V_{S+} = 5 V, $V_{S–}$ = 0 V, G = 7 V/V, R_F = 453 Ω, input common-mode biased at midsupply, R_L = 200 Ω, output load is referenced to midsupply, and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_{OH}	Output voltage (high)(3)	T_A = 25°C, V_{S+} = 3.3 V	2.35	2.4		V
V_{OH}	Output voltage (high)(3)	T_A = 25°C	3.95	4.1		V
		T_A = –40°C to +125°C		4		
V_{OL}	Output voltage (low)(3)	T_A = 25°C, V_{S+} = 3.3 V		1.05	1.15	V
V_{OL}	Output voltage (low)(3)	T_A = 25°C		1.05	1.15	V
		T_A = –40°C to +125°C		1.1		
I_{O_LIN}	Linear output drive (sink and source)(1)	R_L = 10 Ω, A_{OL} > 60 dB	65	80		mA
		T_A = –40°C to +125°C, R_L = 10 Ω, A_{OL} > 60 dB		70		
I_{SC}	Output short-circuit current(1)		85	105		mA
POWER SUPPLY						
I_Q	Quiescent current		16	17.8	19.5	mA
		T_A = –40°C		16.7		
		T_A = 125°C		19.5		
PSRR+	Positive power-supply rejection ratio(1)		80	86		dB
PSRR–	Negative power-supply rejection ratio(1)		70	80		
POWER DOWN						
	Disable voltage threshold	Amplifier off when less than this voltage	0.65	1		V
	Enable voltage threshold	Amplifier on when less than this voltage		1.5	1.8	V
	Power-down quiescent current			70	140	µA
	$\overline{PD}$ bias current			70	140	µA
	Turn-on time delay	Time to V_{OUT} = 90% of final value		15		ns
	Turn-off time delay			120		ns

(1) MIN and MAX limits do not apply for bare die.
(2) Current flowing into the input pin is considered negative.
(3) Amplifier output saturated.

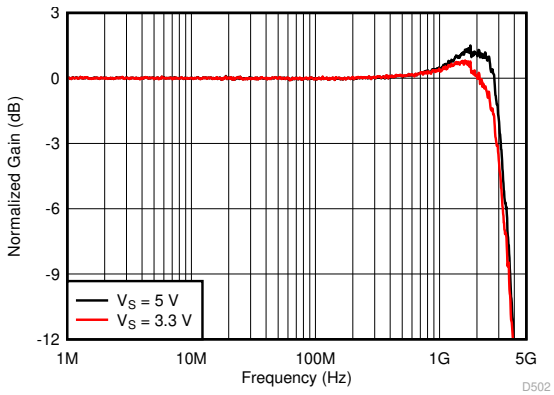
6.6 Typical Characteristics

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, R_F = 453 Ω, gain = 7 V/V, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



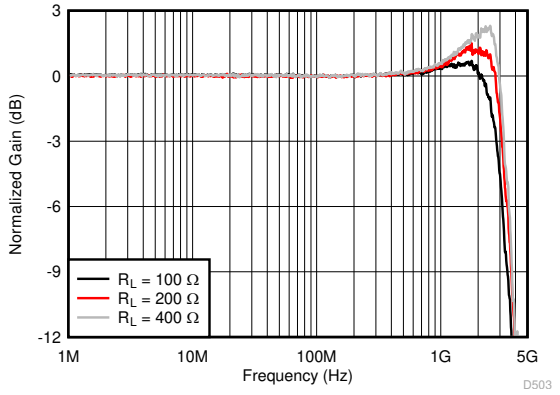
V_{OUT} = 100 mV_{PP}; for circuit configuration, see Section 7

Figure 6-1. Small-Signal Frequency Response vs Gain



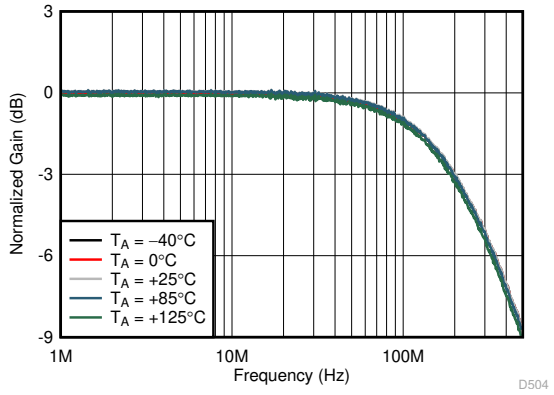
V_{OUT} = 100 mV_{PP}

Figure 6-2. Small-Signal Frequency Response vs Supply Voltage



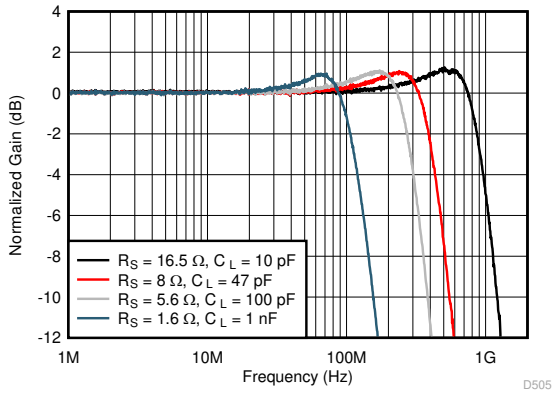
V_{OUT} = 100 mV_{PP}

Figure 6-3. Small-Signal Frequency Response vs Output Load



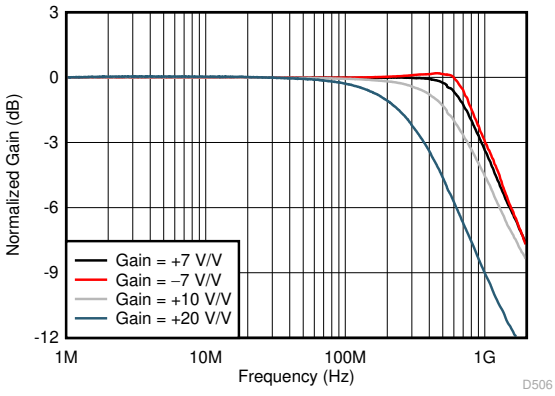
Gain = 39.2 V/V, R_F = 953 Ω, V_{OUT} = 100 mV_{PP}

Figure 6-4. Small-Signal Frequency Response vs Ambient Temperature



V_{OUT} = 100 mV_{PP}; for circuit configuration, see Figure 7-3

Figure 6-5. Small-Signal Frequency Response vs Capacitive Load

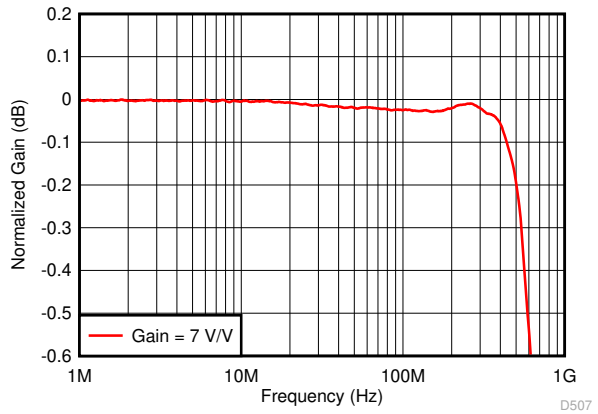


V_{OUT} = 2 V_{PP}

Figure 6-6. Large-Signal Frequency Response vs Gain

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, R_F = 453 Ω, gain = 7 V/V, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



V_{OUT} = 2 V_{PP}

Figure 6-7. Large-Signal Response for 0.1-dB Gain Flatness

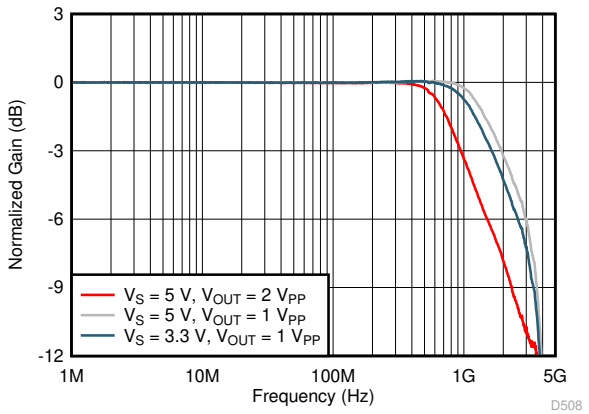
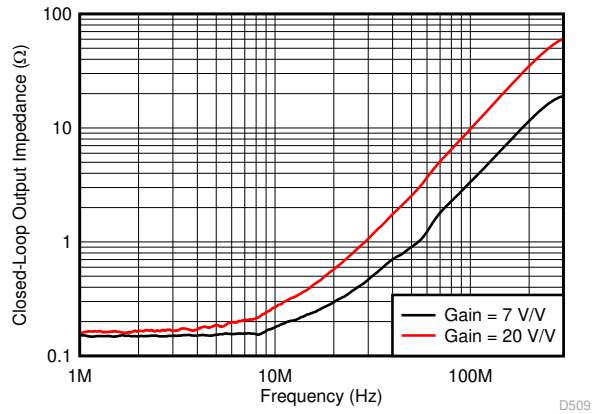
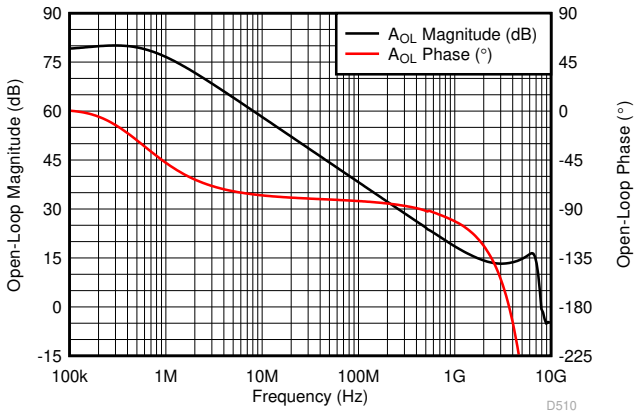


Figure 6-8. Large-Signal Frequency Response vs Voltage Supply



Small-signal response

Figure 6-9. Closed-Loop Output Impedance vs Frequency



Small-signal response

Figure 6-10. Open-Loop Magnitude and Phase vs Frequency

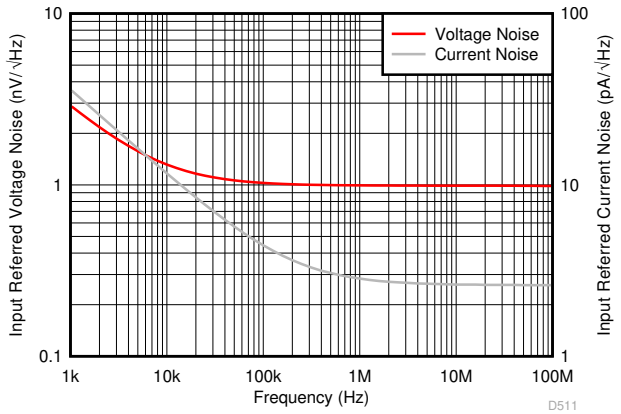
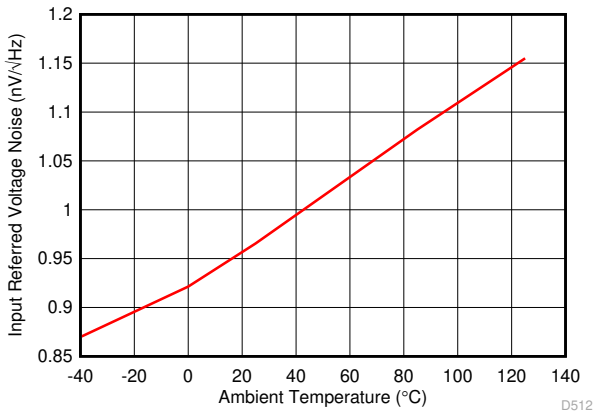


Figure 6-11. Voltage and Current Noise Density vs Frequency



Frequency = 10 MHz

Figure 6-12. Voltage Noise Density vs Ambient Temperature

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, R_F = 453 Ω, gain = 7 V/V, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)

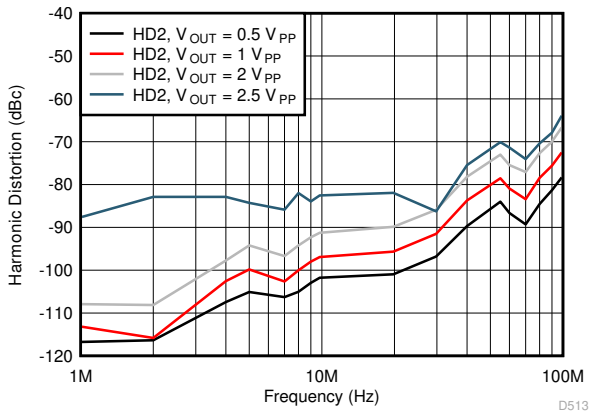


Figure 6-13. Harmonic Distortion (HD2) vs Output Swing

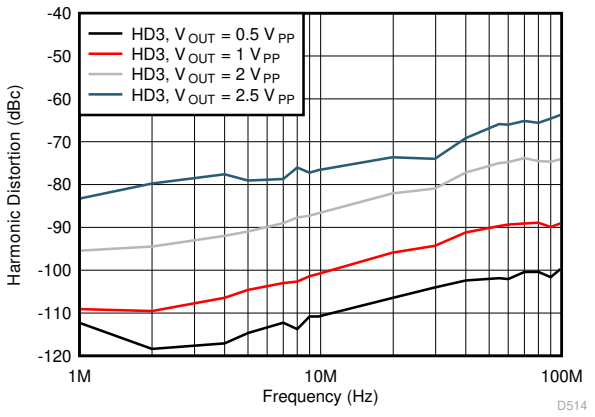


Figure 6-14. Harmonic Distortion (HD3) vs Output Swing

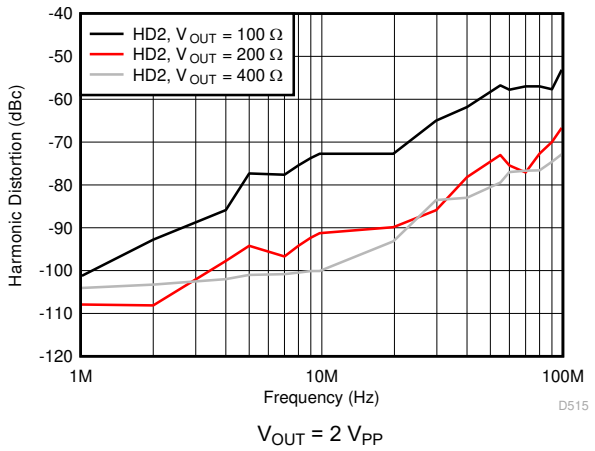


Figure 6-15. Harmonic Distortion (HD2) vs Output Load

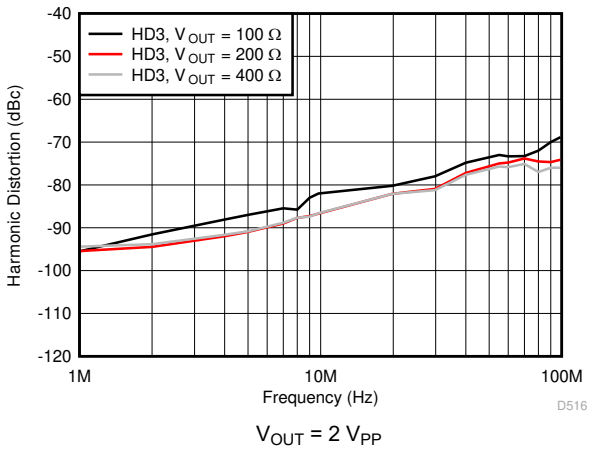


Figure 6-16. Harmonic Distortion (HD3) vs Output Load

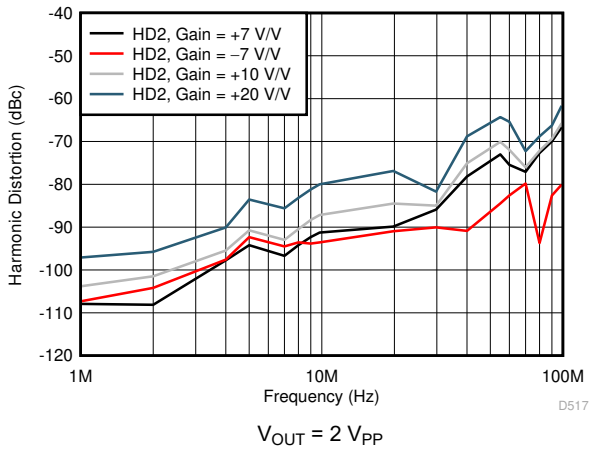


Figure 6-17. Harmonic Distortion (HD2) vs Gain

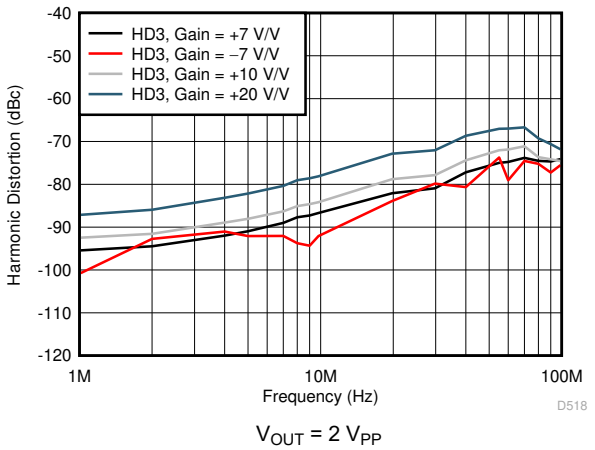
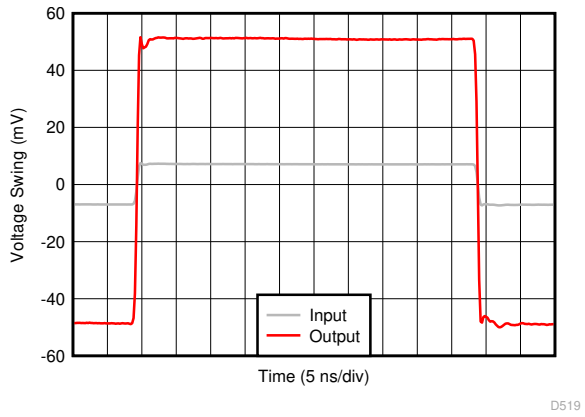


Figure 6-18. Harmonic Distortion (HD3) vs Gain

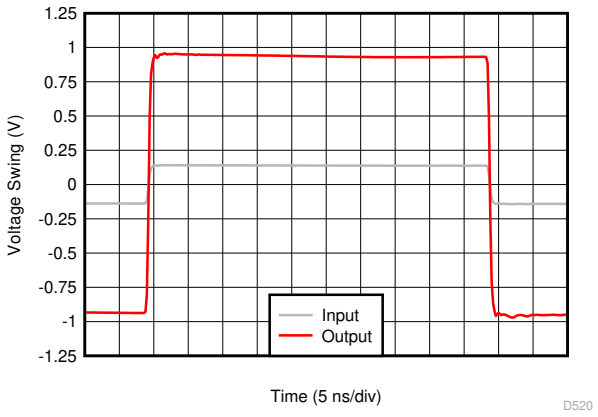
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, R_F = 453 Ω, gain = 7 V/V, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



Average rise-and-fall time (10%–90%) = 300 ps, rise-and-fall time limited by test equipment

Figure 6-19. Small-Signal Transient Response



Average rise and fall time (10%–90%) = 569 ps

Figure 6-20. Large-Signal Transient Response

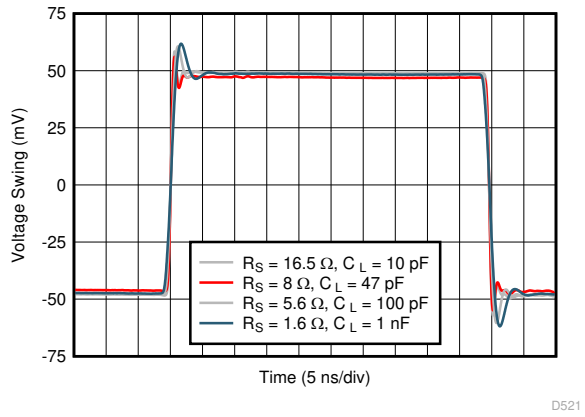
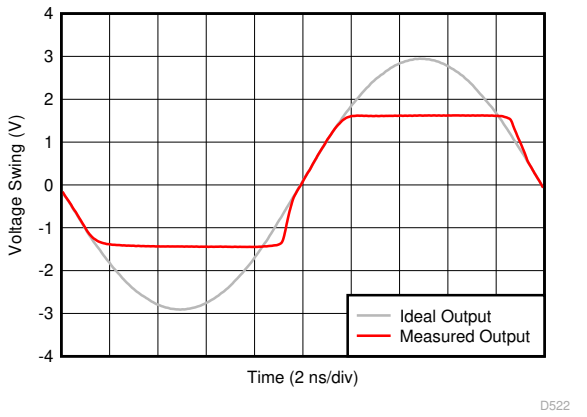


Figure 6-21. Small-Signal Transient Response vs Capacitive Load



2 × output overdrive

Figure 6-22. Output Overload Response

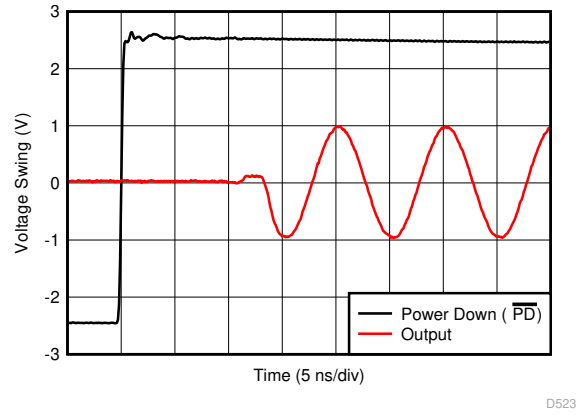


Figure 6-23. Turn-On Transient Response

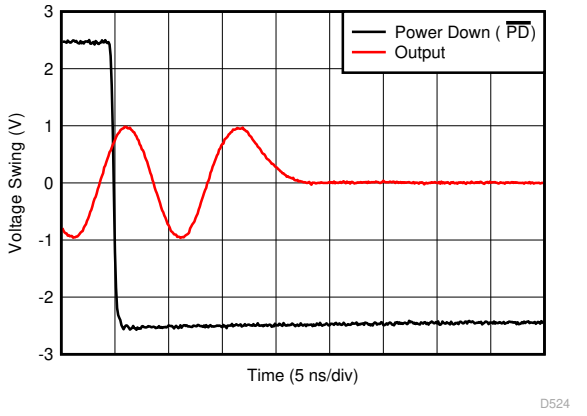
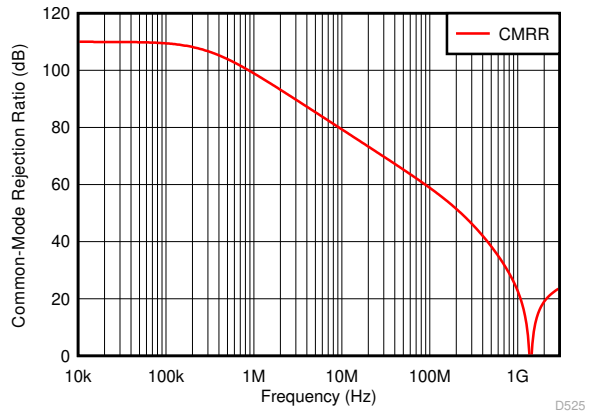


Figure 6-24. Turn-Off Transient Response

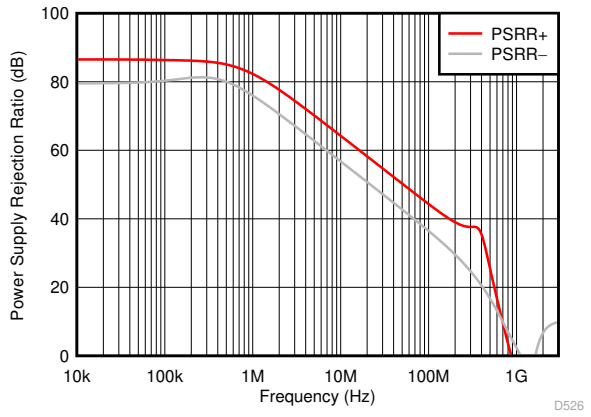
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, R_F = 453 Ω, gain = 7 V/V, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



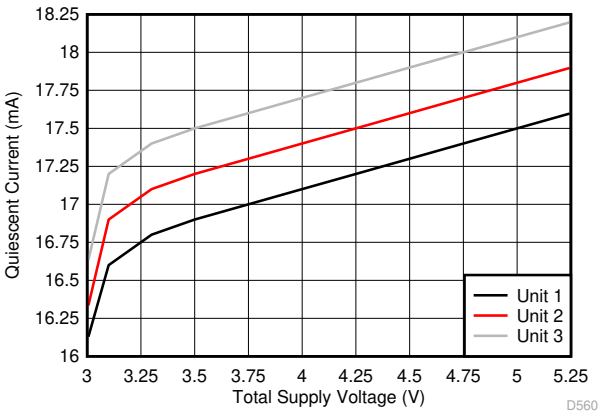
Small-signal response

Figure 6-25. Common-Mode Rejection Ratio vs Frequency



Small-signal response

Figure 6-26. Power Supply Rejection Ratio vs Frequency



3 typical units

Figure 6-27. Quiescent Current vs Supply Voltage

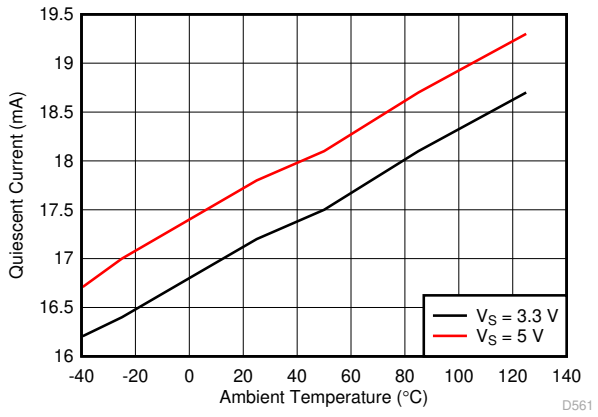
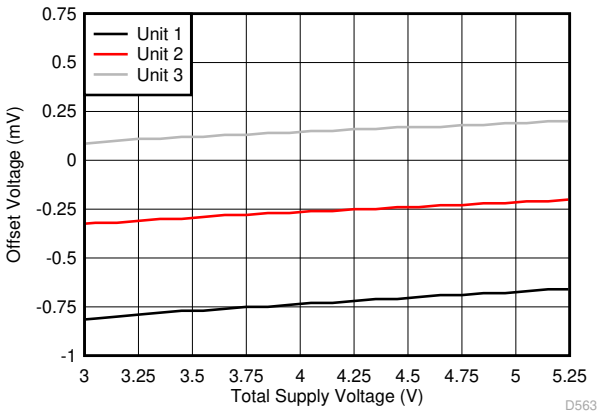
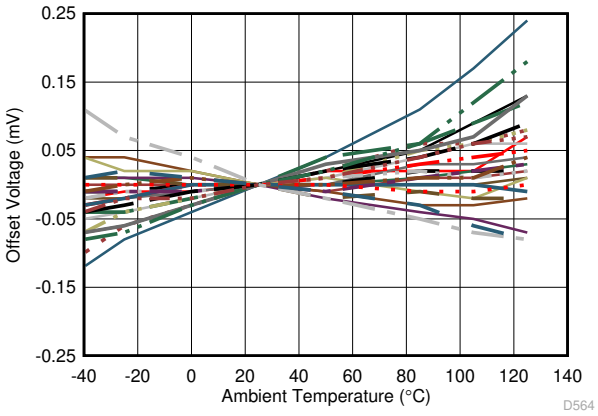


Figure 6-28. Quiescent Current vs Ambient Temperature



3 typical units

Figure 6-29. Offset Voltage vs Supply Voltage

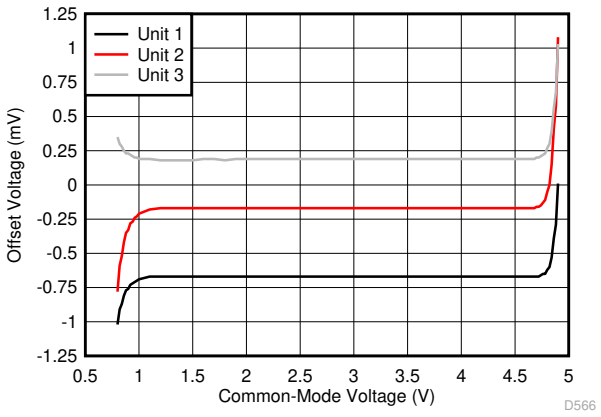


28 units tested, μ = 0.4 μV/°C, σ = 0.7 μV/°C

Figure 6-30. Offset Voltage vs Ambient Temperature

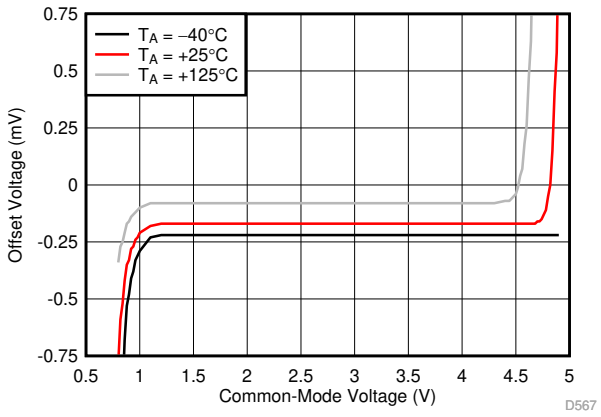
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, R_F = 453 Ω, gain = 7 V/V, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



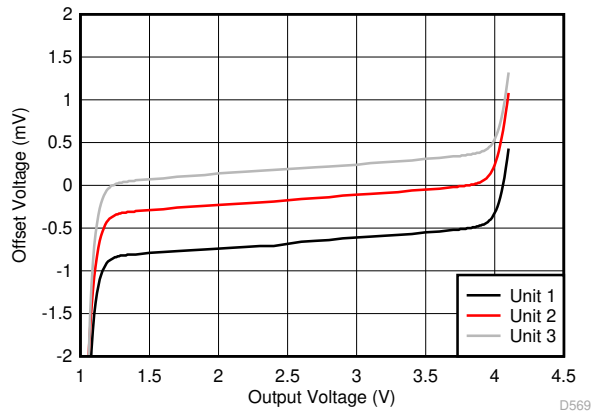
3 typical units, V_{S+} = 5 V, $V_{S–}$ = 0 V

Figure 6-31. Offset Voltage vs Input Common-Mode Voltage



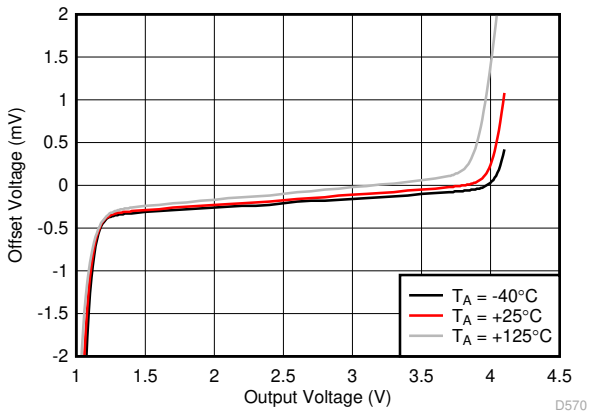
V_{S+} = 5 V, $V_{S–}$ = 0 V

Figure 6-32. Offset Voltage vs Input Common-Mode Voltage



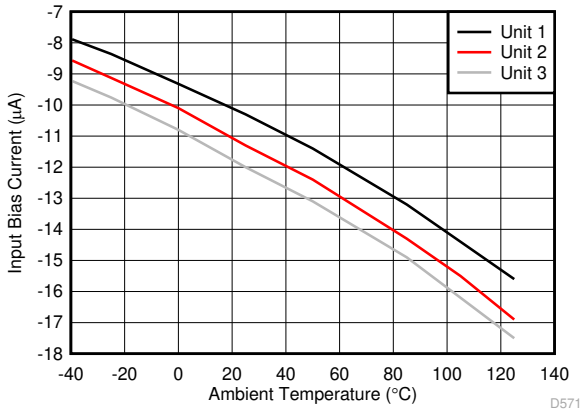
3 typical units, V_{S+} = 5 V, $V_{S–}$ = 0 V

Figure 6-33. Offset Voltage vs Output Swing



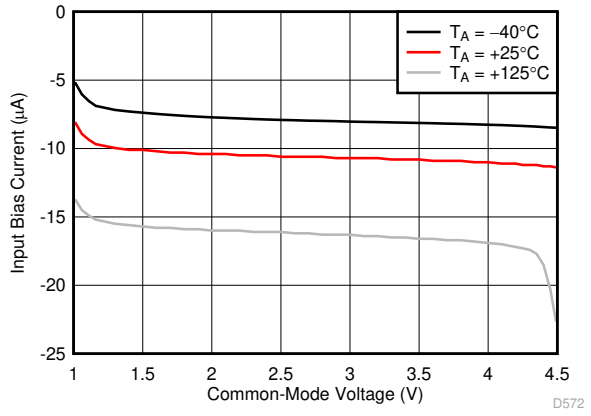
V_{S+} = 5 V, $V_{S–}$ = 0 V

Figure 6-34. Offset Voltage vs Output Swing



3 typical units

Figure 6-35. Input Bias Current vs Ambient Temperature

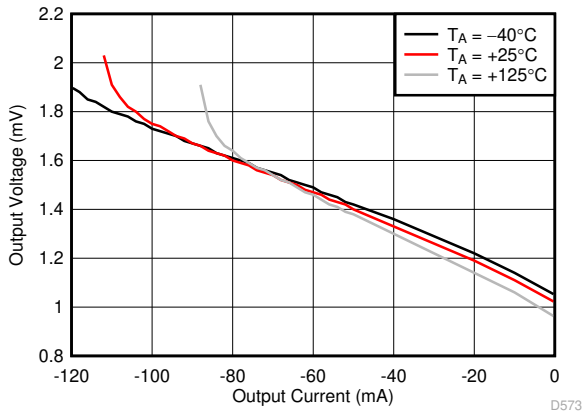


V_{S+} = 5 V, $V_{S–}$ = 0 V

Figure 6-36. Input Bias Current vs Input Common-Mode Voltage

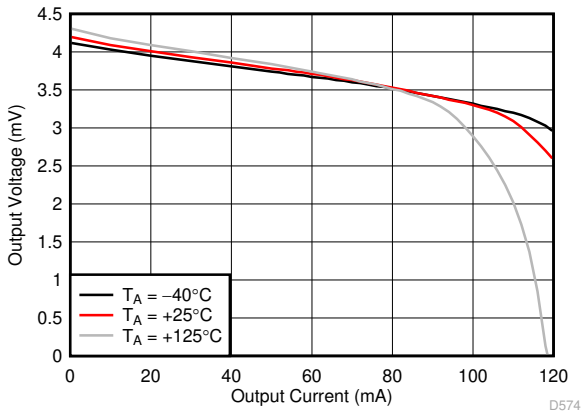
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_{S+} = 2.5 V, $V_{S–}$ = –2.5 V, V_{IN+} = 0 V, R_F = 453 Ω, gain = 7 V/V, R_L = 200 Ω, and output load referenced to midsupply (unless otherwise noted)



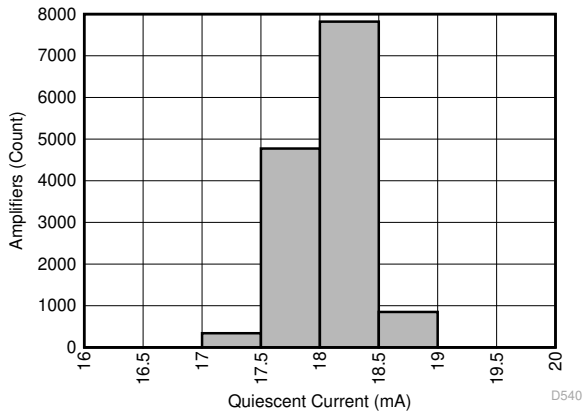
V_{S+} = 5 V, $V_{S–}$ = 0 V

Figure 6-37. Output Swing vs Sinking Current



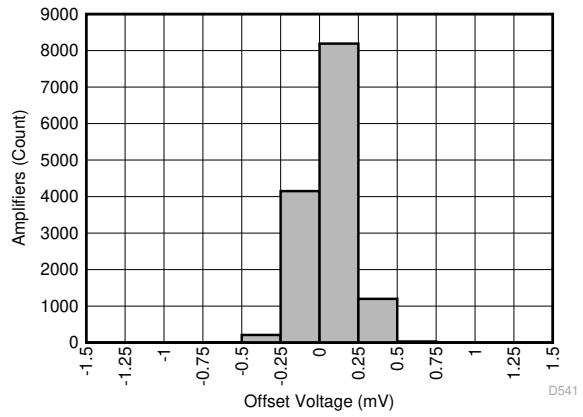
V_{S+} = 5 V, $V_{S–}$ = 0 V

Figure 6-38. Output Swing vs Sourcing Current



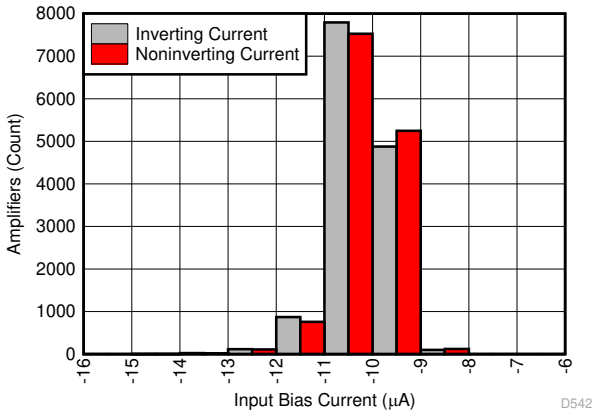
13780 units tested, μ = 17.6 mA, σ = 0.3 mA

Figure 6-39. Quiescent Current Distribution



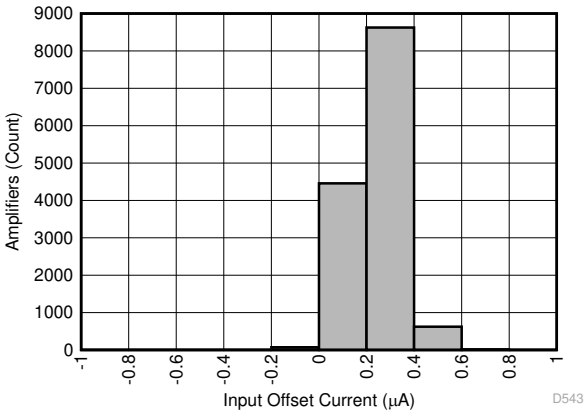
13780 units tested, μ = –0.2 mV, σ = 0.15 mV

Figure 6-40. Offset Voltage Distribution



13780 units tested, μ = –11.2 μA, σ = 0.6 μA

Figure 6-41. Input Bias Current Distribution



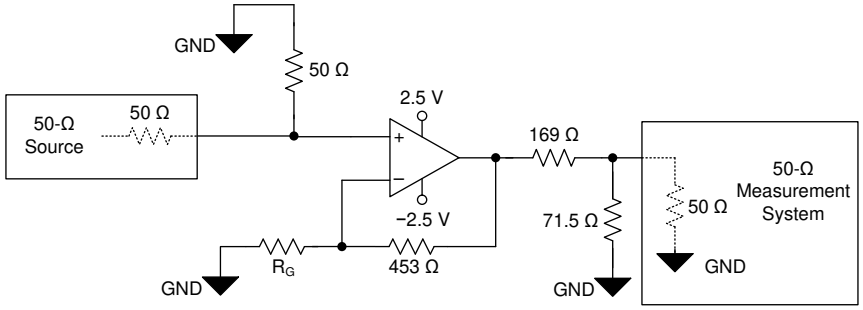
13780 units tested, μ = 0.04 μA, σ = 0.1 μA

Figure 6-42. Input Offset Current Distribution

7 Parameter Measurement Information

The various test setup configurations for the OPA855 are shown in Figure 7-1, Figure 7-2, and Figure 7-3. When configuring the OPA855 in a gain of +39.2 V/V, set the feedback resistor R_F to 953 Ω.

Figure 6-1 shows 5-dB of peaking with the amplifier in an inverting configuration of –7 V/V with the amplifier configured as shown in Figure 7-2. The 50-Ω matched termination of this circuit configuration results in the amplifier being configured in a noise gain of 5.3 V/V, which is lower than the recommended +7 V/V.



R_G values depend on gain configuration

Figure 7-1. Noninverting Configuration

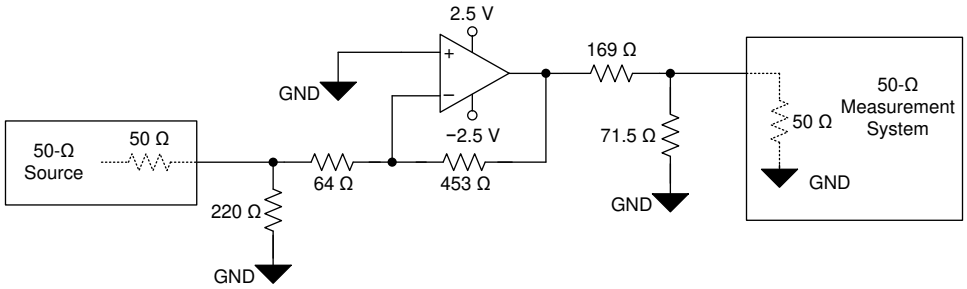


Figure 7-2. Inverting Configuration (Gain = –7 V/V)

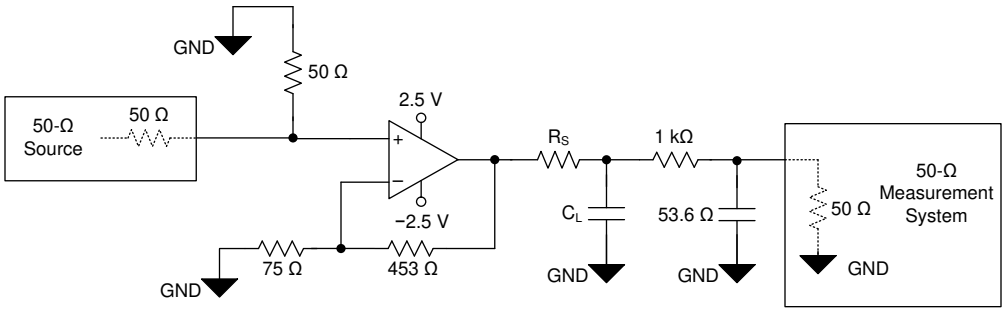


Figure 7-3. Capacitive Load Driver Configuration

8 Detailed Description

8.1 Overview

The ultra-wide, 8-GHz gain bandwidth product (GBWP) of the OPA855, combined with the broadband voltage noise of 0.98 nV/√Hz, produces a viable amplifier for wideband transimpedance applications, high-speed data acquisition systems, and applications with weak signal inputs that require low-noise and high-gain front ends. The OPA855 combines multiple features to optimize dynamic performance. In addition to the wide, small-signal bandwidth, the OPA855 has 850 MHz of large-signal bandwidth (2 V_{PP}), and a slew rate of 2750 V/µs, making the device a viable option for high-speed pulsed applications.

8.2 Functional Block Diagram

The OPA855 is a classic voltage-feedback operational amplifier (op amp) with two high-impedance inputs and a low-impedance output. Standard application circuits are supported, such as the two basic options in Figure 8-1 and Figure 8-2. The resistor on the noninverting pin is used for bias current cancellation to minimize the output offset voltage. In a noninverting configuration, the additional resistors on the noninverting pin add noise to the system; therefore, if SNR is critical, the resistor can be eliminated. In an inverting configuration, the noninverting node is typically connected to a dc voltage; therefore, the high-frequency noise contribution from the bias cancellation resistor can be bypassed by adding a large 1-µF capacitor in parallel to the resistor to shunt the noise. The dc operating point for each configuration is level-shifted by the reference voltage (V_{REF}), which is typically set to midsupply in single-supply operation. V_{REF} is typically connected to ground in split-supply applications.

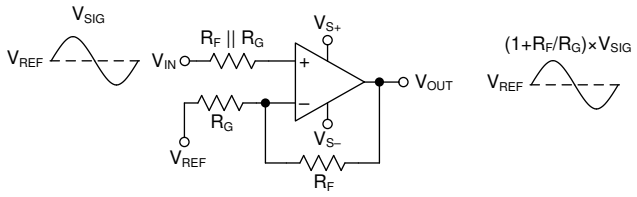


Figure 8-1. Noninverting Amplifier

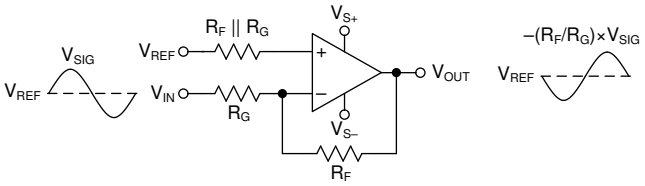


Figure 8-2. Inverting Amplifier

8.3 Feature Description

8.3.1 Input and ESD Protection

The OPA855 is fabricated on a low-voltage, high-speed, BiCMOS process. The internal, junction breakdown voltages are low for these small geometry devices, and as a result, all device pins are protected with internal ESD protection diodes to the power supplies as Figure 8-3 shows. There are two anti-parallel diodes between the inputs of the amplifier that clamp the inputs during an over-range or fault condition.

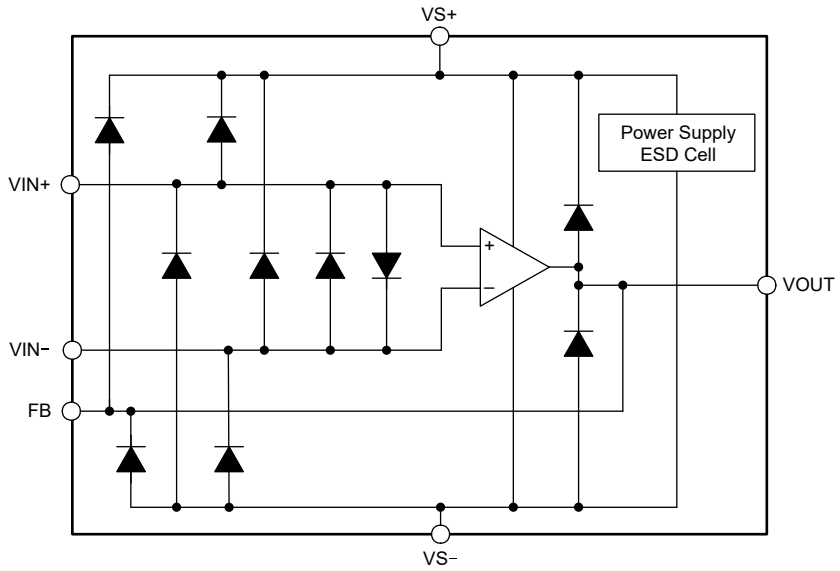


Figure 8-3. Internal ESD Structure

8.3.2 Feedback Pin

The OPA855 pin layout is optimized to minimize parasitic inductance and capacitance, which is a critical care about in high-speed analog design. The FB pin (pin 1) is internally connected to the output of the amplifier. The FB pin is separated from the inverting input of the amplifier (pin 3) by a no connect (NC) pin (pin 2). The NC pin must be left floating. There are two advantages to this pin layout:

1. A feedback resistor (R_F) can connect between the FB and IN– pin on the same side of the package (see Figure 8-4) rather than going around the package.
2. The isolation created by the NC pin minimizes the capacitive coupling between the FB and IN– pins by increasing the physical separation between the pins.

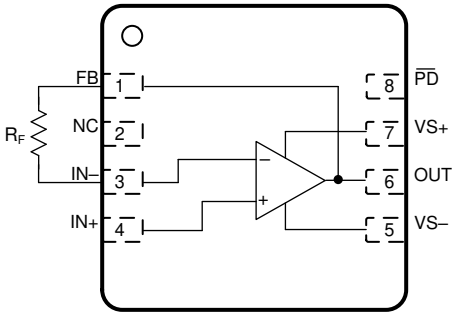


Figure 8-4. R_F Connection Between FB and IN– Pins

8.3.3 Wide Gain-Bandwidth Product

Figure 6-10 shows the open-loop magnitude and phase response of the OPA855. Calculate the gain bandwidth product of any op amp by determining the frequency at which the A_{OL} is 40 dB and multiplying that frequency by a factor of 100. The open-loop response shows the OPA855 to have approximately 62° of phase-margin in a noise gain of 7 V/V. The second pole in the A_{OL} response occurs before the magnitude crosses 0 dB, and the resultant phase margin is less than 0°. This indicates instability at a gain of 0 dB (1 V/V). Amplifiers that are not unity-gain stable are known as decompensated amplifiers. Decompensated amplifiers typically have higher gain-bandwidth product, higher slew rate, and lower voltage noise, compared to a unity-gain stable amplifier with the same amount of quiescent power consumption.

Figure 8-5 shows the open-loop magnitude (A_{OL}) of the OPA855 as a function of temperature. The results show approximately 5° of phase-margin variation over the entire temperature range in a noise gain of 7 V/V. Semiconductor process variation is the naturally occurring variation in the attributes of a transistor (Early-voltage, β, channel-length and width) and other passive elements (resistors and capacitors) when fabricated into an integrated circuit. The process variation can occur across devices on a single wafer or across devices over multiple wafer lots over time. Typically, the variation across a single wafer is tightly controlled. Figure 8-6 shows the A_{OL} magnitude of the OPA855 as a function of process variation over time. The results show the A_{OL} curve for the nominal process corner and the variation one standard deviation from the nominal. The simulated results show less than 2° of phase-margin difference within a standard deviation of process variation in a noise gain of 7 V/V.

One of the primary applications for the OPA855 is as a high-speed transimpedance amplifier (TIA). The low-frequency noise gain of a TIA is 0 dB (1 V/V). At high frequencies the ratio of the total input capacitance and the feedback capacitance set the noise gain. To maximize the TIA closed-loop bandwidth, the feedback capacitance is typically smaller than the input capacitance, which implies that the high-frequency noise gain is greater than 0 dB. As a result, op amps configured as TIAs are not required to be unity-gain stable, which makes a decompensated amplifier a viable option for a TIA. *What You Need To Know About Transimpedance Amplifiers – Part 1* and *What You Need To Know About Transimpedance Amplifiers – Part 2* describe transimpedance amplifier compensation in greater detail.

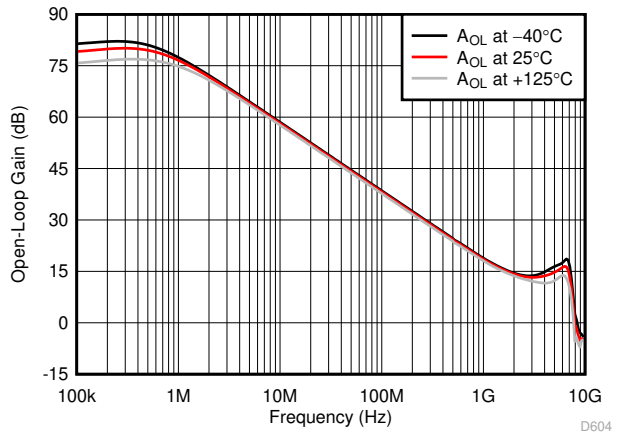


Figure 8-5. Open-Loop Gain vs Temperature

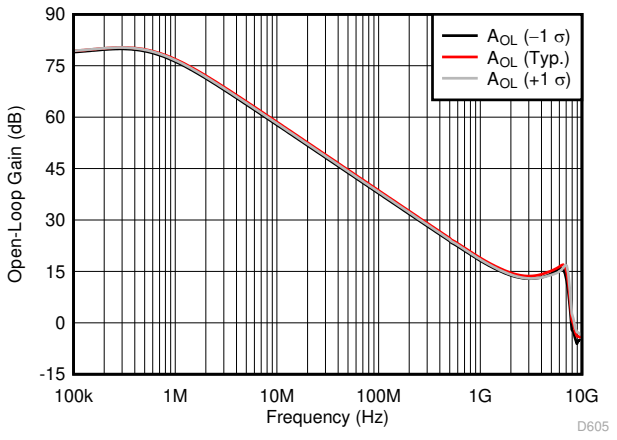


Figure 8-6. Open-Loop Gain vs Process Variation

8.3.4 Slew Rate and Output Stage

In addition to wide bandwidth, the OPA855 features a high slew rate of 2750 V/µs. The slew rate is a critical parameter in high-speed pulse applications with narrow sub-10-ns pulses, such as optical time-domain reflectometry (OTDR) and LIDAR. The high slew rate of the OPA855 implies that the device accurately reproduces a 2-V, sub-ns pulse edge; see also Figure 6-20. The wide bandwidth and slew rate make the OPA855 an excellent amplifier for high-speed signal-chain front ends.

Figure 8-7 shows the open-loop output impedance of the OPA855 as a function of frequency. To achieve high slew rates and low output impedance across frequency, the output swing of the OPA855 is limited to approximately 3 V. The OPA855 is typically used in conjunction with high-speed pipeline ADCs and flash ADCs that have limited input ranges. Therefore, the OPA855 output swing range coupled with the class-leading voltage noise specification maximizes the overall dynamic range of the signal chain.

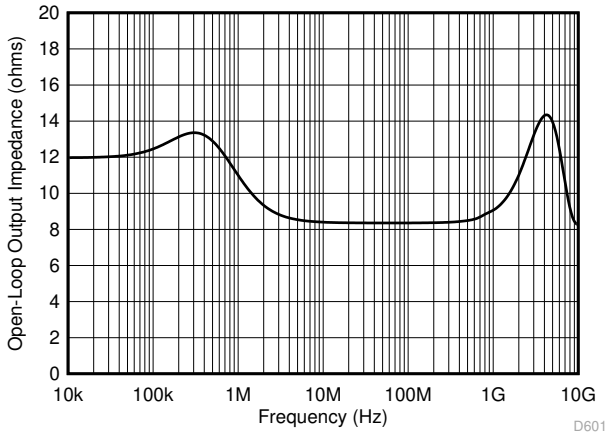


Figure 8-7. Open-Loop Output Impedance (Z_{OL}) vs Frequency

8.4 Device Functional Modes

8.4.1 Split-Supply and Single-Supply Operation

The OPA855 can be configured with single-sided supplies or split supplies; see also Figure 9-11 . Split-supply operation using balanced supplies with the input common-mode set to ground can help ease lab testing (because most signal generators, network analyzers, spectrum analyzers, and other lab equipment typically reference inputs and outputs to ground). In split-supply operation, connect the thermal pad to the negative supply.

Newer systems use a single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA855 can be used with a single positive supply (negative supply at ground) with no change in performance if the input common-mode and output swing are biased within the linear operation of the device. In single-supply operation, level shift the dc input and output reference voltages by half the difference between the power supply rails. This configuration maintains the input common-mode and output load reference at midsupply. To eliminate gain errors, the source driving the reference input common-mode voltage must have low output impedance across the frequency range of interest. In this case, connect the thermal pad to ground.

8.4.2 Power-Down Mode

The OPA855 features a power-down mode to reduce the quiescent current to conserve power. Figure 6-23 and Figure 6-24 show the OPA855 transient response as the $\overline{PD}$ pin toggles between the disabled and enabled states.

The $\overline{PD}$ disable and enable threshold voltages are with reference to the negative supply. If the amplifier is configured with the positive supply at 3.3 V and the negative supply at ground, then the disable threshold voltage is 0.65 V and the enable threshold voltage is 1.8 V. If the amplifier is configured with ±1.65-V supplies, then the disable threshold voltage is –1 V and the enable threshold voltage is 0.15 V. If the amplifier is configured with ±2.5-V supplies, then the disable threshold voltage is –1.85 V and the enable threshold voltage is –0.7 V.

Figure 8-8 shows the switching behavior of a typical amplifier as the $\overline{PD}$ pin is swept down from the enabled to the disabled state. Similarly, Figure 8-9 shows the switching behavior of a typical amplifier as the $\overline{PD}$ pin is swept up from the disabled to the enabled state. The small difference in the switching thresholds between the down sweep and up sweep is due to the hysteresis designed into the amplifier to increase noise immunity on $\overline{PD}$.

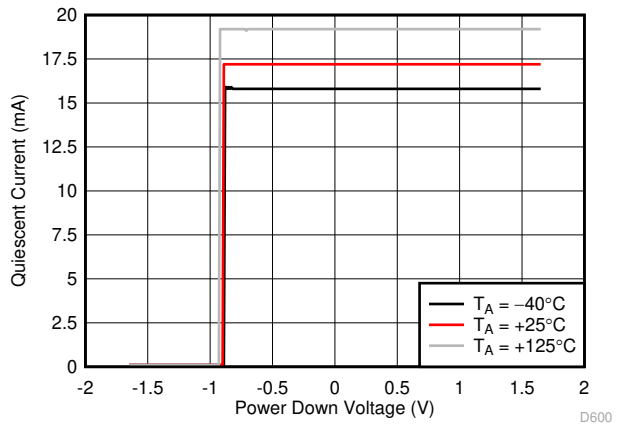


Figure 8-8. Switching Threshold ($\overline{PD}$ Pin Swept From High to Low)

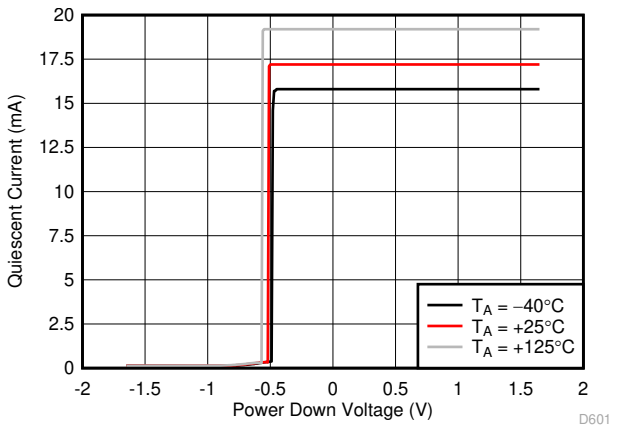


Figure 8-9. Switching Threshold ($\overline{PD}$ Pin Swept From Low to High)

Connecting the $\overline{PD}$ pin low disables the amplifier and places the output in a high-impedance state. When the amplifier is configured as a noninverting amplifier, the feedback (R_F) and gain (R_G) resistor network form a parallel load to the output of the amplifier. To protect the input stage of the amplifier, the OPA855 uses internal, back-to-back protection diodes between the inverting and noninverting input pins; see also Figure 8-3. In the power-down state, if the differential voltage between the input pins of the amplifier exceeds a diode voltage drop, an additional low-impedance path is created between the noninverting input pin and the output pin.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The OPA855 offers very high-bandwidth, high slew-rate, low noise, and better than –60 dBc of distortion performance at frequencies of up to 100 MHz. These features make this device an excellent low-noise amplifier in high-speed data acquisition systems.

9.2 Typical Applications

9.2.1 TIA in an Optical Front-End System

Figure 9-1 shows the OPA855 configured as a transimpedance amplifier (U1) in a wide-bandwidth, optical front-end system. A second amplifier, the OPA859-Q1, configured as a unity-gain buffer (U2) sets a dc offset voltage to the THS4520. The THS4520 is used to convert the single-ended transimpedance output of the OPA855 into a differential output signal. The THS4520 drives the input of the ADS54J64, 14-bit, 1-GSPS analog-to-digital converter (ADC) that digitizes the analog signal.

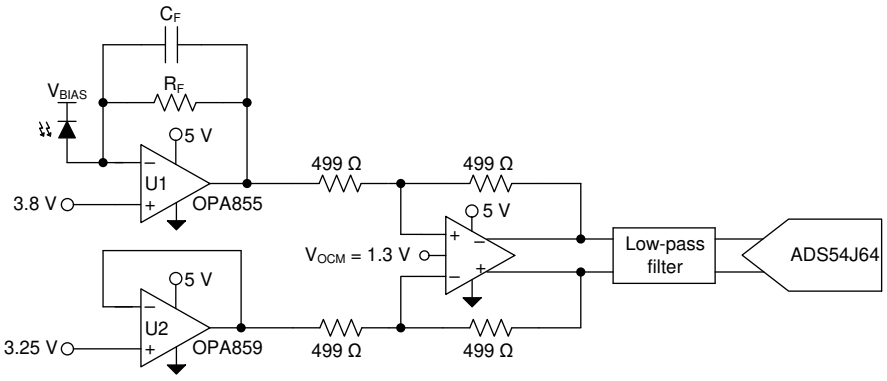


Figure 9-1. OPA855 as a TIA in an Optical Front-End System

9.2.1.1 Design Requirements

The objective is to design a low noise, wideband optical front-end system using the OPA855 as a transimpedance amplifier. The design requirements are:

- Amplifier supply voltage: 5 V
- TIA common-mode voltage: 3.8 V
- THS4520 gain: 1 V/V
- ADC input common-mode voltage: 1.1 V_{PP}
- ADC analog differential input range: 1.1 V_{PP}

9.2.1.2 Detailed Design Procedure

The closed-loop bandwidth of a transimpedance amplifier is a function of the following:

1. The total input capacitance (C_{IN}). This total includes the photodiode capacitance, the input capacitance of the amplifier (common-mode and differential capacitance) and any stray capacitance from the PCB.
2. The op amp gain bandwidth product (GBWP).
3. The transimpedance gain (R_F).

Figure 9-1 shows the OPA855 configured as a TIA, with the avalanche photodiode (APD) reverse biased so that the APD cathode is tied to a large positive bias voltage. In this configuration, the APD sources current into the op amp feedback loop so that the output swings in a negative direction relative to the input common-mode voltage. To maximize the output swing in the negative direction, the OPA855 common-mode voltage is set close to the positive limit; only 1.2 V from the positive supply rail. The feedback resistance (R_F) and the input capacitance (C_{IN}) form a zero in the noise gain that results in instability if left unchecked. To counteract the effect of the zero, a pole is inserted into the noise gain transfer function by adding the feedback capacitor (C_F).

The *Transimpedance Considerations for High-Speed Amplifiers Application Report* discusses theories and equations that show how to compensate a transimpedance amplifier for a particular transimpedance gain and input capacitance. The bandwidth and compensation equations from the application report are available in an Excel® calculator. *What You Need To Know About Transimpedance Amplifiers – Part 1* provides a link to the calculator.

The equations and calculators in the referenced application report and blog posts are used to model the bandwidth (f_{-3dB}) and noise (I_{RN}) performance of the OPA855 configured as a TIA. The resultant performance is shown in Figure 9-2 and Figure 9-3. The left-side Y-axis shows the closed-loop bandwidth performance, whereas the right side of the graph shows the integrated input-referred noise. The noise bandwidth to calculate I_{RN} for a fixed R_F and C_{PD} is set equal to the f_{-3dB} frequency. Figure 9-2 shows the amplifier performance as a function of photodiode capacitance (C_{PD}) for R_F = 6 kΩ and 12 kΩ. Increasing C_{PD} decreases the closed-loop bandwidth. To maximize bandwidth, make sure to reduce any stray parasitic capacitance from the PCB. The OPA855 is designed with 0.8 pF of total input capacitance to minimize the effect of stray capacitance on system performance. Figure 9-3 shows the amplifier performance as a function of R_F for C_{PD} = 1.5 pF and 2.5 pF. Increasing R_F results in lower bandwidth. To maximize the signal-to-noise ratio (SNR) in an optical front-end system, maximize the gain in the TIA stage. Increasing R_F by a factor of X increases the signal level by X, but only increases the resistor noise contribution by √X, thereby improving SNR. Since the OPA855 is a bipolar input amplifier, increasing the feedback resistance increases the voltage offset due to the bias current and also increases the total output noise due to increased noise contributions from the amplifiers current noise.

The OPA859-Q1 configured as a unity-gain buffer drives a DC offset voltage of 3.25 V into the lower half of the THS4520. To maximize the dynamic range of the ADC, the OPA855-Q1 and OPA859-Q1 drive a differential common-mode of 3.8 V and 3.25 V respectively into the THS4520. The dc offset voltage of the buffer amplifier can be derived using Equation 1.

$$V_{BUF\_DC} = V_{TIA\_CM} - \left(\frac{1}{2} \times \frac{V_{ADC\_DIFF\_IN}}{\left(\frac{R_F}{R_G} \right)} \right) \quad (1)$$

where

- V_{TIA_CM} is the common-mode voltage of the TIA (3.8 V)
- $V_{ADC\_DIFF\_IN}$ is the differential input voltage range of the ADC (1.1 V_{PP})
- R_F and R_G are the feedback resistance (499 Ω) and gain resistance (499 Ω) of the THS4520 differential amplifier

The low-pass filter between the THS4520 and the ADC54J64 minimizes high-frequency noise and maximizes SNR. The ADC54J64 has an internal buffer that isolates the output of the THS4520 from the ADC sampling-capacitor input, so a traditional charge bucket filter is not required.

9.2.1.3 Application Curves

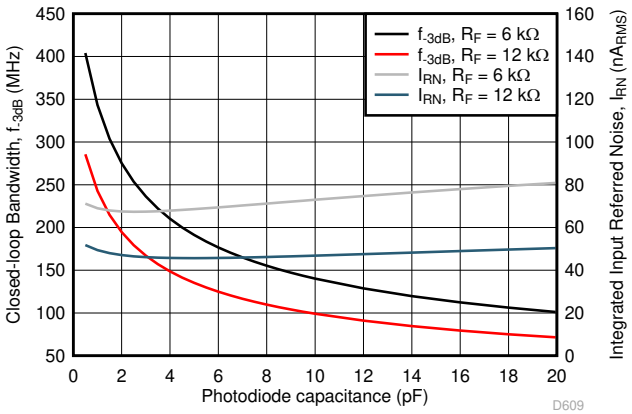


Figure 9-2. Bandwidth and Noise vs Photodiode Capacitance

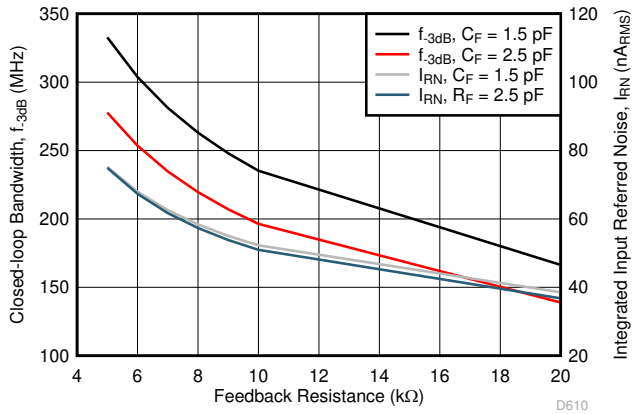


Figure 9-3. Bandwidth and Noise vs Feedback Resistance

9.2.2 Optical Sensor Interface

There are two main approaches for current to voltage conversion. One uses a noninverting voltage feedback amplifier in combination with a shunt resistor to first convert current and then further amplify the optical signal. The other approach configures an amplifier for transimpedance applications which combines both steps into one. Figure 9-4 shows the standard configuration for both approaches.

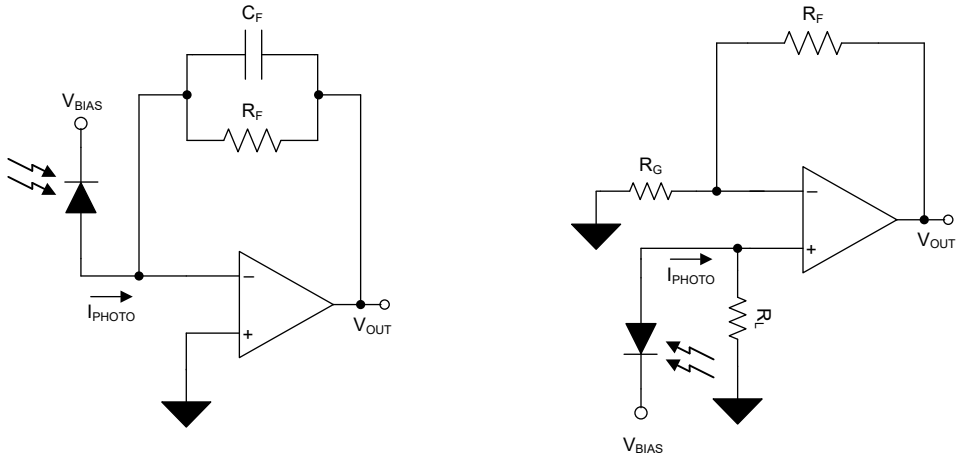


Figure 9-4. Transimpedance Amplifier vs Voltage Feedback Amplifier

Both configurations provide a low output impedance stage which provides the ability to interface with various types of loads. However, the noninverting option comes with a few disadvantages. The TIA input impedance is near zero, since the amplifier keeps the voltage at the inverting input node at the same potential as the non-inverting input node. While the VFB input impedance is equal to the shunt resistor R_L. In the case of the VFB amplifier, the signal response can be slowed due to a large time constant created by the shunt resistor and capacitor. Also, the linearity of the photodetector can suffer, especially for higher detector currents due to the varying voltage bias produced at the shunt resistor. And, since the voltage bias of the photodetector is no longer constant for all detector currents, the diode's internal capacitance can vary. Using a TIA, the voltage bias remains constant at the voltage set by the non-inverting node, and can provide level shifting to the signal which is especially useful for single-supply configurations.

OPA855 offers 8 GHz of gain bandwidth, high slew-rate, and low noise which makes this device an excellent for a wide range of photodetectors. Figure 9-5 shows the OPA855 configured as a transimpedance amplifier (TIA) in a wide-bandwidth, optical front-end system. Various types of optical sensors can be used as an optical input to the amplifier: photodiode (PD), avalanche photodiode (APD), photomultiplier tube (PMT), and multipixel photon counter (MPPC) or known as solid-state photomultiplier (SiPM). Optical detection applications have commonly used APDs, but ultra-low light source detection has been a challenge in past options. With technologies such as PMTs and MPPCs, the high intrinsic gain, while maintaining a fast output, requires a low noise, high-speed interface. The OPA855 can accommodate for these optical challenges and can work equally as well in these applications.

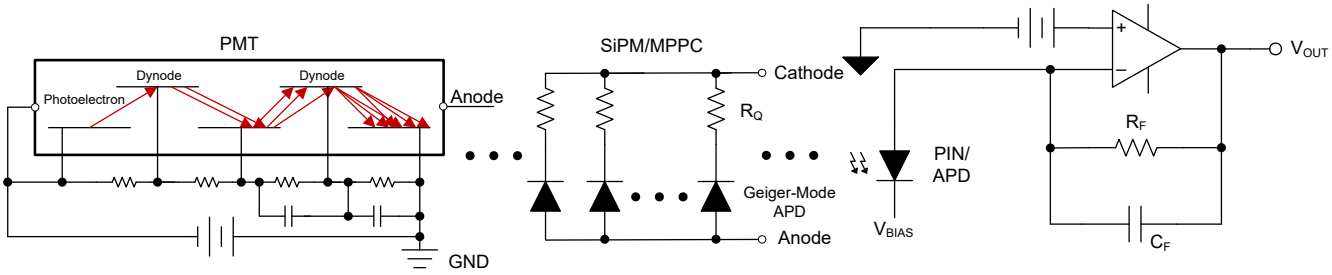


Figure 9-5. Transimpedance Amplifier With APD or SiPM/MPPC or PMT Inputs

Transimpedance applications require low voltage and current noise for an excellent system performance. As a result of the high input impedance structure, the OPA855 has a great balance between low input-referred voltage noise and current noise that is consistent over frequency. Overall, the amplifier noise must have minimal impact to the total noise of the application. Examine the total input referred noise to the optical sensor.

Noise sources in optical sensors vary especially when introducing gain and photon paralleling. Optical power, gain, and applied reverse bias are the main characteristics that can affect signal to noise ratio. Standard photodiodes contribute the lowest noise at the highest quantum efficiency. Internal to photodiodes, noises sources include shot and thermal. Shot noise is a random occurrence of photodetection which arises in periods of both light and dark. Dark current is noise that occurs in the absence of an optical source which can be included with shot noise. And, thermal noise originates from the shunt resistance internal to the diode. At the lower signal levels, shot noise can dominate. Figure 9-6 shows an example of the noise sources present in a transimpedance amplifier circuit. The total TIA noise is the root sum square of each component within the system: photodiode noise, amplifier current noise, amplifier voltage noise, and feedback resistor noise.

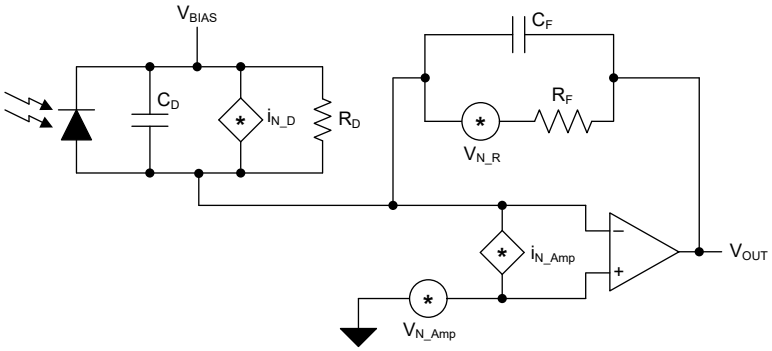


Figure 9-6. Photodiode and TIA Noise Model

Interfacing with APDs is similar to interfacing with PIN PDs, but APDs have additional noise factors due to the internal gain. APDs have increased shot noise and the addition of a multiplication excess noise factor. Decreasing capacitance, increasing diode shunt resistance, and decreasing reverse voltage bias applied to the APD deceases noise at the expense of response time. The MPPCs total noise is comparable to APDs, but with differing noise sources. This optical sensor includes digital-like noise factors such as dark count rate, after pulsing, and optical crosstalk due to the parallel gain cells. For PMTs, dark count rate is lower. In general, PMT total noise is comparable to PDs with an internal gain comparable to APDs. However, PMTs have the lowest quantum efficiency of the optical sensor space.

9.2.2.1 Design Requirements

The objective is to design a low-noise, wideband optical front-end system using a diverse selection of optical sensors: PD, APD, PMT, and MPPC with the OPA855 as the TIA. Table 9-1 lists the approximate design requirements for each type of photodetector.

Table 9-1. Design Parameters

SENSOR	INTRINSIC GAIN (A/W)	REVERSE BIAS (V)	INPUT CAPACITANCE (pF)	TARGET BANDWIDTH (MHZ)	TRANSIMPEDANCE GAIN R_F (kΩ)	TOTAL OPTICAL GAIN (kV/W)
PD (PIN)	1	30	3	15	100	100
APD	100	150	1	200	10	1000
PMT	1×10^6	1250	50	100	1	1×10^6
MPPC (SiPM)	5×10^5	50	100	10	1	5×10^5

9.2.2.2 Detailed Design Procedure

The OPA855 is decompensated and requires a high-frequency gain of 7 V/V or greater to be stable. Using the OPA855 in lower gains results in increased peaking and potential instability. Decompensated amplifiers are advantageous in TIA applications due the inherent characteristics of a TIA design. The zero and pole pair introduced by the input and feedback capacitances along with the feedback resistor increases the noise gain until the flattens out at a high gain with a magnitude shown in Equation 2.

$$1 + \frac{C_{TOT}}{C_F} \tag{2}$$

where

- C_{TOT} is the total input capacitance of the amplifier (includes photodetector capacitance and the common-mode and differential input capacitance of the amplifier)
- C_F is the feedback capacitance of the amplifier

A decompensated amplifier allows for benefits such as increased open loop gain, increased bandwidth, increased slew rate, and lower input-referred noise for the same quiescent current relative to the unity gain stable counterpart.

Similar to the concept described in Section 9.2.1.2, the rise time and the internal capacitance of the photodetector determines the closed-loop bandwidth. Both the closed-loop bandwidth and the transimpedance gain (R_F) determine the necessary gain bandwidth (GBWP) of the amplifier. Table 9-1 shows the standard photodiode characteristics based on type of photodetector. Target values such as the system bandwidth and gain are calculated using these concepts with the chosen photodiode characteristics. Detailed explanations and equations can be found in the application reports discussed in Section 9.2.1.2.

Figure 9-5 shows the OPA855 configured as a TIA, with the optical sensor reverse biased so that the diode cathode is tied to the positive bias voltage. A RC filter can be used at the reverse bias node as a low-pass filter to eliminate high-frequency noise. The internal capacitance of photodetectors vary based on sensor type and the value of the applied reverse voltage. The setups between each sensor type slightly differs, but the connection to the amplifier is consistent throughout.

The difference between each optical design comprise choosing the feedback resistor to set the transimpedance gain, and the feedback capacitance to compensate for the additional input capacitance. With an 8-GHz GBWP, the OPA855 can accommodate very fast rise times to pair with emerging optical sensors to meet industry demands for faster optical detections.

The dc voltage bias at the noninverting input of the OPA855 shown in Figure 9-5 sets the common-mode voltage which maximizes the output swing of the system in mismatched power supply configurations. The dc bias is critical to avoid clipping or saturating the output stage of the amplifier. For the later stages, a fully differential amplifier (FDA) can be used to convert single-ended signal to a differential input to drive an analog-to-digital converter (ADC) as shown in Figure 9-1. Higher order filters can be added between the FDA and ADC for system noise reduction.

Figure 9-7 shows the performance that results from the design parameters provided in Table 9-1, and Figure 9-8 shows the general trends. Both figures depict the closed-loop bandwidth performance of the OPA855 configured as a TIA using different sensor types and gain configurations. Figure 9-7 shows the amplifier performance based on the chosen photodetector from the values provided in Table 9-1. PMTs and MPPCs have higher intrinsic gains, but requires a wide bandwidth to compensate for the higher internal capacitance. Whereas, PDs and APDs require higher gain configurations to achieve similar output voltage levels. The OPA855 can provide the bandwidth to accommodate for both optical challenges. Figure 9-7 shows a generic view of the amplifier performance as a function of sensor capacitance and transimpedance gain. Increasing the feedback resistance and input capacitance, decreases the closed-loop bandwidth. Throughout the trends, the amount of change in closed-loop bandwidth is consistent in relationship of the changes in both terms. A photodiode capacitance of 1 pF and a feedback resistance of 1 kΩ results in a very high closed-loop system bandwidth of 1.1 GHz.

9.2.2.3 Application Curves

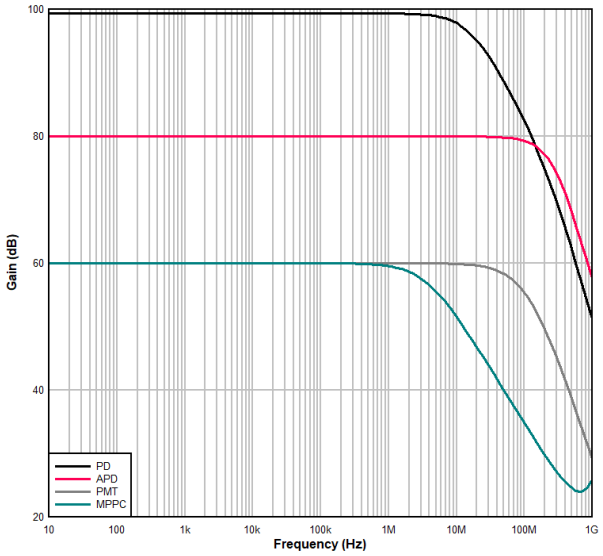


Figure 9-7. Optical Sensor TIA Frequency Response

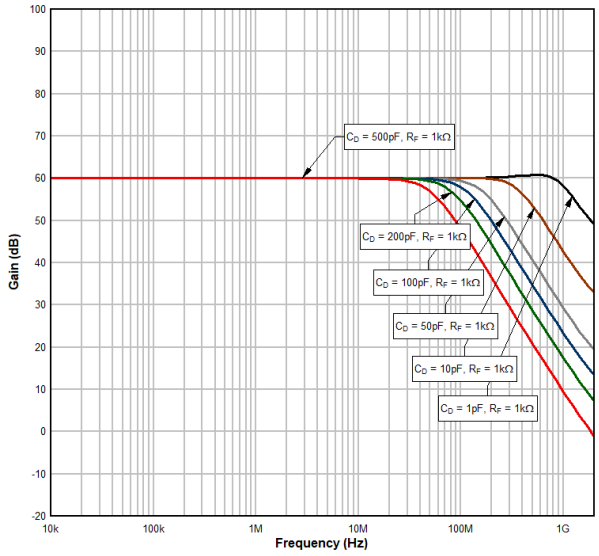


Figure 9-8. 1 Photodetector Input Characteristics TIA Frequency Response

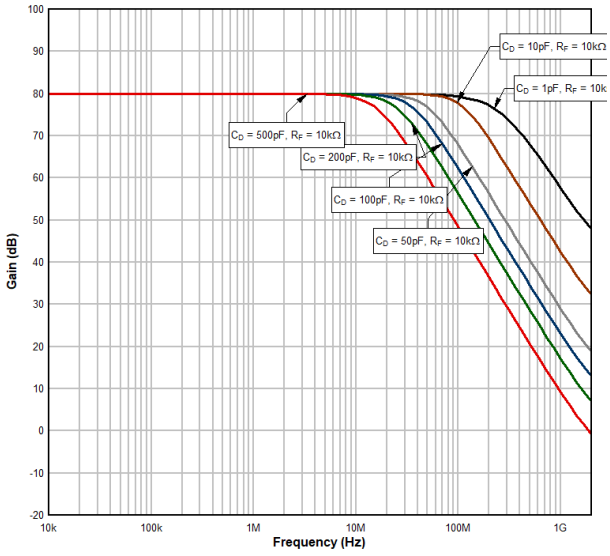


Figure 9-9. 2 Photodetector Input Characteristics TIA Frequency Response

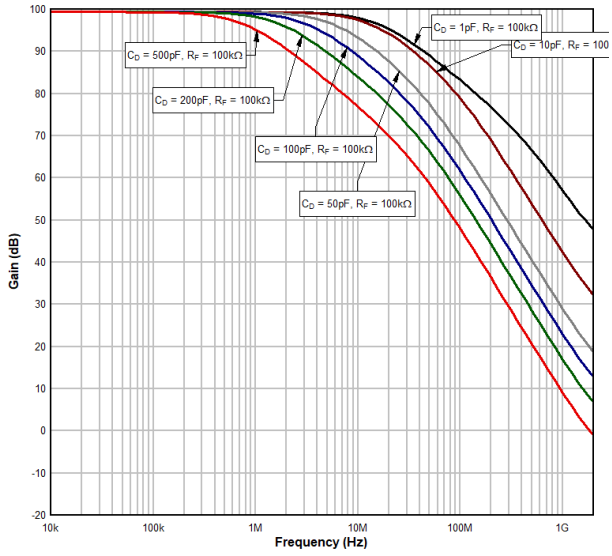
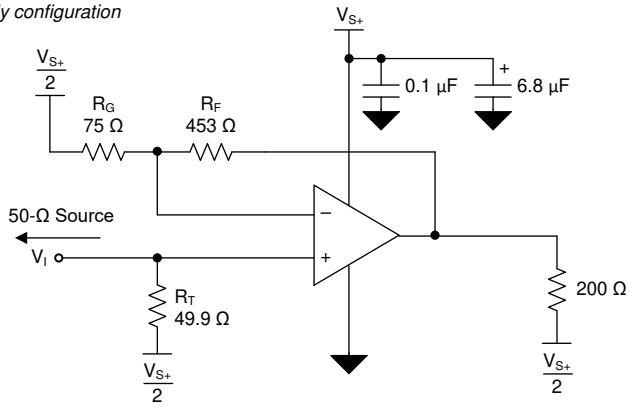


Figure 9-10. 3 Photodetector Input Characteristics TIA Frequency Response

9.3 Power Supply Recommendations

The OPA855 operates on supplies from 3.3 V to 5.25 V. The OPA855 operates on single-sided supplies, split and balanced bipolar supplies, and unbalanced bipolar supplies. Because the OPA855 does not feature rail-to-rail inputs or outputs, the input common-mode and output swing ranges are limited at 3.3-V supplies.

a) Single supply configuration



b) Split supply configuration

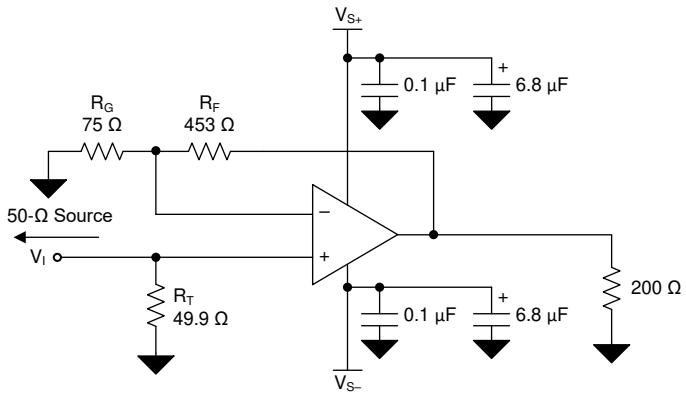


Figure 9-11. Split and Single Supply Circuit Configuration

9.4 Layout

9.4.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA855 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

- **Minimize parasitic capacitance from the signal I/O pins to ac ground.** Parasitic capacitance on the output and inverting input pins can cause instability. To reduce unwanted capacitance, cut out the power and ground traces under the signal input and output pins. Otherwise, ground and power planes must be unbroken elsewhere on the board. When configuring the amplifier as a TIA, if the required feedback capacitor is less than 0.15 pF, consider using two series resistors, each of half the value of a single resistor in the feedback loop to minimize the parasitic capacitance from the resistor.
- **Minimize the distance (less than 0.25-in) from the power-supply pins to high-frequency bypass capacitors.** Use high-quality, 100-pF to 0.1-µF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies. This configuration makes sure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors that are effective at lower frequency must be used on the supply pins. Place these decoupling capacitors further from the device. Share the decoupling capacitors among several devices in the same area of the printed circuit board (PCB).
- **Careful selection and placement of external components preserves the high-frequency performance of the OPA855.** Use low-reactance resistors. Surface-mount resistors work best and allow a tighter overall layout. Never use wire-wound resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close to the output pin as possible. Place other network components (such as noninverting input termination resistors) close to the package. Even with a low parasitic capacitance shunting the external resistors, high resistor values create significant time constants that can degrade performance. When configuring the OPA855 as a voltage amplifier, keep resistor values as low as possible and consistent with load driving considerations. Decreasing the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. However, lower resistor values increase the dynamic power consumption because R_F and R_G become part of the output load network of the amplifier.

9.4.2 Layout Example

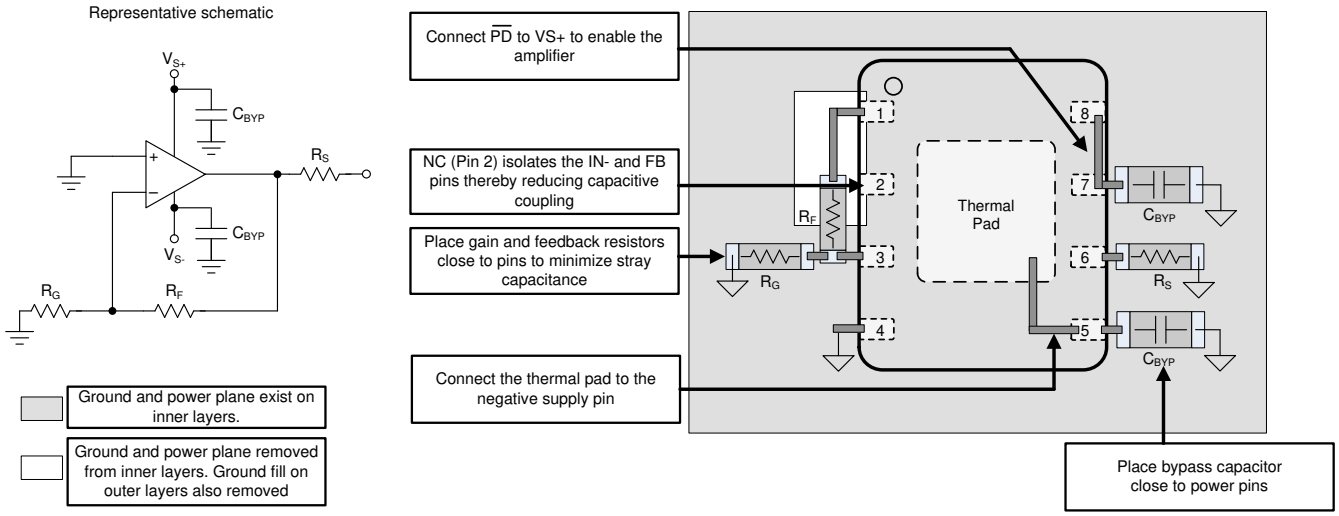


Figure 9-12. Layout Recommendation

When configuring the OPA855 as a transimpedance amplifier, take care to minimize the inductance between the avalanche photodiode (APD) and the amplifier. Always place the photodiode on the same side of the PCB as the amplifier. Placing the amplifier and the APD on opposite sides of the PCB increases the parasitic effects due to via inductance. APD packaging can be quite large, which often requires the APD to be placed further away from the amplifier than ideal. Figure 9-13 shows that the added distance between the two device results in increased inductance between the APD and op amp feedback network. The added inductance is detrimental to a decompensated amplifiers stability because this inductance isolates the APD capacitance from the noise-gain transfer function. The noise gain is given by Equation 3. The added PCB trace inductance between the feedback network increases the denominator in Equation 3 thereby reducing the noise gain and the phase margin. In cases where a leaded APD in a TO-can package is used, further minimize inductance by cutting the leads of the TO-can package as short as possible.

$$\text{Noise Gain} = \left(1 + \frac{Z_F}{Z_{IN}}\right) \tag{3}$$

where

- Z_F is the total impedance of the feedback network.
- Z_{IN} is the total impedance of the input network.

The layout shown in Figure 9-13 is improved by following some of the guidelines in Figure 9-14. The two key rules to follow are:

1. Add an isolation resistor R_{ISO} as close as possible to the inverting input of the amplifier. Select the value of R_{ISO} to be between 10 Ω and 20 Ω. The resistor dampens the potential resonance caused by the trace inductance and the amplifiers internal capacitance.
2. Close the loop between the feedback elements (R_F and C_F) and R_{ISO} as close to the APD pins as possible. This closure provides a more balanced layout and reduces the inductive isolation between the APD and the feedback network.

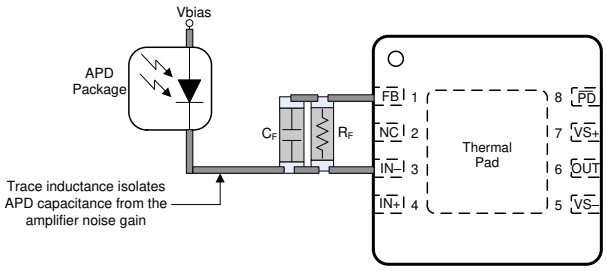


Figure 9-13. Non-Ideal TIA Layout

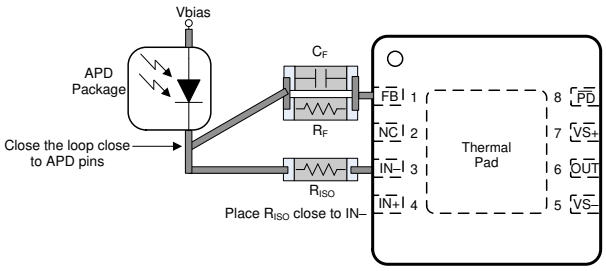


Figure 9-14. Improved TIA Layout

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

- *LIDAR Pulsed Time of Flight Reference Design*
- *LIDAR-Pulsed Time-of-Flight Reference Design Using High-Speed Data Converters*
- *Wide Bandwidth Optical Front-end Reference Design*

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *OPA855EVM user's guide*
- Texas Instruments, *Training Video: High-Speed Transimpedance Amplifier Design Flow*
- Texas Instruments, *Training Video: How to Design Transimpedance Amplifier Circuits*
- Texas Instruments, *Training Video: How to Convert a TINA-TI Model into a Generic SPICE Model*
- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers application report*
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 1*
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 2*

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2023) to Revision D (May 2025)	Page
• Changed bare die status from preview to production data (active)	1

Changes from Revision B (January 2022) to Revision C (January 2023)	Page
• Added the *Typical Application*, *Design Requirements*, *Detailed Design Procedure*, and *Application Curves* sections	23

Changes from Revision A (October 2018) to Revision B (January 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added bare die preview package to the *Features* section and *Device Information* table	1
• Added the *bare die preview package* to the *Pin Configuration and Functions* section	3

Changes from Revision * (July 2018) to Revision A (October 2018)	Page
• Changed from Advance Information to Production Data (active)	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA855IDSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	855
OPA855IDSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	855
OPA855IDSGRG4.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	855
OPA855IDSGT	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	855
OPA855IDSGT.B	Active	Production	WSON (DSG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	855
OPA855YR	Active	Production	DIESALE (Y) | 0	3000 | LARGE T&R	Yes	Call TI	N/A for Pkg Type	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF OPA855 :

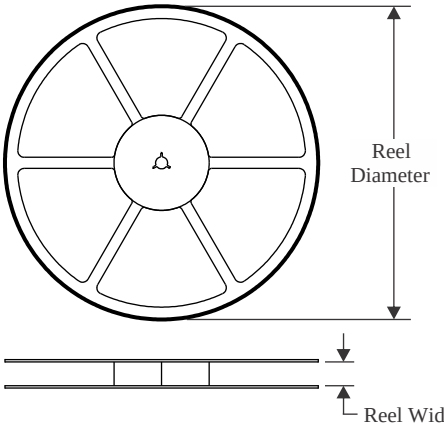
- Automotive : OPA855-Q1

NOTE: Qualified Version Definitions:

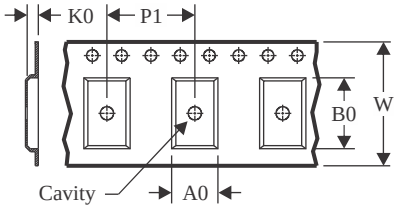
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

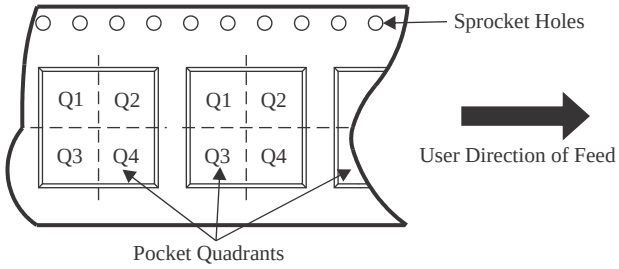


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

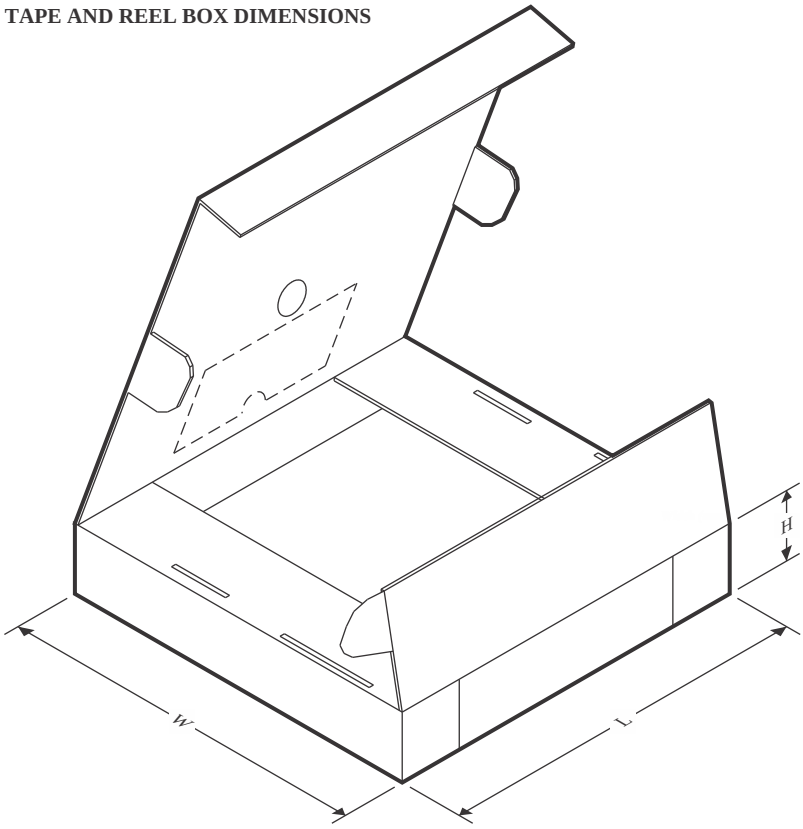
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA855IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA855IDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA855YR	DIESALE	Y	0	3000	180.0	8.4	0.74	0.78	0.45	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA855IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
OPA855IDSGT	WSON	DSG	8	250	210.0	185.0	35.0
OPA855YR	DIESALE	Y	0	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

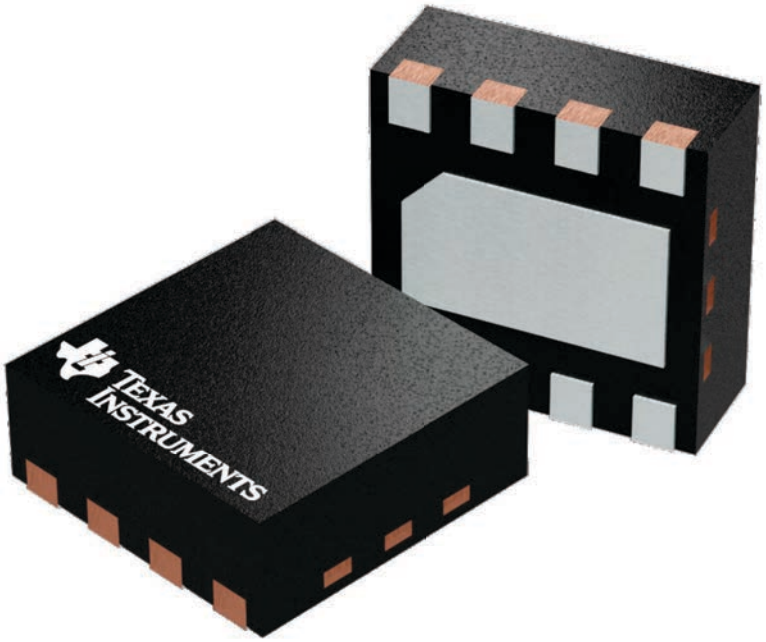
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



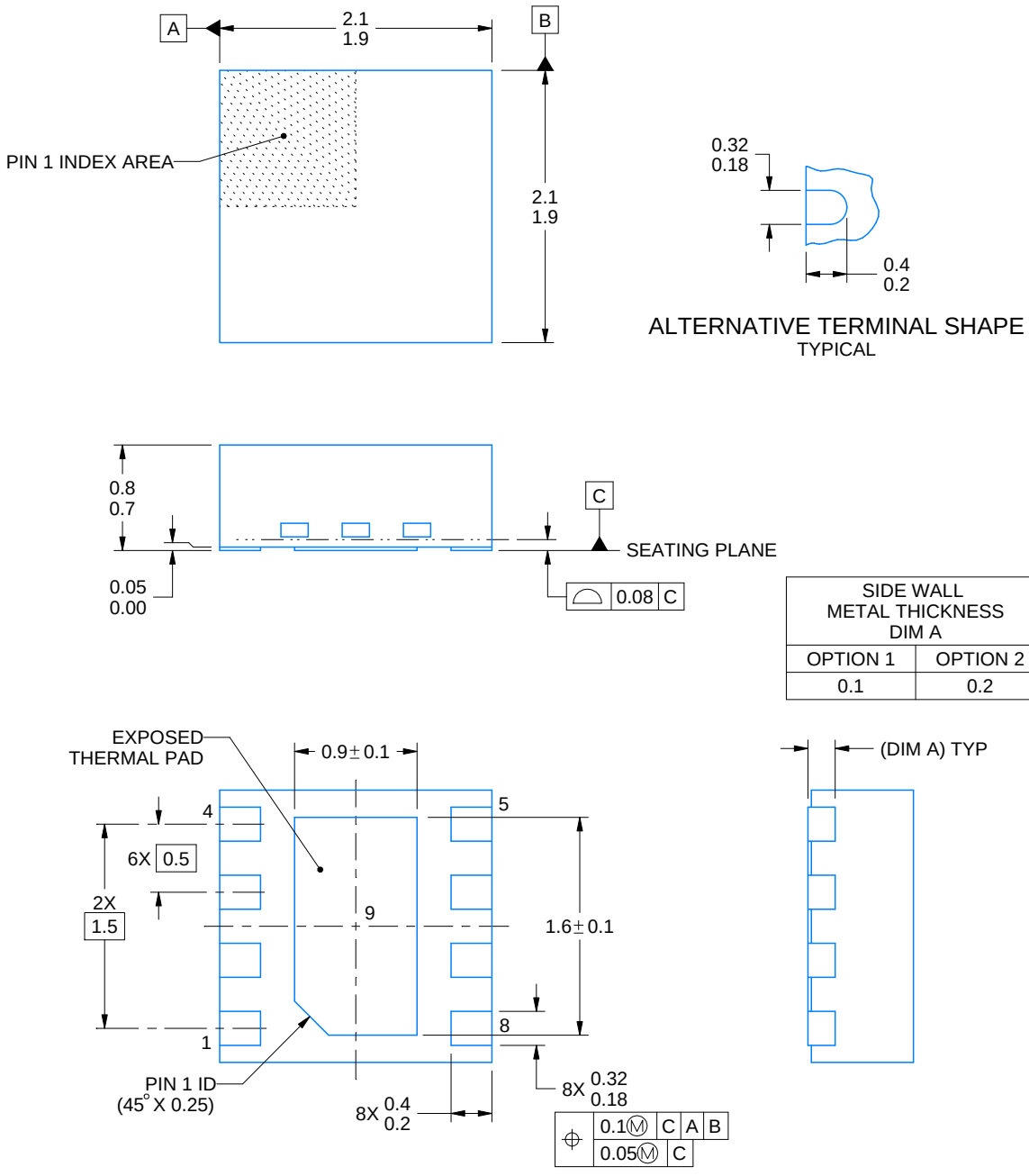
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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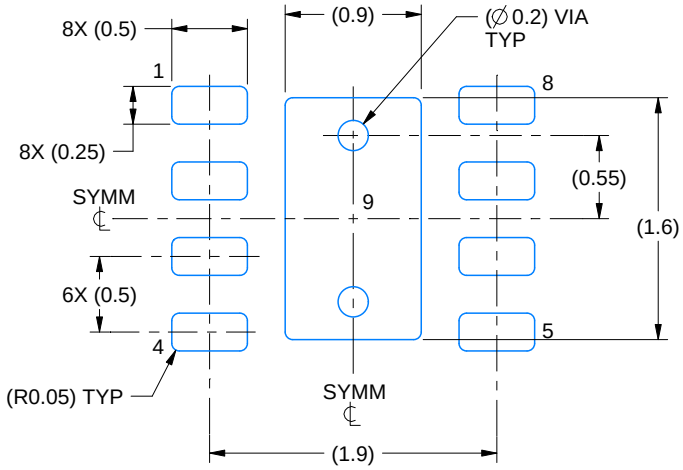
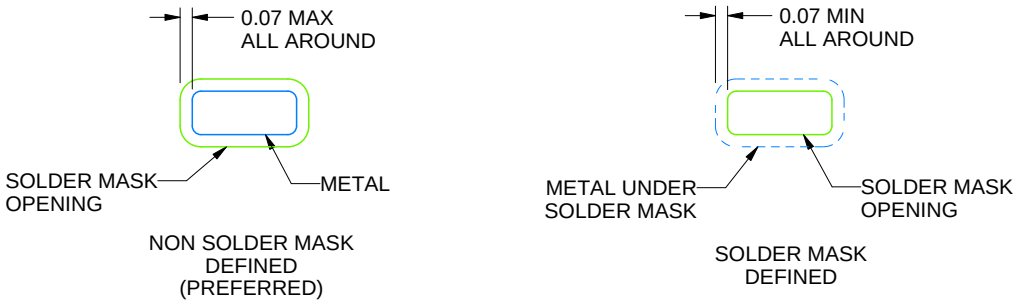
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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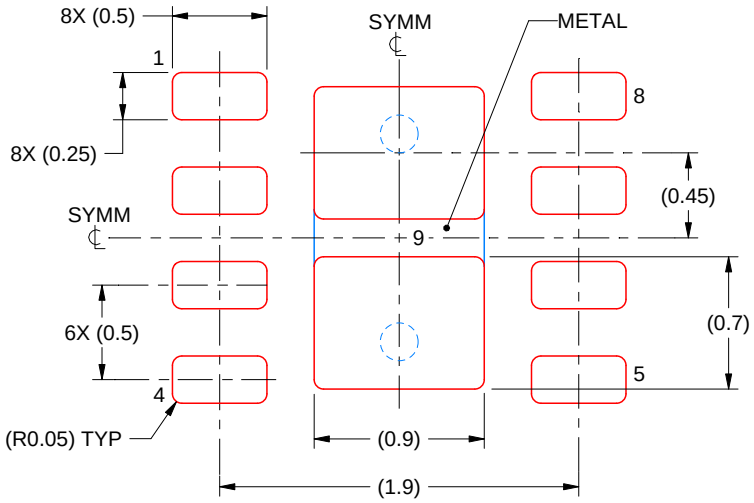
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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