Analog Engineer's Circuit

Circuit Replacing HART® Modem Device Competitors With the DAC8740H

Precision DAC: Factory Automation and Control *Joseph Wu*

Design Objective

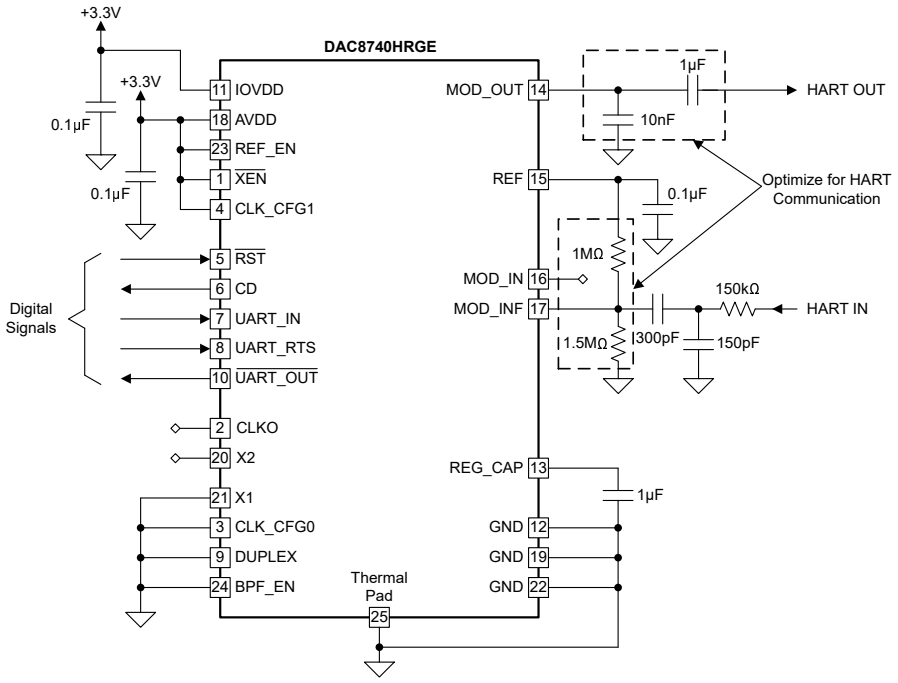
Supply Voltage	HART® Signal Input Voltage	HART® Signal Output Voltage	Recommended Device
3.3V	120mV$_{PP}$–1.5V$_{PP}$ (500mV$_{PP}$ nominal)	460mV$_{PP}$ nominal	DAC8740H

Objective

Use the DAC8740H Highway Addressable Remote Transducer (HART®) modem as a replacement for competitor modem devices.

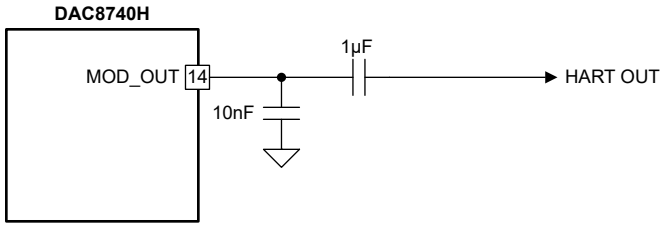
Design Description

Selection of the components around the DAC8740H is very important when using the device as a replacement for similar competitor HART modems. Even if the competitor HART modem is pin-to-pin compatible with the DAC8740H, changes are required to the resistors and capacitors around the modem to pass certain HART tests. This analog engineer's circuit note describes the circuit changes needed to set up the DAC8740H to pass important HART physical layer tests. The DAC8740H is the modem in this circuit for HART-enabled devices like field transmitters and programmable logic controllers (PLCs).



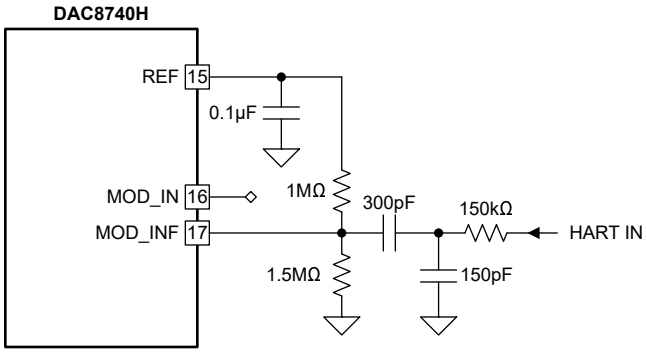
Design Notes

1. Decoupling capacitors are needed on the supply pins, reference, and the internal LDO used for the DAC8740H. The AVDD and IOVDD pins use a minimum capacitance of 0.1µF per pin. The internal reference requires a 0.1µF at the REF pin and the internal LDO requires a 1µF capacitor at REG_CAP.
2. In this circuit, the internal oscillator sets the timing of the device. If a crystal oscillator is used, check the *DAC874xH HART® and FOUNDATION™ Fieldbus and PROFIBUS® PA Modems* datasheet for device settings and circuit changes.
3. The internal reference voltage is 1.5V at the REF pin and is enabled by the REF_EN pin tied high.
4. The DAC8740H HART modulator output signal path is shown in the following figure.

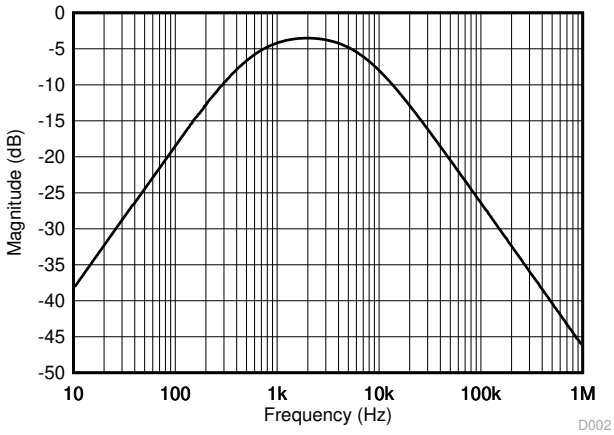


5. The DAC8740H datasheet shows a HART output parallel capacitor of 22nF. Consider this value to be the high end of the range and 10nF is a preferred value. For the pass-through capacitance for the HART signal, the datasheet shows a 4700pF capacitor. Consider this value to be the lower bound of the capacitance. A value of 1µF or greater can be used as the output to insert the HART signal into the loop.
6. When using an external filter for receiving the HART signal, a band-pass filter constructed from passive devices is placed from the HART input to the MOD_INF pin. The band-pass filter is shown in the figure below. Use X7R or NP0 capacitors, as the tolerance, drift, and voltage coefficient change the frequency response of the filter.

   The DAC8740H MOD_INF input is set to a different dc level than other competitor devices. Here, the voltage divider is constructed with a different resistor ratio from the REF pin using 1MΩ and 1.5MΩ.



The frequency response of this HART mode external band-pass filter is shown in the following figure.



7. If the voltage divider ratio of the external band-pass filter is not changed (as described in 6), the signal can still be correctly received. However, the HART communication likely fails in the presence of noise.

   For physical layer tests, HART devices must pass noise sensitivity level tests. In these tests, sinusoidal interference noise is generated at different frequencies and amplitudes. The HART device must simultaneously reject the sinusoidal noise and detect and decode the HART transmission sent with a frequency shift keyed (FSK) sinusoidal signal. The following table describes the different interference noise that the HART device must reject.

HART® Noise Sensitivity Level Tests

Interference Amplitude Specification	Waveshape	Frequency (Hz)	HART® Signal Amplitude (mV_{PP})
$55mV_{PP}$	Sinusoidal	1700	175
$220mV_{PP}$	Sinusoidal	250	175
$880mV_{PP}$	Sinusoidal	125	175
$3.52V_{PP}$	Sinusoidal	63	175
$16V_{PP}$	Sinusoidal	29	175

   Based on previous testing, the low-frequency, higher-voltage interference signals are more likely to fail if the resistance divider is not set to the recommended values (1MΩ and 1.5MΩ). The noise signals for $880mV_{PP}$ at 125Hz, $3.52V_{PP}$ at 63Hz, and the $16V_{PP}$ at 29Hz likely interfere with the HART transmission.

8. After the HART modem is replaced with the DAC8740H, run the full set of HART tests. These tests include the FSK physical layer tests which cover the waveform characteristics, signal integrity and amplitude, carrier detection, device input and output impedance, and performance in the presence of noise. Other HART tests include the data link layer tests (DLL), the universal command tests (UAL), and the common practice command tests (CAL). These tests verify the protocol timing, communication signaling, and check the application layer command responses.

HART® Timing

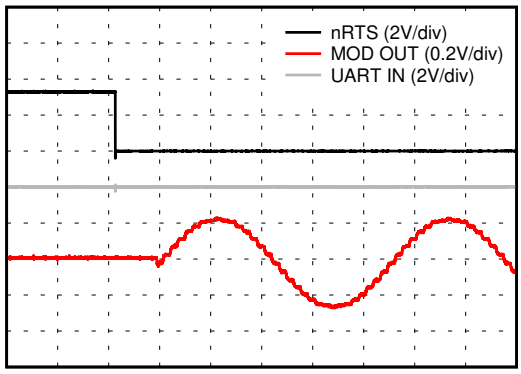
Even with the previously described schematic changes, there can still be timing differences that disrupt operation. Check the HART Mode Timing from the DAC8740H in the following table.

HART® Timing Mode

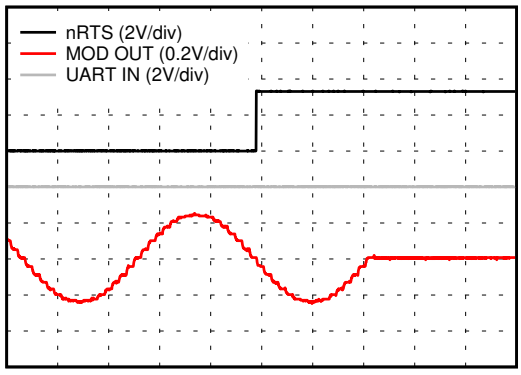
Parameter	Description	Minimum	Maximum	Units
t_{cstart}	Carrier start time. Time from $\overline{RTS}$ falling edge to transmit carrier reaching the first peak.		5	bit times
t_{cstop}	Carrier stop time. Time from $\overline{RTS}$ rising edge to transmit carrier amplitude falling below the receive amplitude.		3	bit times
t_{cdecay}	Carrier decay time. Time from $\overline{RTS}$ riding edge to carrier amplitude dropping to zero.		6	bit times
t_{cdeton}	Carrier detect on. Time from valid carrier on receive path to CD rising edge.		6	bit times
$t_{cdetoff1}$	Carrier detect off. Time from valid carrier removed on receive path to CD falling edge.		3	ms
$t_{cdetoff2}$	Carrier detect on when transitioning from transmit mode to receive mode in the presence of a constant valid receive carrier.	2.1		ms

The timing for the HART signal is described in either bit times or milliseconds. For the HART signal, the transmission is 1200 baud. This means that each bit time is 833µs. The timing from the table describes the maximum times for the DAC8740H to start or stop a transmission or the maximum times for the device to start or stop detecting a carrier HART signal from another device.

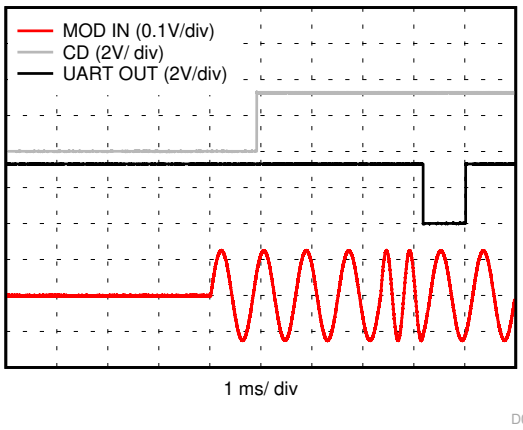
The following oscilloscope plots show the HART timing parameters described in the previous table. First, the DAC8740H starts a transmission using the request-to-send ($\overline{RTS}$) signal. When the $\overline{RTS}$ signal goes low, the HART sinusoid appears at the MOD_OUT pin. The following oscilloscope plots show a start and stop of the transmission timing based on the input of $\overline{RTS}$. The first plot shows a typical carrier start time (t_{cstart}) for the MOD_OUT based on $\overline{RTS}$ transition low.



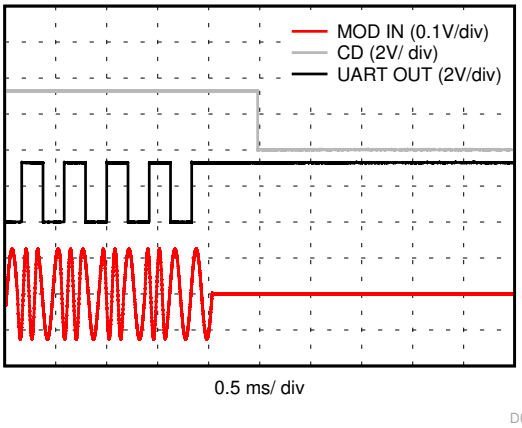
The carrier stop time (t_{cstop}) is the time taken for the transmitted signal to drop below the minimum receivable HART signal level of 80mV$_{PP}$. Similarly, the carrier decay time (t_{cdecay}) is the time taken for the HART signal to drop from the minimum receivable HART signal level to the maximum noise amplitude of 6.16mV$_{PP}$. The second shot shows the time for both based on the $\overline{RTS}$ rising to the MOD_OUT completion. While the plot does not specifically show the exact timing, the plot shows that the device is within the specification.



The DAC8740H uses a carrier detect (CD) signal to show that a HART signal is detected at the MOD_INF (or MOD_IN if the internal filter is used). The following oscilloscope plots show a typical CD start and stop of the transmission timing based on the signal at MOD_INF or MOD_IN. The first plot shows the typical carrier detect on (t_{cdeton}) time where CD rises when the HART signal is detected.



This final plot shows the carrier detect off ($t_{cdetoff1}$), where the CD falls as the HART signal completion stops the DAC8740H carrier detection.



The last row of the HART Timing Mode table is the carrier detect on timing ($t_{cdetoff2}$) when transitioning from transmit mode to receive mode. Use this minimum time after the $\overline{RTS}$ completes to detect for a HART signal from another transmitter.

In most cases, using the DAC8740H as a replacement for competitor devices does not require any changes to the stack timing. However, if there are problems with testing, the timing differences can be reviewed.

Device Compatibility

The DAC8740H device is designed to couple in the signal at MOD_OUT in different HART transmitter products. Devices like the DAC8760, DAC7760, DAC8771, DAC8775, DAC161S997, and DAC161P997 all have dedicated HART input pins that can couple in a HART signal to the DAC output. To couple in a HART signal to the output of any of the previously listed DACs, review the datasheets of the respective devices.

Additionally, a loop-powered 4-20mA field transmitter can be made HART-enabled with the DAC8740H even if the DAC does not have a dedicated HART input pin. The DAC8830 is shown with the DAC8740H as part of a HART-enabled transmitter in *Highly Accurate, Loop-Powered, 4- to 20-mA Field Transmitter With HART Modem Reference Design*. This topology can be used to create a loop transmitter with HART signaling from any generic voltage output DAC.

For more information about the HART protocol, see *A Basic Guide to the HART Protocol*. Information about HART-compatible DAC devices and HART protocol testing is also found in the following documentation:

- *HART-Enabled PLC Analog Input Module Reference Design*
- *Design and Test of a HART-Enabled Field Transmitter for 4-20mA Loops*
- *HART-Enabled Transmitter Based on an Evaluation Module Design*

Design Featured Devices

Find other possible DAC devices using the parametric search tool.

Device	Key Features	Link
DAC8740H, DAC8741H	DAC874xH HART® and FOUNDATION™ Fieldbus and PROFIBUS® PA Modems	DAC8740H
DAC8742H	DAC8742H, HART and FOUNDATION Fieldbus / PROFIBUS PA Modem	DAC8742H
DAC8760, DAC7760	DACx760 Single-Channel, 12- and 16-Bit Programmable Current and Voltage Output Digital-to-Analog Converters for 4-mA to 20-mA Current-Loop Applications	DAC8760
DAC8750, DAC7750	DACx750 Single-Channel, 12-Bit and 16-Bit Programmable Current Output Digital-to-Analog Converters for 4-mA to 20-mA Current-Loop Applications	DAC8750
DAC8775	DAC8775 Quad-Channel, 16-Bit Programmable Current Output and Voltage Output Digital-to-Analog Converter with Adaptive Power Management	DAC8775
DAC8771	DAC8771 Single-Channel,16-Bit Voltage and Current Output Digital-to-Analog Converter with Adaptive Power Management	DAC8771
DAC8830	DAC8830 16-bit, single-channel, ultra-low power, voltage output DAC	DAC8830
DAC161S997	DAC161S997 16-Bit SPI-Programmable DAC for 4-20 mA Loops	DAC161S997
DAC161P997	DAC161P997 Single-Wire 16-bit DAC for 4- to 20-mA Loops	DAC161P997

Design References

See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, *A Basic Guide to the HART Protocol Application Note*
- Texas Instruments, *Design and Test of a HART-Enabled Field Transmitter for 4-20mA Loops Application Note*
- Texas Instruments, *HART-Enabled Transmitter Based on an Evaluation Module Design Application Note*
- Texas Instruments, *Highly-Accurate, Loop-Powered, 4mA to 20mA Field Transmitter With HART Modem Reference Design*
- Texas Instruments, *HART-Enabled PLC Analog Input Module Reference Design*
- Texas Instruments, *TI Precision Labs - DACs*

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