Technical White Paper

Op Amp Input and Output Swing Limitations

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ABSTRACT

Exceeding the input or output swing limitations on amplifiers causes distortion on the output signal. This document initially covers the basic methods for calculating these limitations. Next, a simplified explanation of how the limitation occurs on internal transistor topology is covered. The internal operation is described to provide insight to the board-and-system level designer on how different categories of amplifiers behave. For example, the operation of two different types of rail-to-rail common-mode range are compared and contrasted. Each of these topologies has specific advantages and disadvantages related to noise and distortion. Finally, the impact of output current on swing limitations, short-circuit protection, and other topics related to the op amp input and output stage are covered.

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1 Introduction

The practical output voltage range of an op-amp circuit is limited by the power supply voltage, internal op-amp design, and circuit configuration. The output range is always less than the power supply range. Thus, for a ±15-V supply, the output range can be at most ±15 V. From a practical perspective some amplifiers can get very close to the supply limits, but no amplifier actually achieves output swing all the way to the supply voltage. A CMOS rail-to-rail amplifier, for example, can have an output swing a few millivolts from the power supply rail.

There are two amplifier specifications that determine the output voltage range: common-mode range, and output swing from the supply rail. The common-mode range is the range of linear operation of the amplifier versus the input common-mode signal. The input common-mode signal is defined as the average voltage applied to the input of the op amp. However, since the op amp has a virtual short between the two inputs, the voltage is approximately the same on either input. Thus, under normal linear operating conditions, any voltage measured on either input is the common-mode voltage. The common-mode range provides the range of linear operation of the amplifier input stage relative to the power supplies. The output swing range is the range of linear operation for an amplifier output stage relative to the power supply voltage and the load current.

The common mode and output swing specification in Table 1-1 can be used to determine the input and output range of the amplifier. Use the minimum and maximum limits from the specification table with the power supply voltages to determine the input and output range for the amplifier. The *OPAx206 Input-Overvoltage-Protected, 4-µV, 0.08-µV/°C, Low-Power Super Beta, e-trim™ Op Amps* data sheet provides two different specification tables: one at ±5 V and one at ±15 V. Since the actual circuit is between these limits, the worst case is selected. Figure 1-1 provides an example illustrating how the data sheet specification can be applied to a specific power supply configuration to determine the input and output limitations. In this example the minimum common-mode limit can be determined by using the negative supply and minimum limit from the specification table (that is, (V–) + 1 = (–5 V) + 1 V = –4 V). The maximum can similarly be determined using the 12-V supply and the table maximum limit (that is, (V+) – 1.4 V = 12 V – 1.4 V = 10.6 V). The same approach can be used to calculate the output swing limitation. However, in this case the load must be accounted for. In this example, the load is 10 kΩ, so the output swing is limited by 0.2 V from either supply rail (–4.8 V < V_{OUT} < 11.8 V). It is also important to realize that this output limitation is the point that the amplifier is completely nonlinear and the output is saturated. As you approach the saturation limit, the amplifier output becomes distorted. Section 9 covers details explaining the difference between the saturation and linear limit for the amplifier. The common mode and output swing examples use an asymmetrical power supply arrangement of V_{CC} = +12 V and V_{EE} = –5 V. In practical circuits the supplies are more commonly balanced but can be asymmetrical as shown in the example. The example uses different values for V_{CC} and V_{EE} for instructive purposes to help identify and differentiate between the two supplies.

Table 1-1. OPA206 Common Mode and Output Swing Specifications

Parameter: OPA206		Conditions	Min	Typ	Max	Unit
V_{CM}	Common-Mode Voltage Range		(V–) + 1		(V+) – 1.4	V
V_{OUT}	Voltage Output	R_L = 10 kΩ, V_S = ±15 V	(V–) + 0.2		(V+) – 0.2	V
		R_L = 2 kΩ, V_S = ± 15 V	(V–) + 0.35		(V+) – 0.35	V

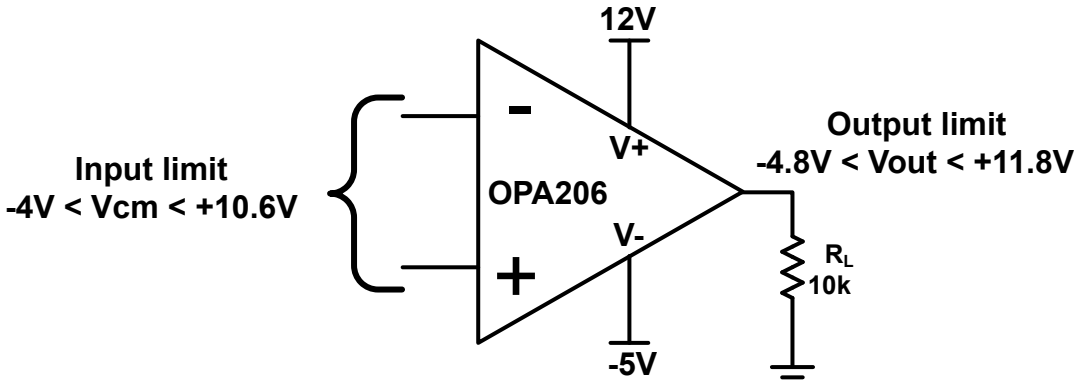

Figure 1-1. OPA206 Example Common Mode and Output Swing Limits

2 Circuit Configuration Impact on Common-Mode Range

The *Introduction* showed how the common-mode limitation of the amplifier can be calculated given the supply voltages and the data sheet specification table. The amplifier circuit configuration often determines if this limitation causes nonlinear operation. The voltage follower is the configuration that is most likely to be impacted by common-mode limitations. This is because the common-mode voltage is the same as the input signal and the input signal often covers the entire supply range. Figure 2-1 provides a DC input sweep to illustrate the common-mode limitation of the OPA206 in a buffer configuration. Note that the input voltage is equal to the common-mode signal in this configuration, so the linear range is –4 V to 10.6 V as calculated in Figure 1-1.

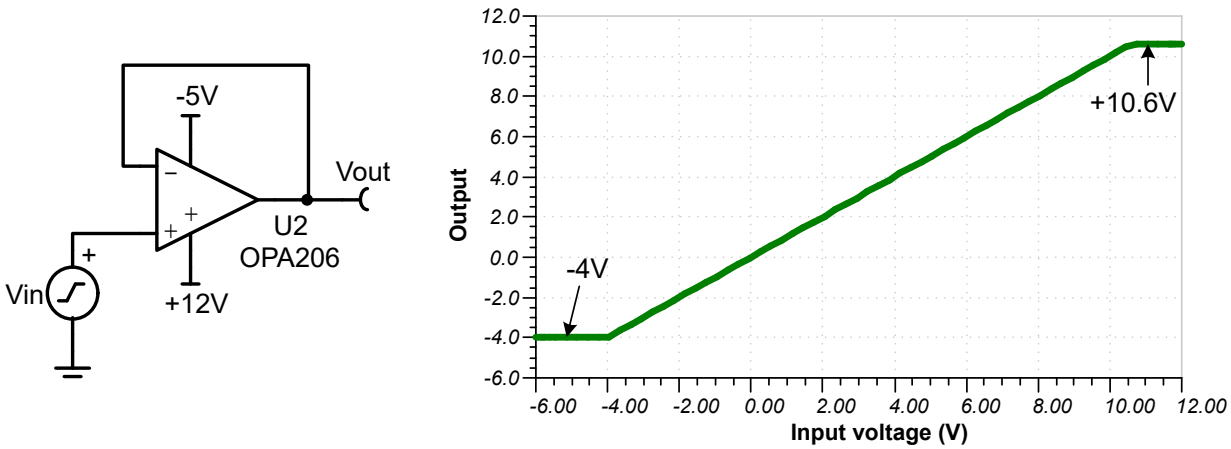

Figure 2-1. Common-Mode Limit of OPA206 in Buffer Configuration

The same op amp in a gain configuration is not impacted by the common-mode limitations because the valid input signal range for the gain configuration is small and does not approach the common-mode limits. For example, in a gain of 10 V/V, the input range is ten times smaller than the output range. Figure 2-2 shows the same supply arrangement in a gain of 10 V/V. In this case, the best output range is –5 V to +12 V, so the valid input range is –0.5 V to 1.2 V. Since the common-mode range for this device is –4.0 V to +10.6 V, the valid input signal is never near the common-mode limits. For this example, notice that the output signal does not swing all the way to the supply limits. This limitation is because of the output swing limitations, and not the common-mode limits and are covered in detail later in this white paper.

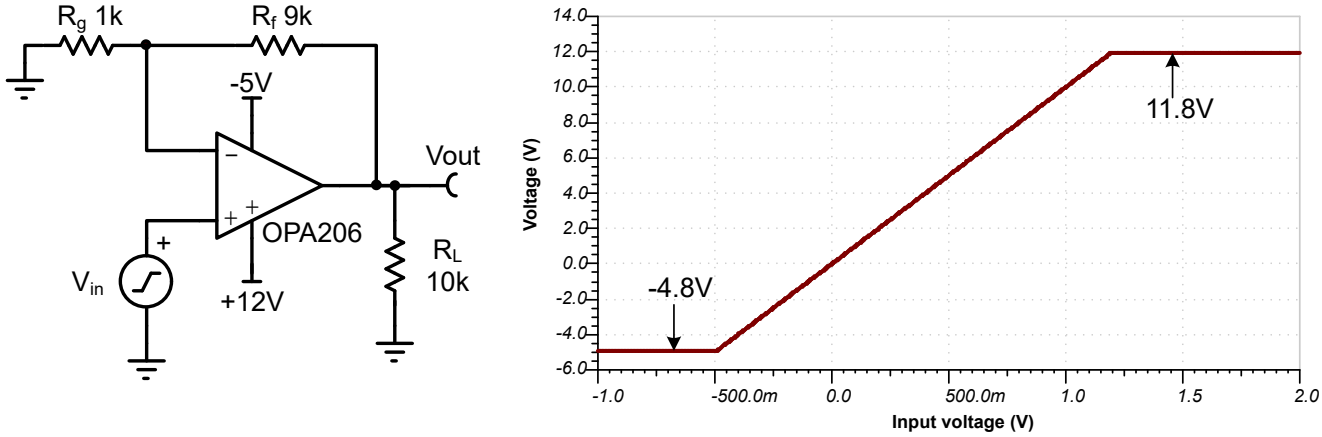

Figure 2-2. Common Mode Does not Limit OPA206 in Non-inverting Gain of 10 V/V

In the non-inverting configuration, the common-mode voltage is equal to the input signal. For the inverting configuration the common-mode voltage is equal to the voltage applied to the non-inverting input. In general, for inverting amplifiers the non-inverting input is connected to ground or a fixed DC voltage. For inverting amplifiers, the common-mode voltage remains constant regardless of the input signal, so these types of amplifiers generally do not have common-mode issues. The example shown in Figure 2-3 shows that the common-mode signal is held constant at ground, and the amplifier does not experience common-mode limitations. This amplifier has a gain of –1 V/V, so you can substitute this configuration for a buffer configuration if common-mode limitation is a problem for the buffer. However, remember that the inverting amplifier configuration has gain error and drift due to the tolerance of the feedback resistors, whereas the buffer has a very accurate gain of 1 V/V. Furthermore, the resistors add noise and additional power consumption for the amplifier.

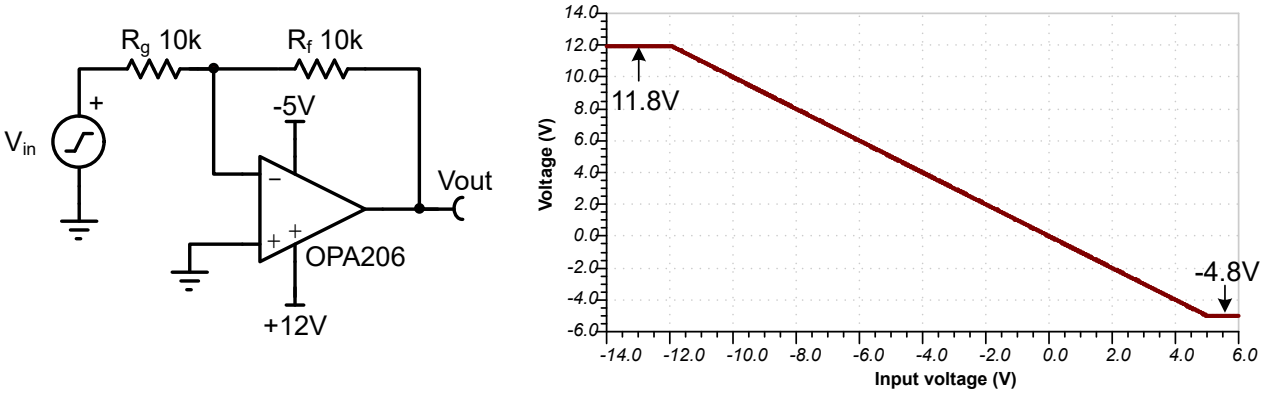

Figure 2-3. Common Mode Does not Limit OPA206 in Inverting Gain Configuration

3 Practical Input Limitations

Section 2 demonstrated the common-mode limitations for different configurations by running a DC sweep. The simulation indicated that the common-mode range was violated by clamping the output signal. Furthermore, the limit always occurred at the minimum and maximum limit of the common-mode range. First, understand that the common-mode range given is the worst-case range, so when measuring actual devices, the performance is often better than the specification. Nevertheless, when designing a system, assume that the worst-case specification is a possibility due to process variation. Never base a system design on lab measurement of a few units. Always design considering the published minimum and maximum data sheet specifications.

The common-mode limitation also does not necessarily clamp the output as is generally shown in simulation models. A real-world device can introduce substantial distortion when the input range is violated rather than clamp the output. Furthermore, this effect can be dependent on other factors such as input frequency, or temperature. Figure 3-1 illustrates a case where the amplifier common-mode range limitation is dependent on frequency. The data sheet specification for this device provides the worst-case common-mode range across the entire bandwidth of the device. Lab measurements at low frequency indicate that the device has common-mode range much wider than the specification, whereas the measurements at higher frequency show substantial distortion where the signal exceeds the common-mode limit. Notice that even the higher frequency case does not clamp at the common-mode limitation, but rather introduces unacceptable distortion.

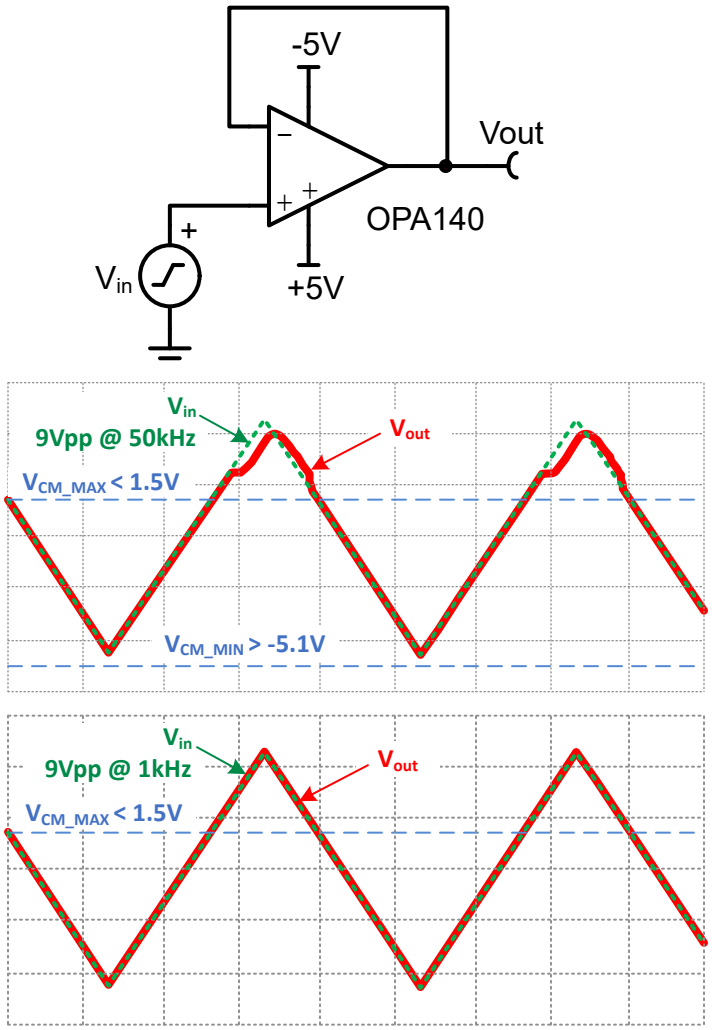

Figure 3-1. Measured Common-Mode Limitation on OPA140 versus Frequency

4 Input Phase Reversal (Inversion)

Normally when an op-amp input is driven beyond the common-mode range, the output becomes distorted or clipped. During the early years of op-amp semiconductor development some amplifiers exhibited a different phenomenon when the common-mode range was exceeded, called phase reversal. When the common-mode range is exceeded for a device with phase reversal, the output actually moves in the opposite of the expected direction. Figure 4-1 illustrates this issue on a buffer amplifier. Notice that when the input moves positively beyond the common-mode range the output actually moves negatively. This problem is related to a design oversight, and all modern amplifiers are designed and tested so that this issue is no longer a problem. Even legacy devices that once had phase reversal, have generally been revised to correct this issue. This section is included in the document to alleviate concerns related to legacy literature. Most modern data sheets include a line item indicating no phase reversal.

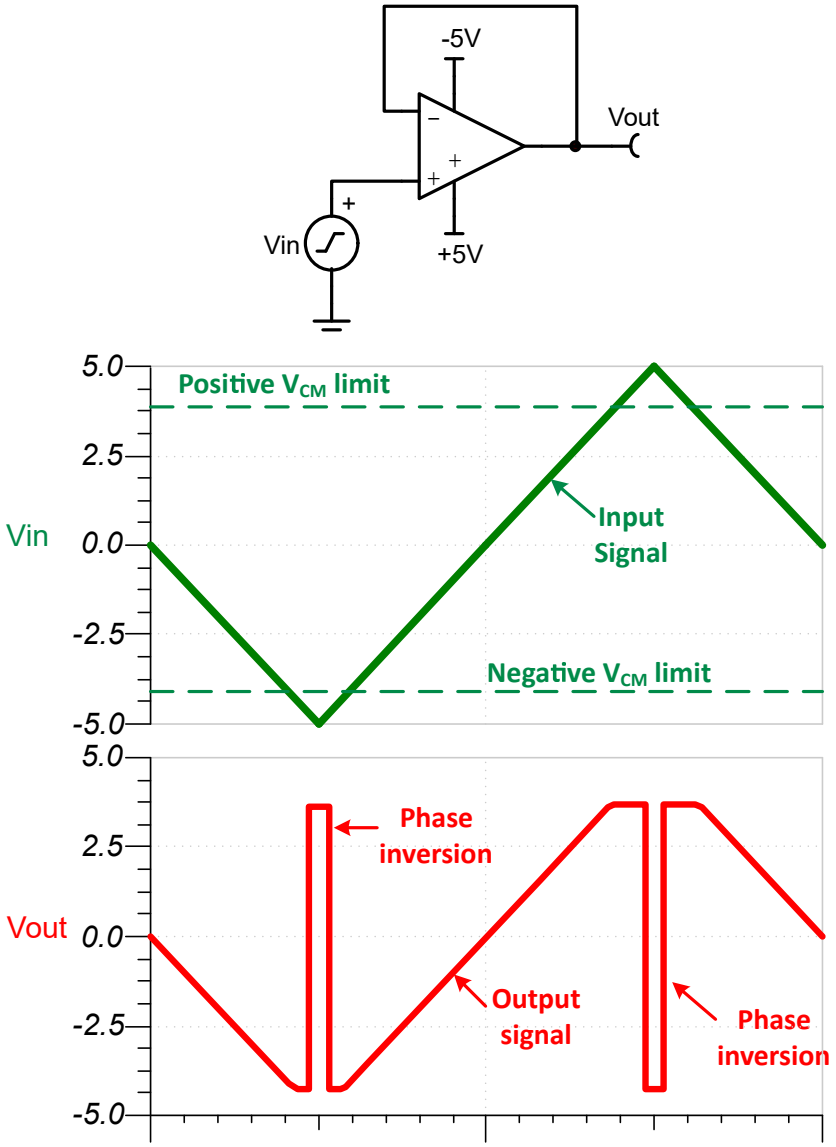

Figure 4-1. Phase Inversion (Reversal)

5 Common-Mode Limitations Inside Bipolar Amplifiers

This section covers some of the details regarding the internal operation of the op amp. It is not necessary to have a deep understanding of the internal operation to design effective board-level amplifier circuits. However, developing a rudimentary understanding of the internal operation helps to provide a better insight into device selection, operation, and trade-offs for different technologies. This section provides some high-level details on internal operation, but for a complete coverage, consult integrated circuit design textbooks such as *Analysis and Design of Integrated Circuits by Gray and Meyer* [(2)].

From a common-mode perspective, CMOS and bipolar have different characteristics and need to be considered separately. A simplified version of a typical bipolar input stage is shown in Figure 5-1. The transistors Q1 and Q2 translate a differential input voltage to a single-ended output for the next stage. Transistor Q4 sets the bias current for the differential pair. The positive common-mode limitation of the input stage occurs when Q4 becomes saturated. For a bipolar transistor, saturation occurs at maximum collector current and minimum collector-to-emitter voltage ($V_{CE(SAT)}$ = 0.2 V to 0.3 V). The positive common-mode range can be calculated doing a Kirchhoff's walk from the input to ground. For this example, $V_{IN\_MAX} = -V_{BE(Q1)} - V_{CE(Q4\text{-}SAT)} + V_{CC}$. For a 0.7-V V_{BE} drop and a saturation voltage of 0.3 V the common-mode limit is approximately 1 V from V_{CC}. If the common-mode input signal is equal to or greater than the common-mode limit, the transistor Q4 saturates and the amplifier becomes non-linear.

Figure 5-2 illustrates the negative common-mode limitation on a bipolar input stage. The negative supply becomes nonlinear when the input signal is driven near V_{EE} so that Q1 becomes saturated. Doing a Kirchhoff's walk from V_{EE} to the input shows that $V_{IN\_MIN} = V_{EE} + V_{D1} + V_{CE(SAT\text{-}Q1)} - V_{BE(Q1)}$, or $V_{IN\_MIN} = V_{EE}$ + 0.3 V.

It is evident from the bipolar common-mode examples that the input common-mode range is limited by 0.3 V from the negative rail and 1 V from the positive rail. Depending on the internal topology, the common-mode range can have even greater swing limitations. Some relatively unusual bipolar devices can have swing to V_{EE}, but no bipolar has rail-to-rail input. If a wide common-mode range is required, CMOS rail-to-rail devices offer input swing from the negative to positive input supply (see Section 7).

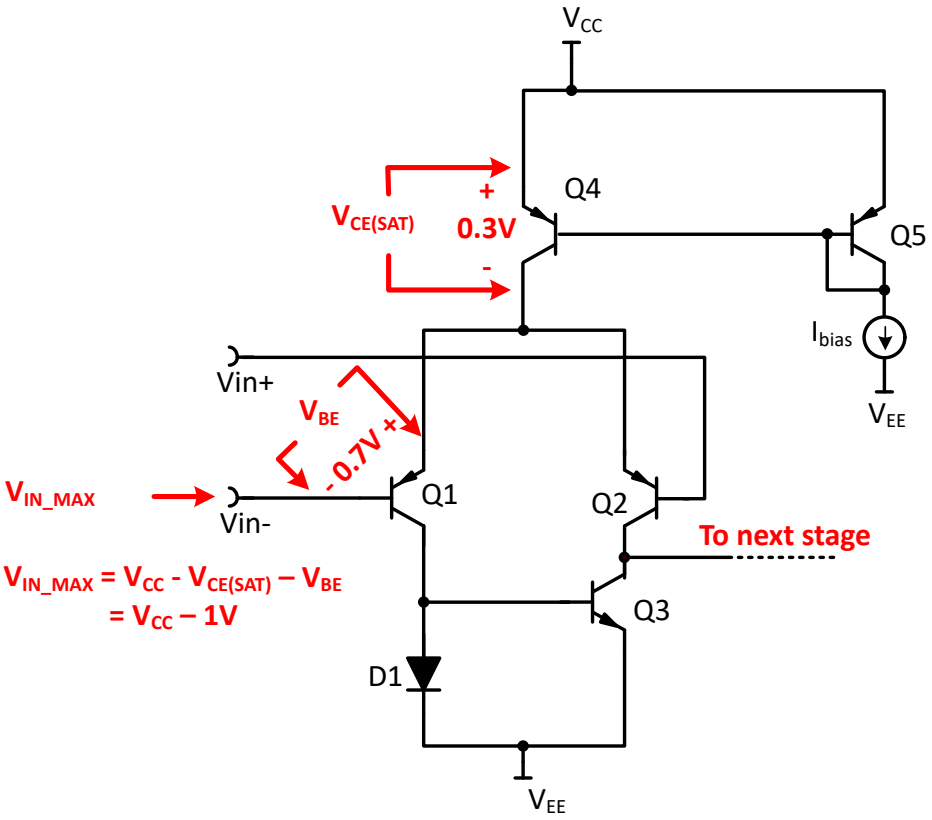

Figure 5-1. Bipolar Input Stage Positive Common-Mode Limit

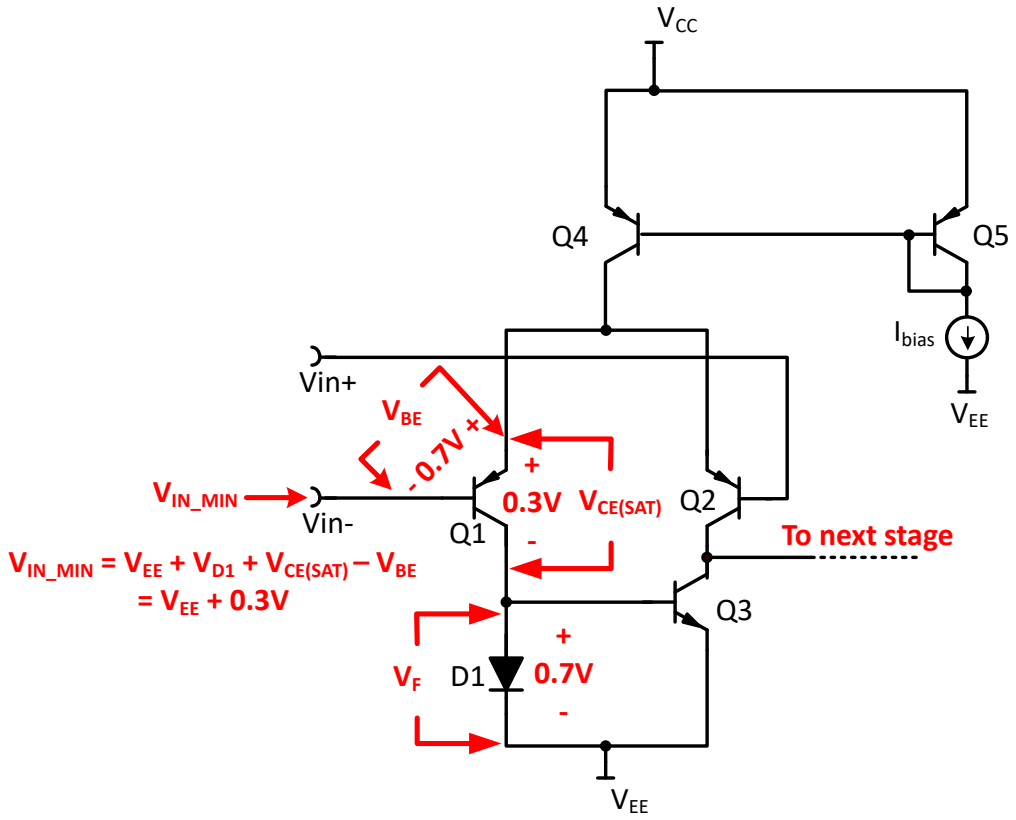

Figure 5-2. Bipolar Input Stage Negative Common-Mode Limit

6 Common-Mode Limitations Inside CMOS Amplifiers

From a high level, the internal biasing of CMOS input stages looks similar to the bipolar device, but these devices are voltage controlled rather than current controlled. Depending on whether a P-channel, or N-channel device is used, the gate-to-source voltage required to bias the device generally allows for linear operation to either the negative or positive power-supply rail. Figure 6-1, Figure 6-2, and Figure 6-3 illustrate the P-channel case where the input operates linearly with input signals to the negative supply rail, but has common-mode limitations as the positive rail is approached.

Figure 6-1 illustrates the characteristic curve for the input P-channel devices. For linear operation the input transistors need to operate on the flat part of the curve where gate-to-source voltage is –0.9 V. Figure 6-2 illustrates the swing to the negative rail. The drops shown in this schematic illustrate the minimum voltages required for linear operation. Doing a Kirchhoff's walk to the negative supply, shows that the minimum voltage for linear operation is –0.2 V below the negative rail. For example, if the negative supply is –2.5 V, the input signal can swing below the negative rail to –2.7 V. Figure 6-3 illustrates the swing to the positive rail. Doing a Kirchhoff's walk to the positive supply, shows that the that the input signal can swing to 1 V below the positive rail or 1.5 V in this example. Since this op amp uses P-channel devices the op amp can swing all the way to the negative rail, but has limitations with the positive rail. An N-channel device behaves in the opposite manner.

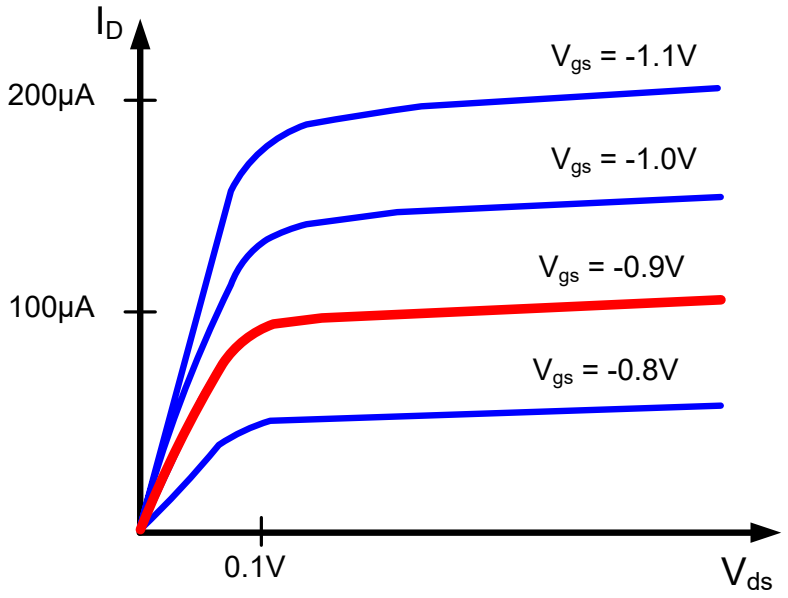

Figure 6-1. Characteristic Curve for P-channel MOSFET

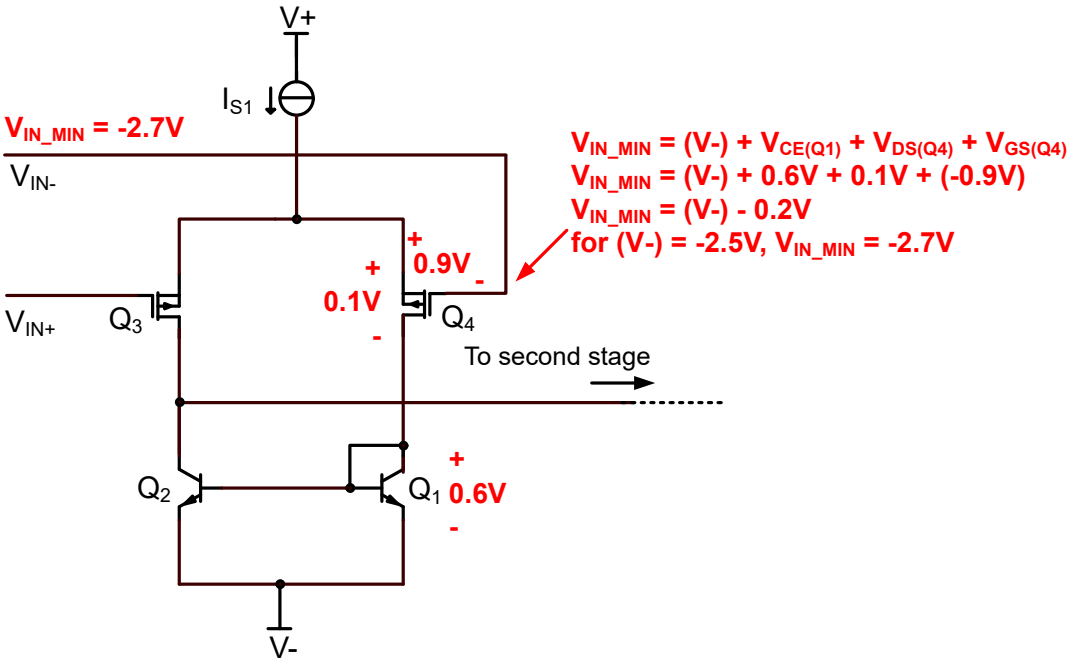

Figure 6-2. Swing to Negative Supply Rail Limitation for P-channel MOSFET

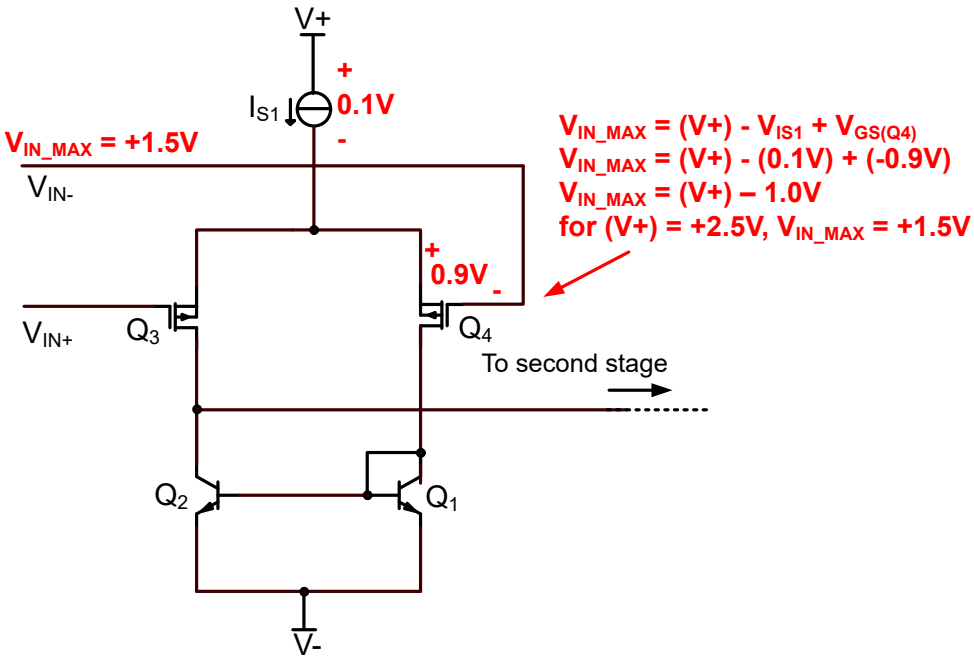

Figure 6-3. Swing to Positive Supply Rail Limitation for P-channel MOSFET

7 Rail-to-Rail CMOS Amplifiers

CMOS amplifiers also can have input common mode from the negative to positive op-amp power supply (rail-to-rail common-mode range). In many cases, the input common mode actually extends beyond the supply rails. For example, a rail-to-rail CMOS device with a ±2.5-V supply can have common-mode range 200 mV beyond the supply rails (–2.7 V < V_{CM} < +2.7 V). From an internal operation perspective, one common way that this feature is implemented is to use both a PMOS and NMOS differential input stage. Observe in the previous CMOS example that a PMOS input stage has common-mode range to the negative supply and NMOS input stage has common-mode range to the positive supply. The rail-to-rail input structure uses both types of input transistors with a circuit to enable and disable the transistors according to their valid common-mode range. There is a small common-mode range, called the crossover region, where both sets of transistors are turned on.

One disadvantage to this approach is that the offset of the PMOS transistor pair is different from the offset of the NMOS pair. This difference causes an abrupt transition of offset voltage when the common-mode voltage transitions through the crossover region. This offset transition introduces crossover distortion that is inherent with this type of rail-to-rail amplifiers. Note that for precision devices, the offset of the two input pairs is often trimmed so that the mismatch is minimized. Even in trimmed devices some crossover distortion is introduced as the offset changes in the crossover region because both input pairs are turned on simultaneously. Figure 7-1 illustrates a simplified rail-to-rail input stage and the associated offset response versus common-mode input. Note that the common-mode range is broken into the PMOS region, crossover region, and NMOS region.

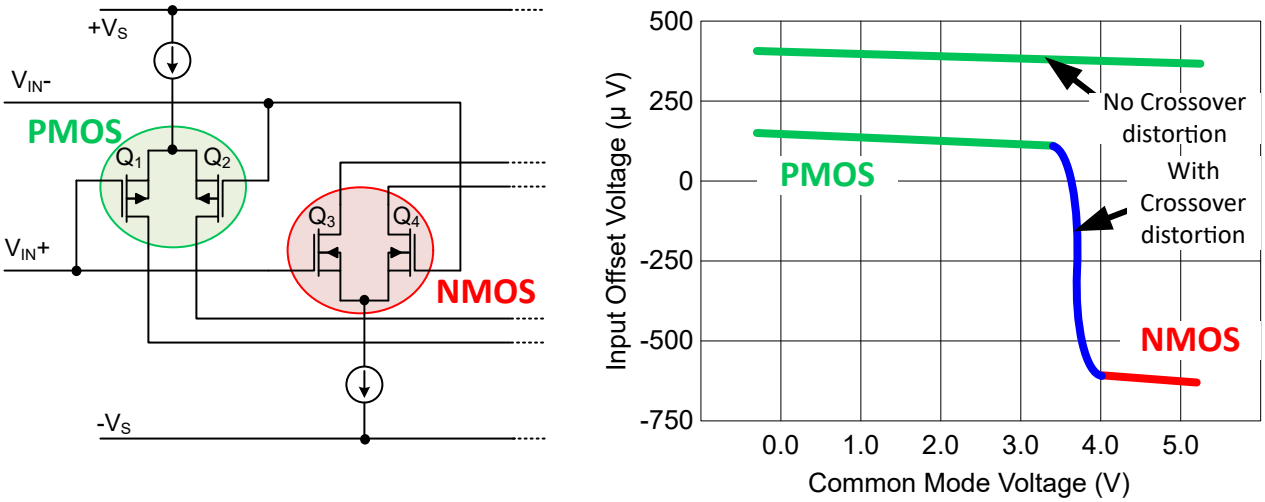

Figure 7-1. Rail-to-Rail Input Stage With Two Input Pairs and Associated Offset vs Common-Mode Graph

Figure 7-2 illustrates how a sinusoidal signal is impacted by crossover distortion from the rail-to-rail input stage. In this example, the input signal is applied to a unity gain buffer that has an input stage with crossover distortion. The input signal is an ideal sinusoidal waveform, and the output signal tracks the input until the common mode transitions through the crossover region. When passing through the crossover region, the amplifier offset changes so the output signal shifts up or down according to the offset shift. This offset change can range from microvolts to millivolts depending on the amplifier offset. Generally, this shift is too small to notice on an oscilloscope, so this image is exaggerated for illustrative purposes. This kind of distortion is noticeable in the frequency domain or when THD is calculated. The amplifier from Figure 7-3 has a crossover region at 3.75 V and is configured in a buffer configuration. When the input signal avoids the crossover region the distortion is low (THD = 108.5 dB). When the signal passes through the crossover region, the distortion increases (THD = 83.8 dB). Furthermore, inspecting the FFT graph shows significant increase in the harmonic components.

Amplifiers with crossover distortion often provide a specification for common-mode rejection ratio (CMRR), that is defined according to the crossover region. Table 7-1 shows a typical CMRR specification for a rail-to-rail amplifier with crossover distortion. Notice that the CMRR is significantly better when the input range is limited below the crossover region ($CMRR_{MIN}$ = 76 dB, V_{IN}< (V+) – 1.4 V) as compared to the entire input range ($CMRR_{MIN}$ = 65 dB, V_{IN} < 5.7 V).

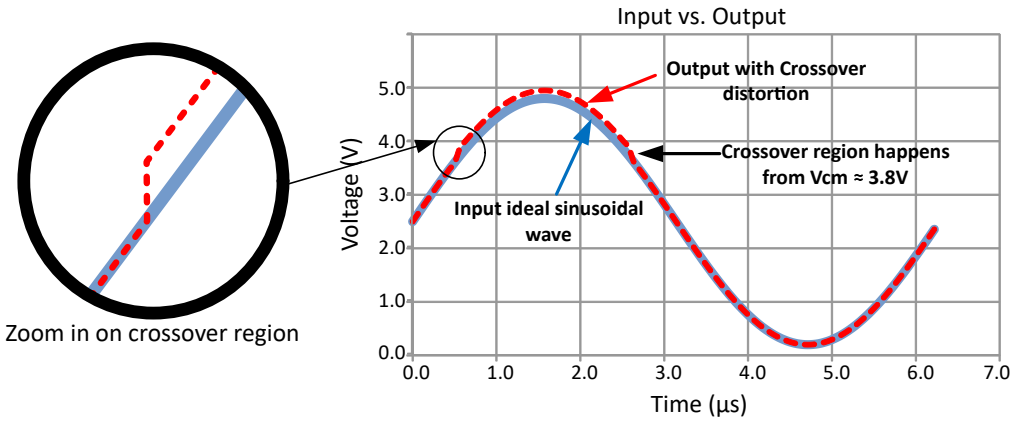

Figure 7-2. Rail-to-Rail Input Stage With Two Input Pairs and Associated Offset vs Common-Mode Graph

Table 7-1. Common-Mode Rejection Specification for an Op Amp With Crossover Distortion (OPA316)

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
CMRR	Common-mode rejection ratio	V_S = 5.5 V, (V–) – 0.2 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to 125°C	76	90		dB
		V_S = 5.5 V, V_{CM} = –0.2 V to 5.7 V, T_A = –40°C to 125°C	65	80		dB

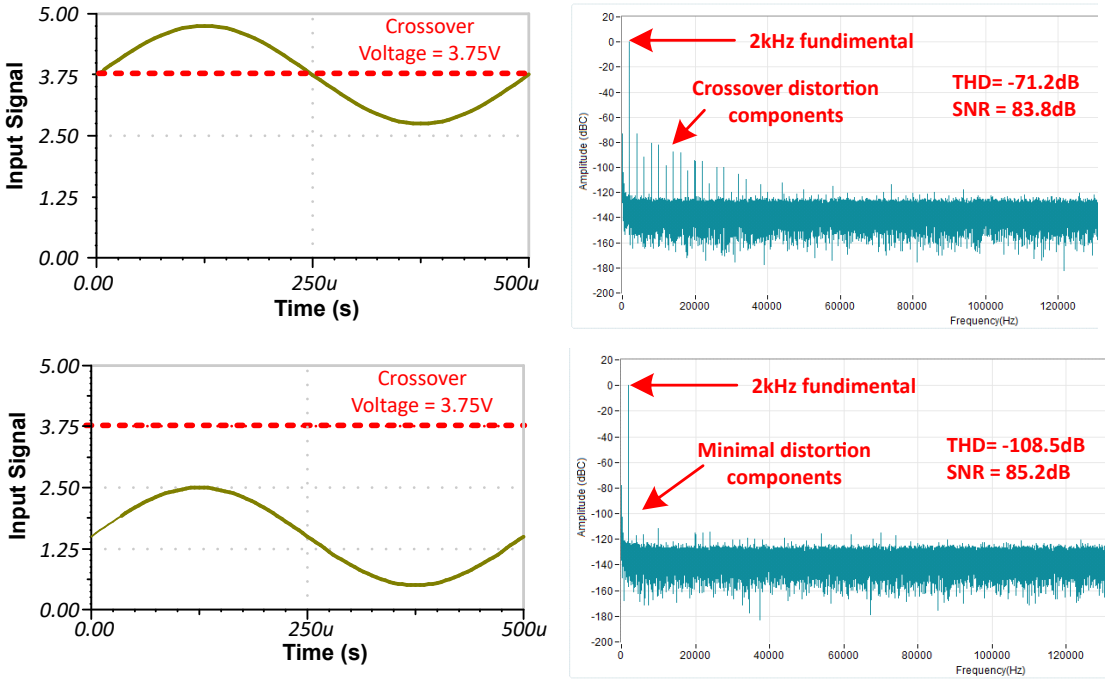

Figure 7-3. FFT of Signal Inside and Outside of the Crossover Region (OPA316)

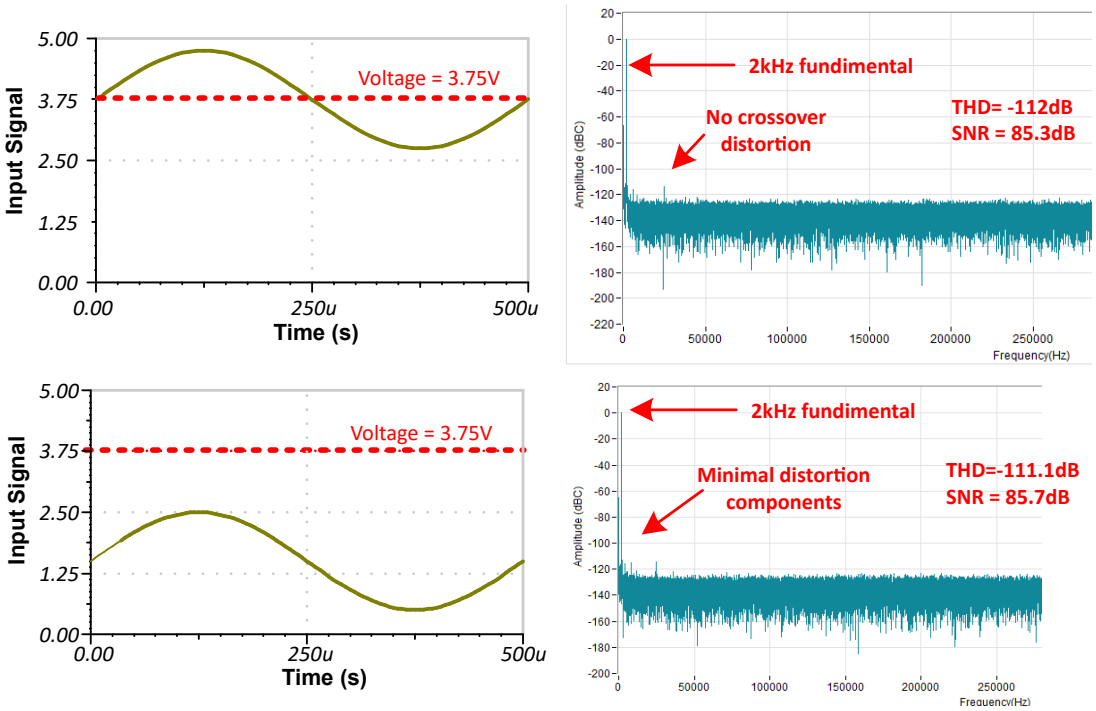

Figure 7-4. FFT of Signal Inside Applied to a Zero-Crossover Distortion Device (OPA320)

A different approach to rail-to-rail common-mode range is to use a single PMOS input stage with an internal charge pump to boost the supply. For this approach, the charge pump generally boosts the internal supply of the input stage by approximately 1.8 V. An amplifier with a 5-V supply is internally boosted to 6.8 V. The internal PMOS stage operates linearly to approximately 1.0 V from the positive supply, so amplifier common mode extends to 5.8 V (6.8 V – 1.0 V = 5.8 V). Note that although the common-mode range can extend to 5.8 V, the ESD input structure clamps the input at about 5.3 V. This example is illustrated in Figure 7-5. Although the values can differ for different devices, the principle is the same for all zero-crossover devices. Since this approach only uses one input transistor pair, it does not have crossover distortion and is called a zero-crossover amplifier. Figure 7-4 shows the FFT of a zero-crossover op amp (OPA320). This measurement was made under the same test conditions and hardware as was used for Figure 7-3, but the amplifier was changed to a zero-crossover type. Observe by comparing the two figures that when the signal is below 3.75 V, the performance for the two circuits is similar. This is because neither op amp is in a crossover region for this common-mode range. However, when the signal passes through 3.75 V, the OPA316 shows crossover distortion but the OPA320 does not have crossover distortion.

For the zero-crossover device, the input stage does not consume much power, so this charge pump does not need external components to function. Nevertheless, this zero-crossover type input stage has some additional noise from the charge pump circuit. This noise can show up in the time domain as a ripple on the noise signal, or in the noise spectral density curve as a tone at the charge pump switching frequency. However, this noise is quite low for most modern zero-crossover devices, and can be insignificant for many applications. Figure 7-6 illustrates two examples of how the noise transient can show up in the time and frequency domain measurements of a device with the internal charge pump. Notice that the OPA320 has noise tones at 6 MHz and harmonics of this frequency. These tones are related to the switching of the internal charge pump. Comparing the OPA320 to the OPA365 shows larger noise tones for the OPA365. The OPA320 is a modern version of this zero-crossover technology and significant effort has been placed on minimizing the charge pump noise. Also observe that the time domain noise for the OPA365 shows a periodic charge pump signal whereas the OPA320 charge pump signal is buried in the broadband noise. In general, for zero-crossover devices, the charge pump noise is mainly a concern for low-gain applications. In higher-gain applications the amplifier bandwidth is normally below the charge pump switching frequency, so the noise tones are attenuated. Furthermore, an external filter can be added to further minimize any charge pump switching noise.

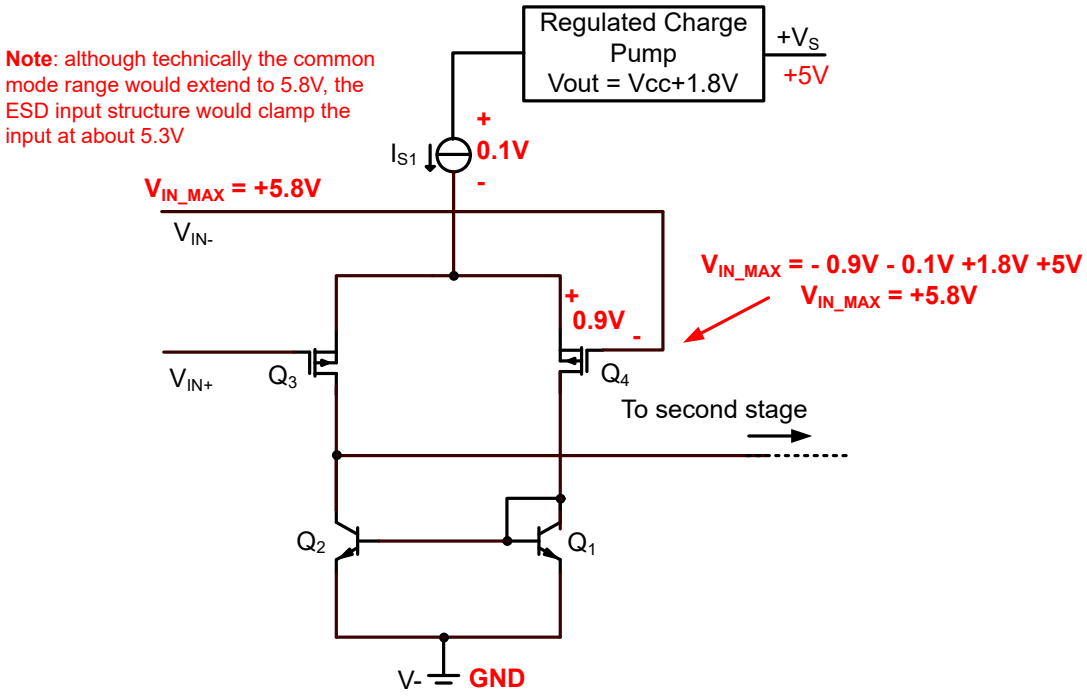

Figure 7-5. Zero-Crossover Internal Operation to Positive Supply Rail

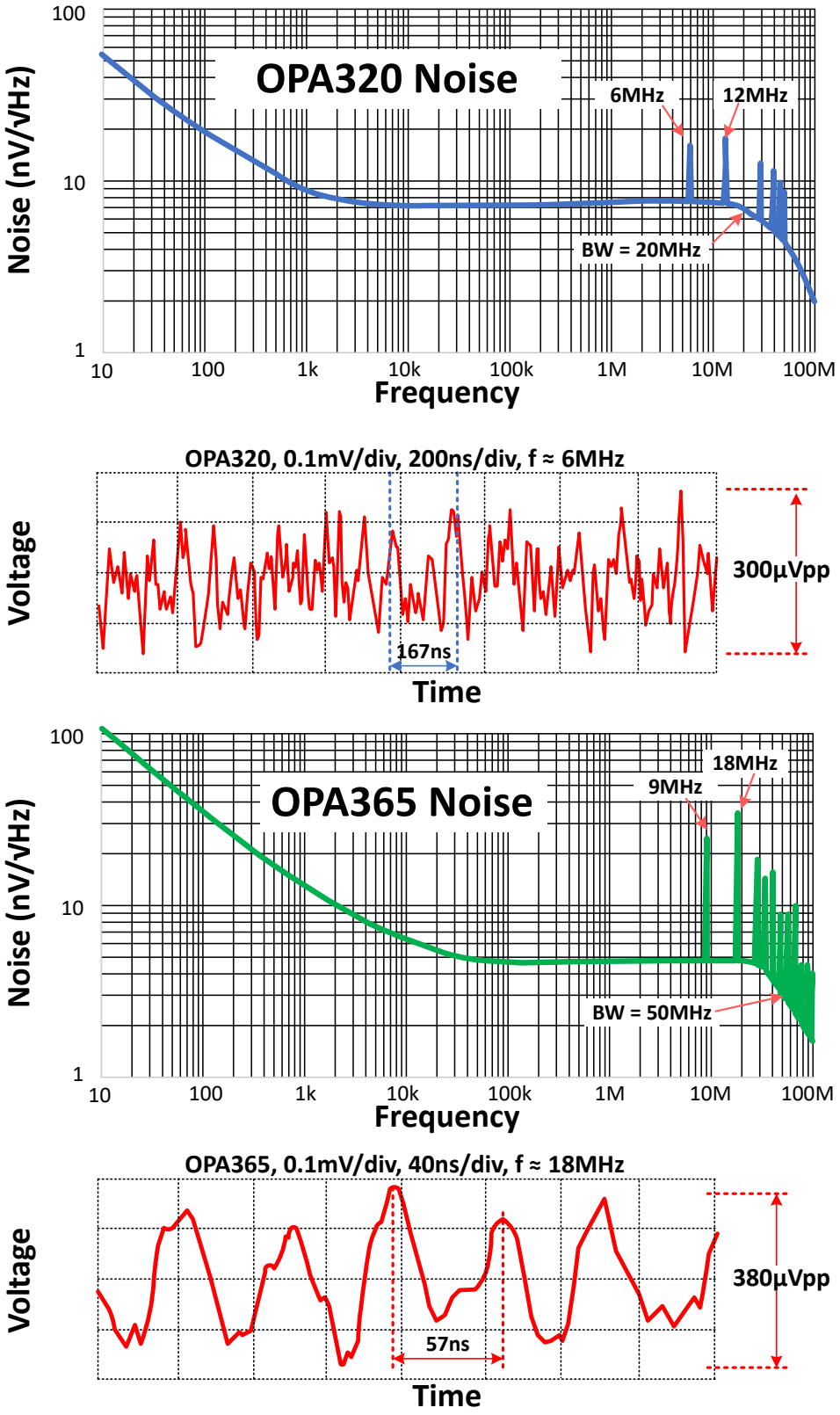

Figure 7-6. Time and Frequency Domain Graph for Device With Internal Charge Pump (Zero-Crossover)

8 Output Swing Limitations Inside a Bipolar Op Amp

At room temperature, the classic bipolar output stage shown in Figure 8-1 has an output swing limitation of approximately 0.9 V from the supply rail. In this example, for linear operation the minimum voltage from the output to the positive supply can be calculated as the sum of the base-to-emitter voltage of Q1 and the saturation voltage of Q3 (Vbe + Vsat = 0.7 V + 0.2 V = 0.9 V). Other more complex topologies can have even greater output swing limitations. It is not unusual for bipolar devices to have between 1-V and 2-V output swing limitations depending on the design. Later sections cover how both CMOS and bipolar rail-to-rail output configurations can swing much closer to the supply rails.

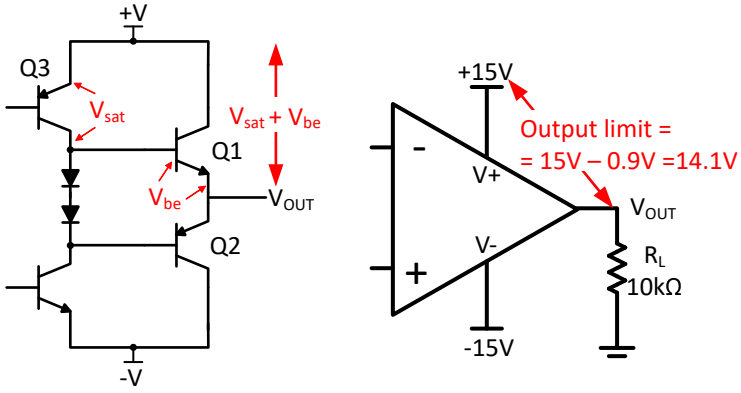

Figure 8-1. Bipolar Output Stage Example Where Swing is Limited to 0.9 V From Supply

9 Linearity of Output Swing Specifications

To this point linear and non-linear regions of operation for output swing limitations have been documented. In reality, the limitations given for output swing in the data sheet tables are generally saturation limitations. That means that one of the output transistors is fully turned on and the other is fully off. For a triangle input signal, the output is clipped when the signal reaches the saturation limit (see Figure 9-1). However, it is important to understand that the amplifier does not abruptly transition from linear operation to completely non-linear (saturated). In fact, as the output signal approaches the saturation limit, the signal begins to become non-linear. Unfortunately, it is not always obvious according to data sheet specifications where the output begins to become non-linear or the extent of the non-linearity.

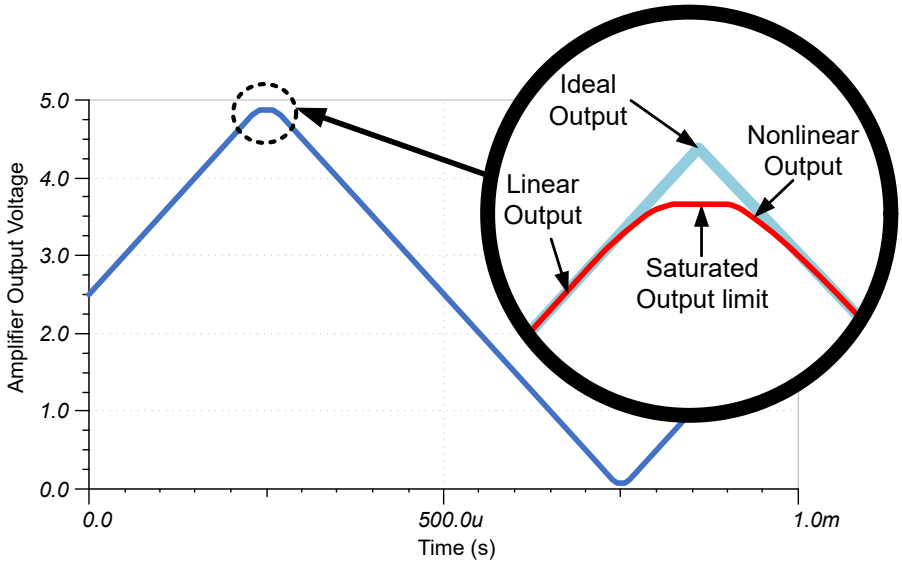

Figure 9-1. Linear Output Range versus the Saturation Output Swing Limit

One common approach used to estimate the range where the amplifier has excellent linearity is to check the test conditions for the open-loop gain specification (A_{OL}). Figure 9-1 illustrates the data sheet specification for output swing and A_{OL}. Notice that the test condition for A_{OL} indicates that A_{OL} is specified for output voltages of 100 mV from the supply rails unloaded, and 200 mV from the rail with a 2-kΩ load. The same data sheet illustrates that the saturation limit is 5 mV from the supply rail unloaded, and 15 mV with a 2-kΩ load. The main point is that somewhere between saturation and the A_{OL} test limit the open loop gain begins to drop off leading to non-linear operation.

Table 9-1. Linear and Saturation Limits on Data Sheet Excerpt

Parameter OPA328		Test Conditions		MIN	TYP	MAX	UNIT
V_O	Voltage output swing from both rails	V_S = 5.5 V **(saturation limit)**	R_L = 10 kΩ			5	mV
			R_L = 2 kΩ			15	mV
A_{OL}	Open-loop voltage gain	(V) + 100 mV < V_O < (V+) – 100 mV R_L = 10 kΩ, **(linear limit)**	T_A = 25°C	108	132		dB
			T_A = 40°C to +125°C	96	130		dB
		(V–) + 200 mV < V_O < (V+) – 200 mV R_L = 2 kΩ **(linear limit)**	T_A = 25°C	106	123		dB
			T_A = –40°C to +125°C	90			dB

10 Output Voltage Swing vs Output Current

We now know that data sheet tables provide an output swing saturation limit for a few different loads. Also, the open-loop gain specification from the data sheet specification table can be used to infer the linear output swing limitations. Beyond the specifications table, the data sheet provides a set of typical characteristic curves. The output voltage swing vs output current curve shows the typical output swing saturation limit for amplifiers (see Figure 10-1). The curve shows how output swing is impacted by a wide range of different load currents. The graph also shows how temperature impacts output swing. For CMOS, output swing gets worse for increasing temperature whereas for bipolar the output swing improves for increasing temperature due to the negative temperature coefficient of the base to emitter voltage (ΔV_{BE} = –2 mV/°C). Finally, the output voltage swing curves illustrate the short-circuit current limit. The short-circuit limit is from an internal protection mechanism that limits the amplifier output stage drive when excessive current is drawn. On the graph, the short circuit current limit is the section where the output voltage drops rapidly at high current.

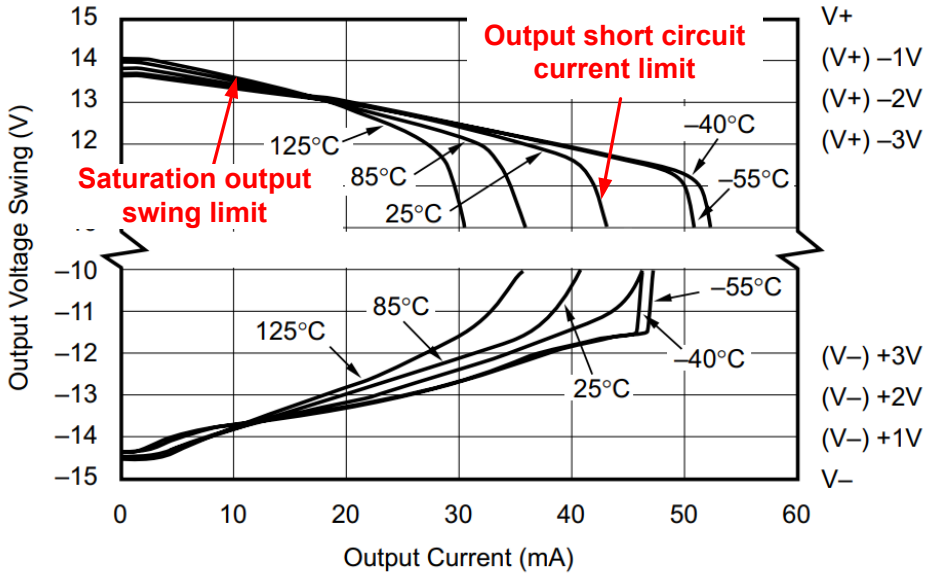

Figure 10-1. Output Voltage Swing vs Output Current for Classic Bipolar Output Stage OPA277

11 Classic Bipolar vs Rail-to-Rail Output Stage for CMOS and Bipolar

Figure 11-1 compares a classic bipolar output stage to a CMOS and bipolar rail-to-rail output stage. The classic bipolar output swing is limited by a base-to-emitter drop of Q1 and the saturation of Q3. This configuration is sometimes called a common emitter push-pull output. The rail-to-rail bipolar output stage uses a common collector configuration. The output swing limitation for the rail-to-rail bipolar common collector circuit is the saturation voltage of the output transistor. For bipolar devices the saturation voltage is between 0.2 V and 0.3 V. Thus, for bipolar rail to rail the best output swing is approximately 0.2 V from the supply rail.

The rail-to-rail CMOS common-drain configuration is only limited by the voltage drop when the MOS transistor is driven into triode or ohmic region ($V_{DS} \leq V_{SAT}$)[1]. This minimum voltage is set by the physical size (channel width / length) of the transistors. The size sets the minimum resistance for the transistor that occurs when the transistor is fully turned on. The example shows the output swing to the positive rail is limited by the minimum drain-to-source voltage of the PMOS output transistor. The voltage depends on the current flowing through the transistor and the resistance of the transistor. A large (W / L) output transistor has a small resistance and can have a very low voltage drop if the output current is small. It is not unusual for CMOS output stages to have output swing within millivolts from the supply rail when the output current is low. However, increasing the load current causes a larger voltage drop on the output transistor so the output swing is degraded.

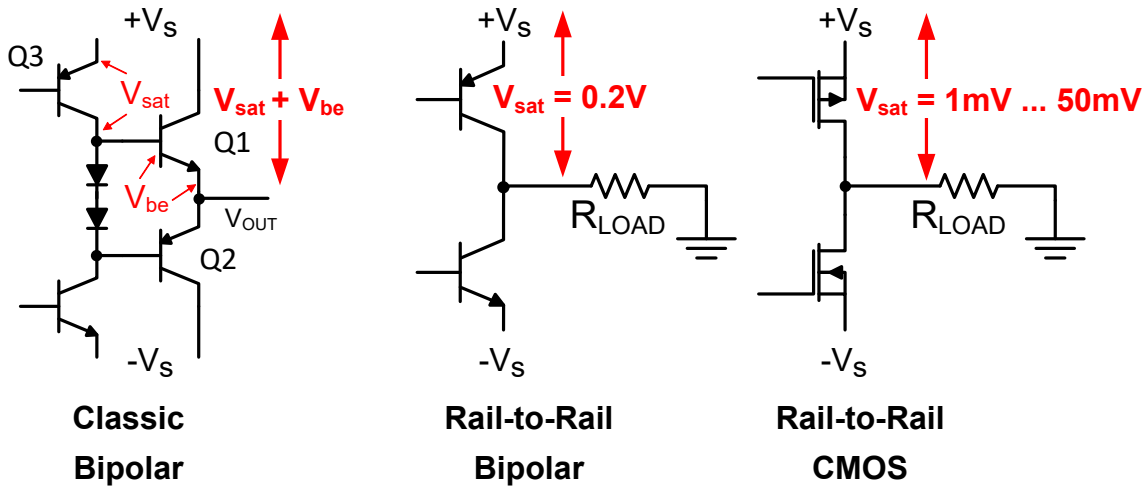

Figure 11-1. Classic Bipolar Output Stage vs CMOS and Bipolar Rail-to-Rail Output Stage

One key difference between the bipolar device and CMOS device is that the CMOS device acts like a resistor when fully-on, but the bipolar device has a 0.2-V saturation voltage that is relatively constant for different currents. For low output currents CMOS rail-to-rail devices can swing very close to the rail, whereas bipolar devices are limited by the 0.2-V saturation voltage. However, at higher currents the output swing on the CMOS degrades but the bipolar output swing remains relatively constant at 0.2 V. Figure 11-2 shows that for very low output currents the CMOS device swings within millivolts from the rail, but at 20 mA of output current the swing is degraded by approximately 1 V. Conversely, the output swing bipolar device remains relative constant from 0 mA to 30 mA of output current.

[1] When comparing CMOS topologies to bipolar, the terminology can be confusing because the term saturation for bipolar transistors indicates a transistor that is operating in non-linear region with a minimum collector-to-emitter drop whereas saturation for CMOS actually refers to the linear (flat part) of the characteristic curve where the device is normally biased. For MOS transistors, the transistor is in the triode (ohmic / nonlinear) region when the transistor has minimum drain-to-source resistance minimum V_{DS} voltage.

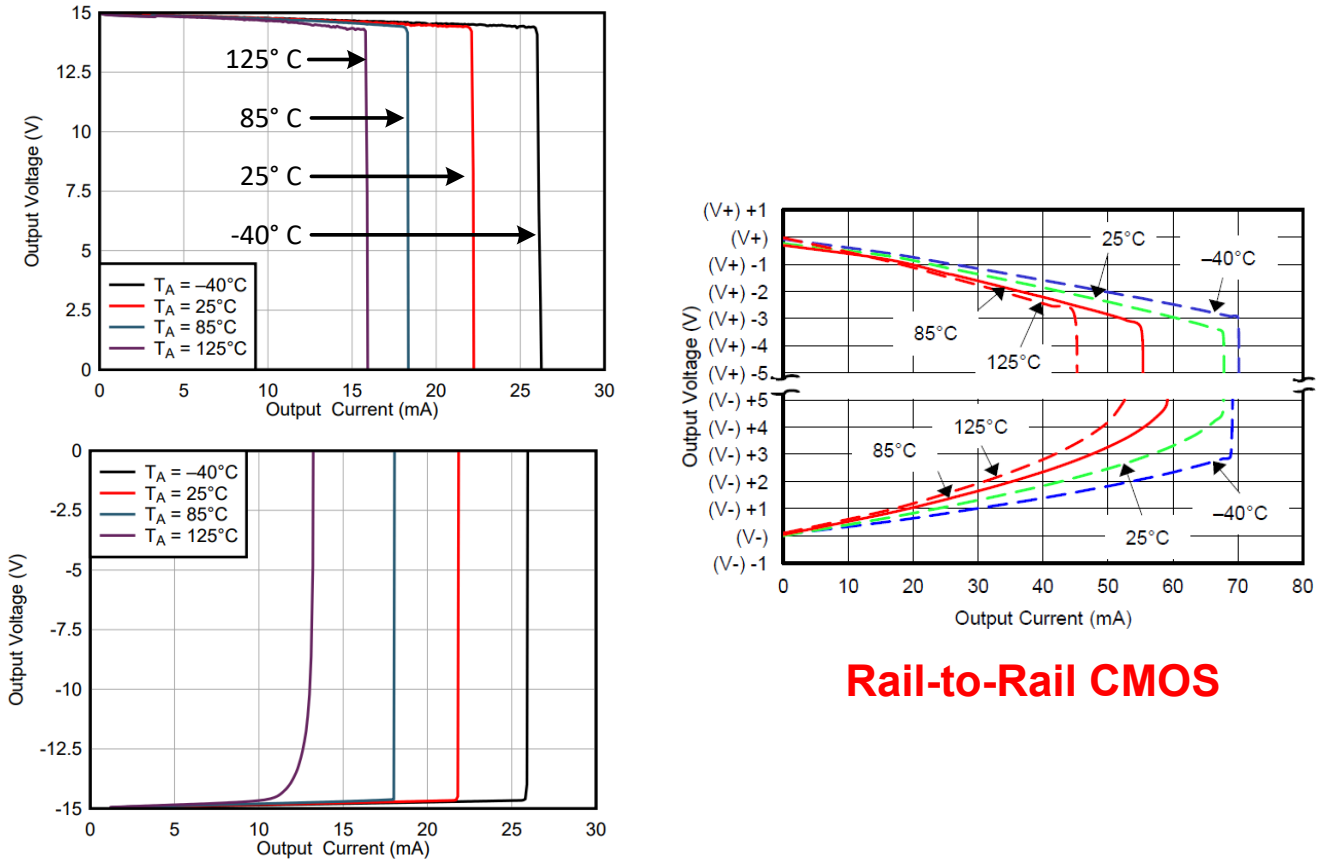

Figure 11-2. Bipolar Rail-to-Rail vs CMOS Rail-to-Rail

One common request is to design an amplifier that can swing all the way to the supply rail (0-V swing limitation). Unfortunately, rail-to-rail output swing is not practical. Even if the output transistors are sized to be quite large it is always necessary to have an output-stage bias current in the output stage for linear operation. Thus, a current flows in the output transistor even when the load current is zero. This bias current creates a voltage drop (V_{DS} – R_{ON} × $I_{Q(OUT)}$) on the output transistor and limits the output swing. Increasing the size of the output transistor helps minimize this limitation but cannot eliminate the output swing limitation. Furthermore, there is a practical limit to the size of the output transistors from a cost and performance perspective.

12 Rail-to-Rail Output and Open-Loop Gain Dependence

As mentioned previously, the traditional output stage uses a common emitter topology and the rail-to-rail output stage uses a common collector topology. The common emitter configuration gain is approximately unity, whereas the common collector has a significant gain that is dependent on the load impedance. The open-loop gain for an op amp is the product of all the gain values for each amplifier stage. So, for a rail-to-rail amplifier, the DC open-loop gain changes when the amplifier load changes. Thus, for rail-to-rail devices, connecting a low-resistance load on the output of the op amp causes open loop gain to drop compared to the unloaded case. Conversely, the loading impact of loading on a traditional common emitter output stage has a minimal effect on open-loop gain. Table 12-1 shows an excerpt from a data sheet showing how open-loop gain is impacted by load resistance. Figure 12-1 shows how this loading impacts the A_{OL} curve. Although this discussion focused on bipolar amplifiers the same concepts apply to CMOS devices.

Table 12-1. Impact of Loading on DC Open-Loop Gain Table (OPA210)

OPA210							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
A_{OL}	Open-loop voltage gain	(V–) + 0.2 V < V_O < (V+) – 0.2 V R_L = 10 kΩ	T_A = 25°C	126	132		dB
			T_A = –40°C to +125°C	120			dB
		(V–) + 0.6 V < V_O < (V+) – 0.6 V R_L = 600 Ω	T_A = 25°C	114	120		dB
			T_A = –40°C to +125°C	110			dB

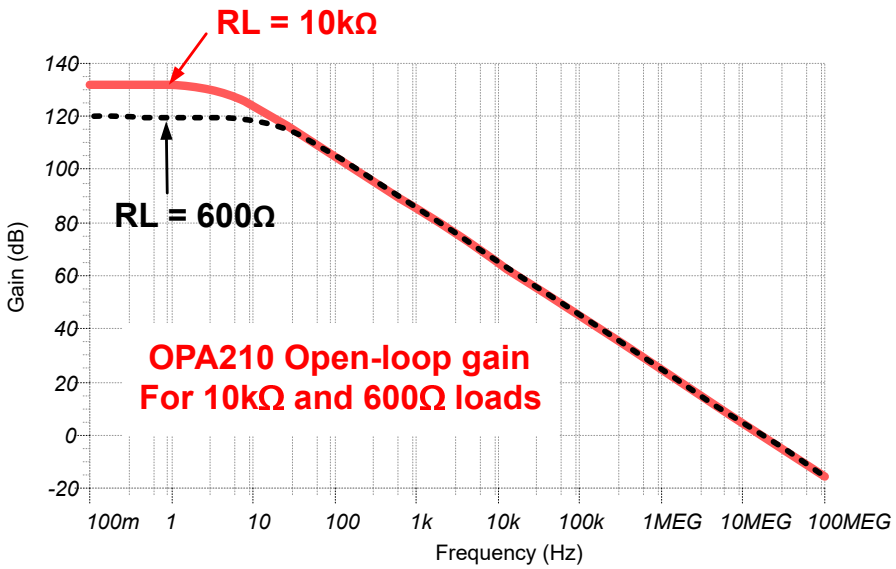

Figure 12-1. Impact of Loading on A_{OL} Curve vs Frequency (OPA210)

13 Output Short-Circuit Protection

The vast majority of op amps have an output short-circuit protection circuit. This circuit limits the output current to protect the device when the output of the op amp is shorted to ground. In fact, the output can be shorted to any voltage between the power supply and the circuit protects the device from damage. Shorting the op-amp output to a voltage outside the supply limits turns on the output ESD structures and if unprotected, damages the amplifier. The short circuit limit can be seen on the output voltage versus output current curve as an abrupt drop in output voltage when the limit is exceeded. Note that the short-circuit current is generally designed to have a negative temperature coefficient so that the device does not go into thermal runaway[2]. For example, if the short-circuit limit is tripped at room temperature, the device self-heats, but the current limit decreases as the temperature increases to reach equilibrium. Figure 13-1 shows how short-circuit limit decreases with increasing temperature. For example, the positive short-circuit limit is 67 mA at 25°C and 60 mA at 85°C. The figure also illustrates that the short-circuit limit is not necessarily symmetrical depending on the output voltage of the amplifier because different types of transistors drive the positive and negative output swing. For example, the positive short circuit limit at 25°C is approximately 67 mA, but the negative is 55 mA.

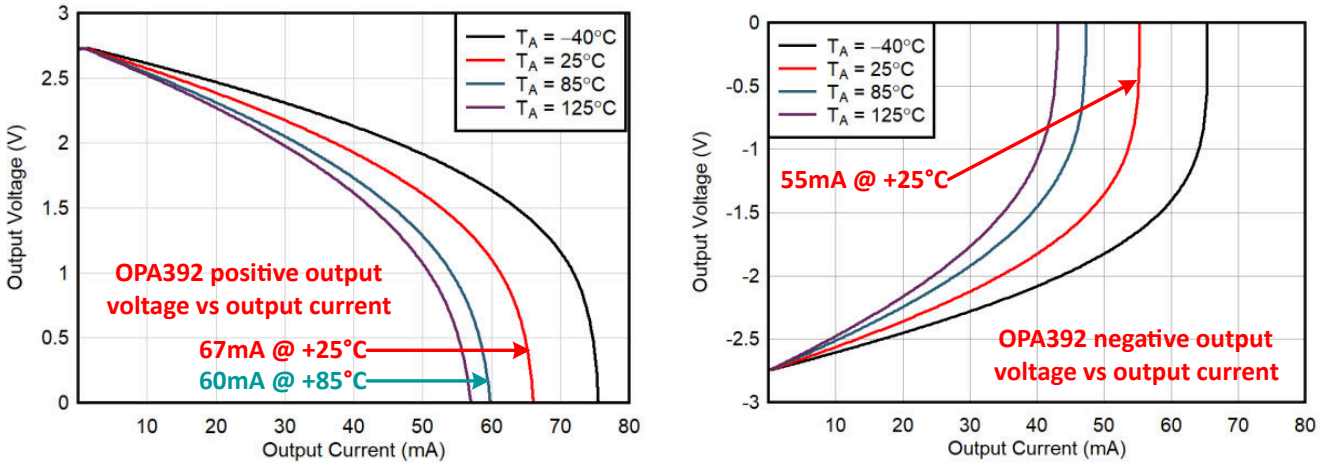

Figure 13-1. Short-Circuit Limit vs Temperature for OPA392

[2] Thermal runaway occurs when an increase in device temperature causes an internal change in device operation which further increases the device temperature. This condition leads to device damage. This problem is not a concern on modern amplifiers. Thermal runaway is mentioned here to explain the temperature coefficient for short-circuit current.

Figure 13-2 illustrates a simplified op-amp output short-circuit protection. Q1 and Q4 are the classic bipolar output stage. Transistors Q2 and Q3 and the output current sense resistors R1 and R2 form the short-circuit protection. For example, assume the output is driving a positive voltage, and is shorted to ground. Doing this causes a large current to flow through Q1. This current develops a drop on R1 that turns on Q2. Turning on Q2 steals base current from Q1 which decreases the output of Q1. This effectively limits the output current by turning down the output drive transistor. The same phenomena occurs on Q3 and Q4 if the amplifier were grounded when driving a negative output.

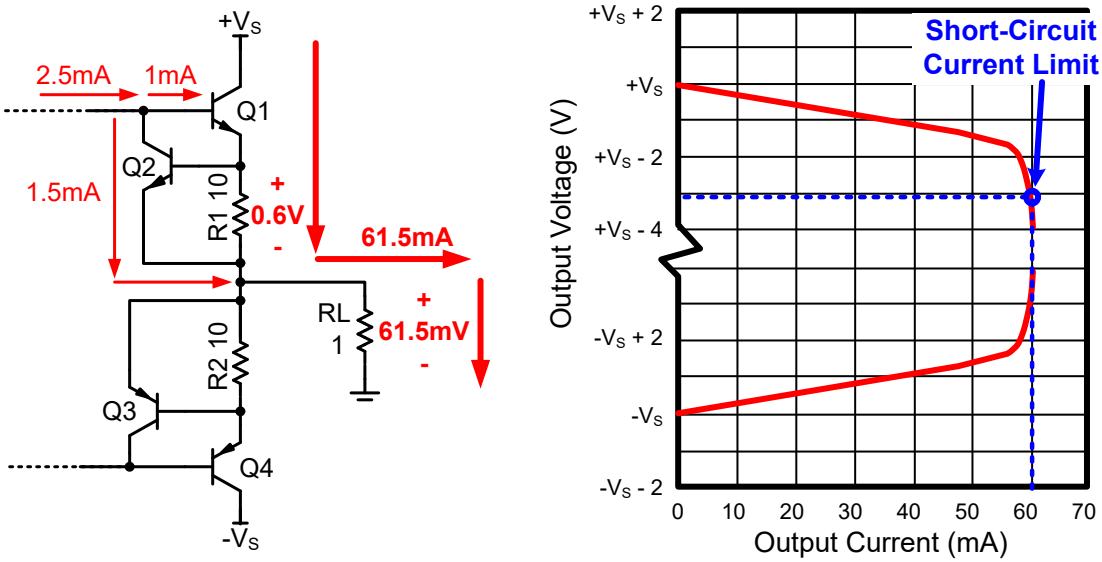

Figure 13-2. Short-Circuit Protection Inside Bipolar Amplifier

14 Overload Recovery

Exceeding the output swing range for an amplifier causes transistors in the output stage to saturate for bipolar and triode for CMOS. Once the input condition causing the output swing violation is removed, it takes some time for the output to leave this non-linear condition. This time period is called the overload recovery time. Transitioning a bipolar transistor from a saturated state to a linear operating state introduces a delay because, when in saturation, the transistors gain is abnormally low, and the collector-to-base junction is forward biased. Some time is required for this abnormal condition to reverse itself.

Many amplifier data sheets provide a specification or graph showing output overload recovery time. This specification relates to driving the output outside the valid output voltage swing limit. A similar phenomenon can occur when input common-mode limits are exceeded, but this effect is generally not specified. For a particular device, the overload recovery time can differ depending on if the output is saturated to the positive or negative power supply rail. This difference is because the type of output transistor saturated is different in the two cases, and the two different transistor types have different specifications. It is also worth noting that zero-drift amplifier types can have significantly longer overload recover times as compared to traditional amplifiers. This is because a saturated amplifier has a very large differential input voltage and the zero-drift calibration mechanism attempts to correct for that error. Once the input is transitioned to a valid range, the zero-drift calibration takes several clock cycles to recover from the overload condition, so a recovery time of 10 µs to 50 µs is not unusual.

Figure 14-1 shows a typical graph illustrating the overload recovery for OPA828. In this example, the amplifier is configured in a gain of –10 V/V with a –2-V input applied to saturate the output to +18 V. The input signal is stepped from –2 V to 0 V to bring the output out of saturation. The delay from the start of the step to where the output leaves the saturated state indicates the positive overload recovery time. The negative overload recovery time uses the same method but the input step transitions from +2 V to 0 V. Notice that the positive and negative recovery time is different for the two cases (40 ns and 50 ns, respectively).

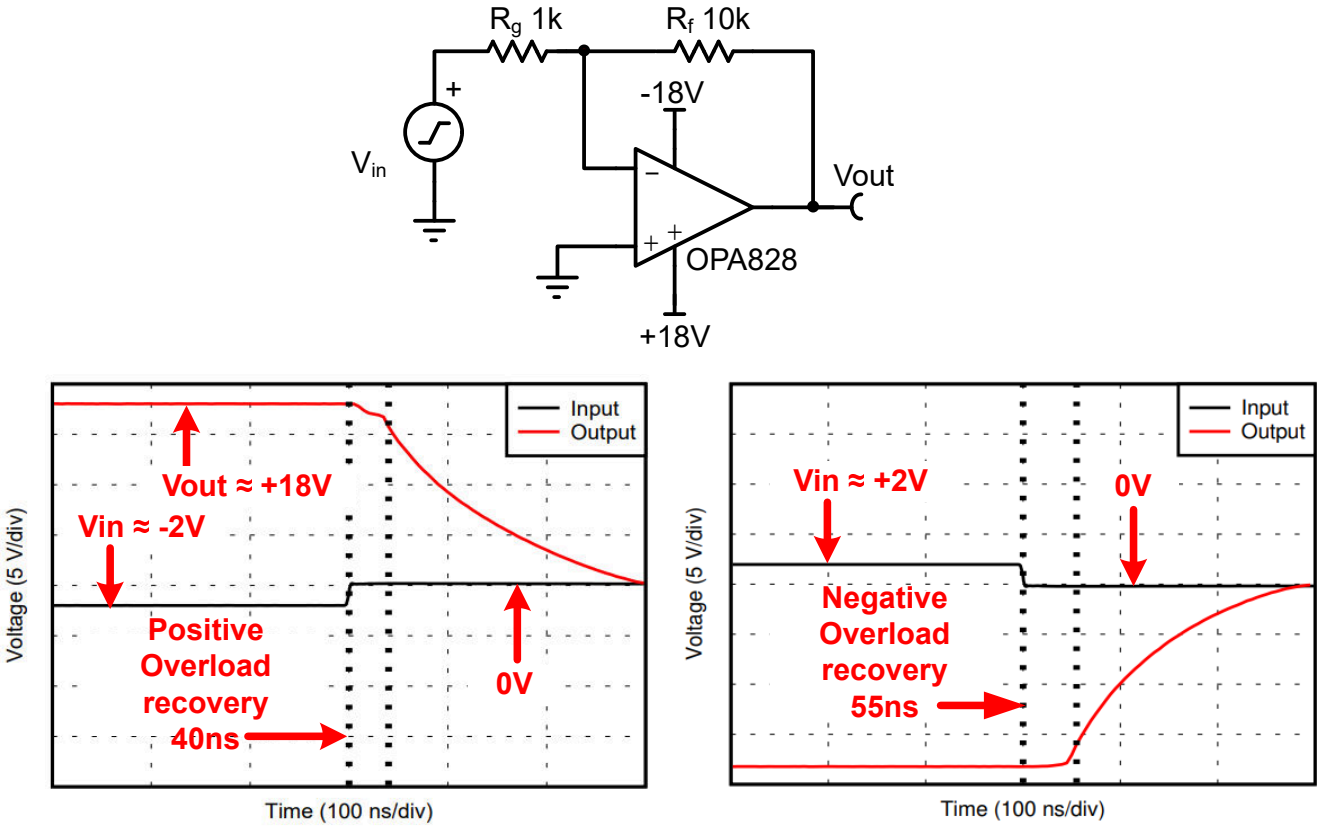

Figure 14-1. Overload Recovery on OPA828

15 Supply Current During Input and Output Swing Limitations

The majority of op-amp supply current flows through the amplifier output stage. For a bipolar amplifier driving the output stage beyond the output swing limitation causes one of the output transistors to saturate. Saturation of a bipolar transistor causes the current gain to dramatically decrease. The decrease in current gain in the output and preceding stages causes a significant increase in input base current of these transistors and consequently increases the overall op amp supply current. This increase in supply current is generally even higher with circuits that have a slew-boost circuit as the slew-boost is normally triggered when the output is driven to the supply rail. The OPA828 is an example of device that has a special feature that disables the slew-boost circuit when the output is driven into the supply rail. This feature significantly decreases the supply current compared to other similar devices that do not include this feature (see Figure 15-1).

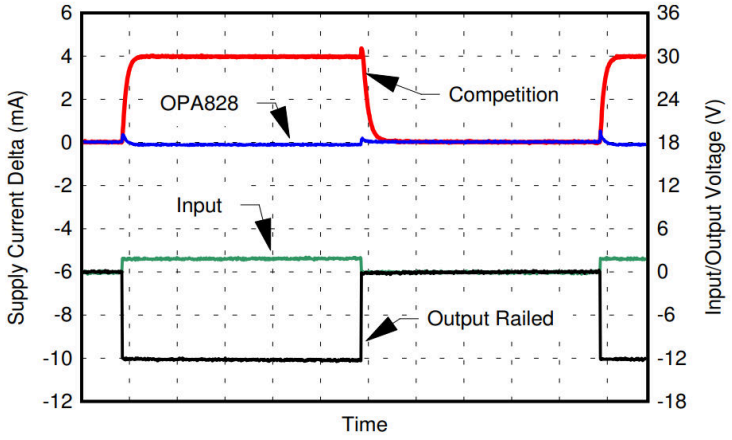

Figure 15-1. Supply Current Change With Overloaded Output (OPA828 vs Competition)

When a CMOS output stage is driven into the supply rail, the transistors go into triode state (fully turned on). In this case, the biasing of the output stage is not disrupted in the same manor as the bipolar configuration, so output stage current does not significantly increase. The exception case is CMOS amplifiers with slew-boost that do not include the previously-mentioned disable feature.

From an input perspective, supply current is generally not impacted by common-mode range violations, but the input bias current (I_B) of bipolar devices can be affected. Whenever a bipolar transistor is saturated, the current gain (beta) significantly decreases causing an increase in the base current. Since CMOS devices are voltage controlled, the non-linear operation of the input stage that occurs during common-mode violations does not impact the bias current. Figure 15-2 contrasts input bias current vs common-mode voltage for CMOS and bipolar amplifiers.

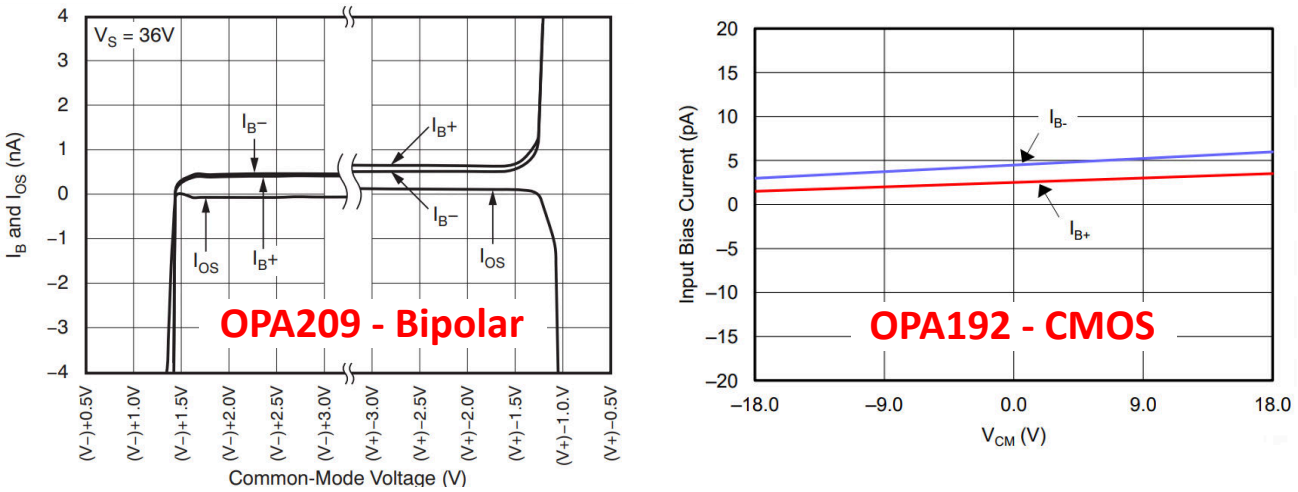

Figure 15-2. Bias Current vs Common-Mode Voltage

16 Summary

This document explains the input common mode and output swing limitations for op amps. A simplified explanation of the internal circuitry is covered to provide intuition behind differences between CMOS and bipolar technologies. Furthermore, the operation of features such as amplifier rail-to-rail inputs and outputs are covered. The limitations and advantages of these features relative to distortion, and noise, and other specifications are covered. Finally, the operation of short-circuit protection, overload recovery, and other features related to op-amp input and output stages is covered.

17 References

1. Lis, Marek. Interview and discussions on amplifier design, 23 October, 2023.
2. Gray, P. R., Hurst, P. J., Lewis, S. H., Meyer, R. G., 2009, *Analysis and Design of Analog Integrated Circuits*, Wiley; 5th edition
3. Williams, I., Kay, A., *Input and Output Limitations*, https://www.youtube.com/watch?v=q9jz1cY_1ts
4. Williams, I., Kay, A., *Input and Output Limitations – Common Mode Voltage*, https://www.youtube.com/watch?v=D60-68JcQD0
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