Application Note

2nd Order Shelving Filter Design for DC in AC Sensing

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ABSTRACT

Some current sensing applications in the metering and power conversion space require DC current sensing alongside the AC current sensing. The DC often is an unwanted or false signal content which needs to be detected, measured, and removed. For instance, in AC power systems, DC energy dissipates in a transformer as heat because DC energy cannot be transferred across the transformer. This energy dissipation creates power losses and thermal problems. Current sensing in such applications can be realized by a shunt-based approach measuring the voltage drop across a small value sense resistor. DC signals within the AC are very small and challenge the dynamic range of a system. This application note introduces a preconditioning filter circuit to relax those requirements and improve the DC in AC measurement.

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Trademarks

1 Introduction

When measuring current, often shunt-based designs are used. In grid systems, the AC content is 50/60 Hz based and contains the fundamental plus harmonic distortion. For example, in power quality analysis or DC/AC power conversion, the harmonics are analyzed individually to monitor and minimize distortion. The AC carries the main power but an unwanted DC content can be present in addition which must be eliminated by the control loop or detected as an error. Therefore, measuring the DC value at the same time is important. For example, a DC/AC system can generate a 20-A AC current sine wave. At the same time, a 20-mA DC current must be measured. This requirement increases the dynamic range of the system and challenges the analog to digital conversion. Furthermore, the voltage across the shunt can be small such that an external gain stage can be beneficial.

2 Example Considerations

This section provides an example for better understanding. A 16-A, 50-Hz AC current shall be measured including it's harmonics plus a 20-mA DC current within the AC. The sensing approach is shunt-based. The size of the shunt is selected to keep power dissipation low, normally well below 1 W. In the example, the shunt is 1 mOhm.

Power dissipation:

$$Ploss = I \times I \times R = 16\,A \times 16\,A \times 1\,mOhm = 256\,mW \quad (1)$$

AC peak voltage across the shunt:

$$Vpeak = I \times R \times \sqrt{2} = 16\,A \times 1\,mOhm \times \sqrt{2} = 22\,mV \quad (2)$$

DC voltage across the shunt:

$$VDC = I \times R = 20\,mA \times 1\,mOhm = 20\,uV \quad (3)$$

Assume an ADC using a 1.2-V VREF with +/-1.2 V full scale swing. For the AC signal, a gain of 54 is required to match full scale. With this gain, the DC voltage results in 1.08 mV. Integrated PGAs inside ADCs normally follow binary gain steps. To avoid clipping one must select a gain of 32; some swing is wasted. At the gain of 32, the AC maximum swing results in a 704-mV peak and the DC maximum is 640 uV. The 640 uV are nearly equal to the LSB size of 585 uV of a 12-bit converter with 1.2V VREF and bipolar +/-VREF swing. Higher resolution converters are needed. Even with a 16-bit converter, the DC resolution is 4-bit only. A 24-bit converter provides more resolution and often contains the PGA. A 50-Hz signal including the 15th harmonic results in 800 Hz analog bandwidth. A typical delta sigma converter using a SINC3 filter has a -3 dB point at $0.262 \times fs$. For the 800 Hz desired bandwidth, one must select a 3.2-ksps sample rate. The input referred noise for such delta sigma converters with adjusted gain is in the single digit uVrms range. In relation to the DC signal amplitude of 20 uV, there is only marginal SNR.

For a better understanding, let's look at the frequency spectrum of the described signal as the result of a coherent FFT calculation. The frequency sample contains 50-Hz wide frequency bins of the fundamental and the harmonic as well as the DC energy.

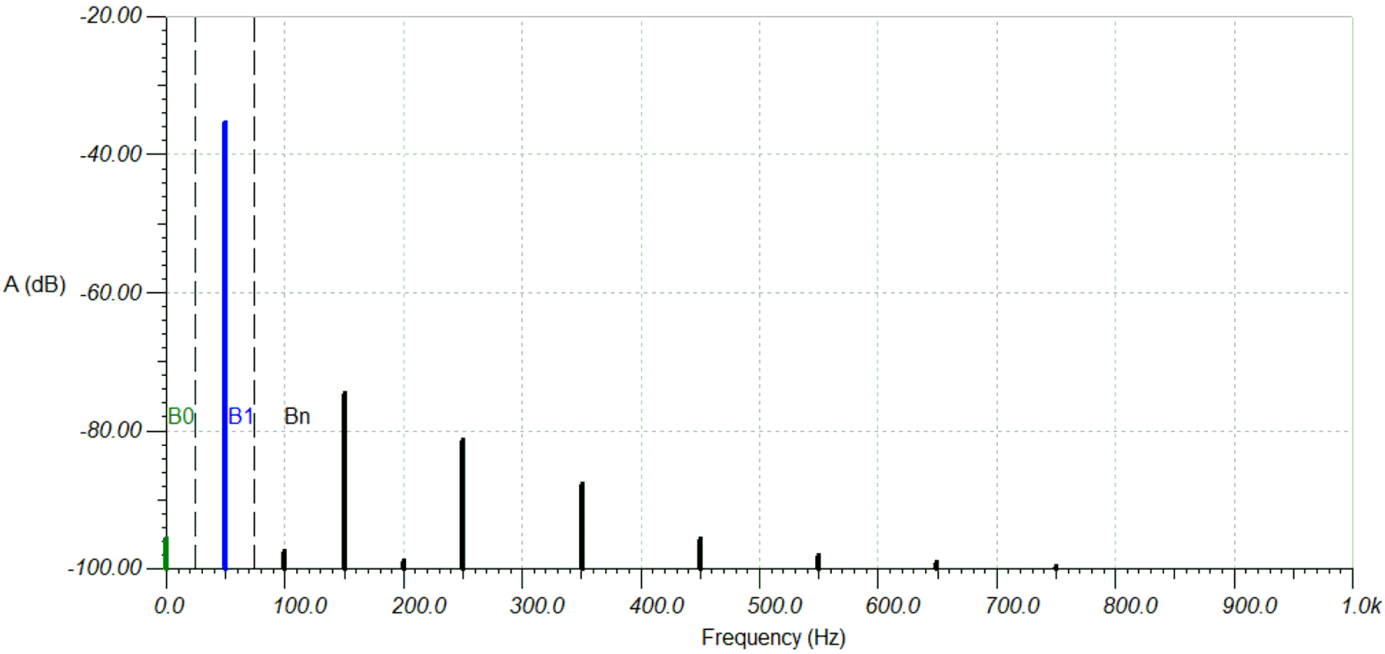

Figure 2-1. FFT DC in AC + Harmonics, VREF=1.2V

B0: DC energy bin

B1: AC fundamental bin

Bn: AC harmonic frequency bins

3 Introducing a Preconditioning Circuit

Improvement of the spectrum is achieved by introducing the ADC gain of 32. For simplicity, only the DC energy and the AC fundamental are considered. The AC harmonics follow the gain of the AC fundamental. The gain corrected spectrum is as follows:

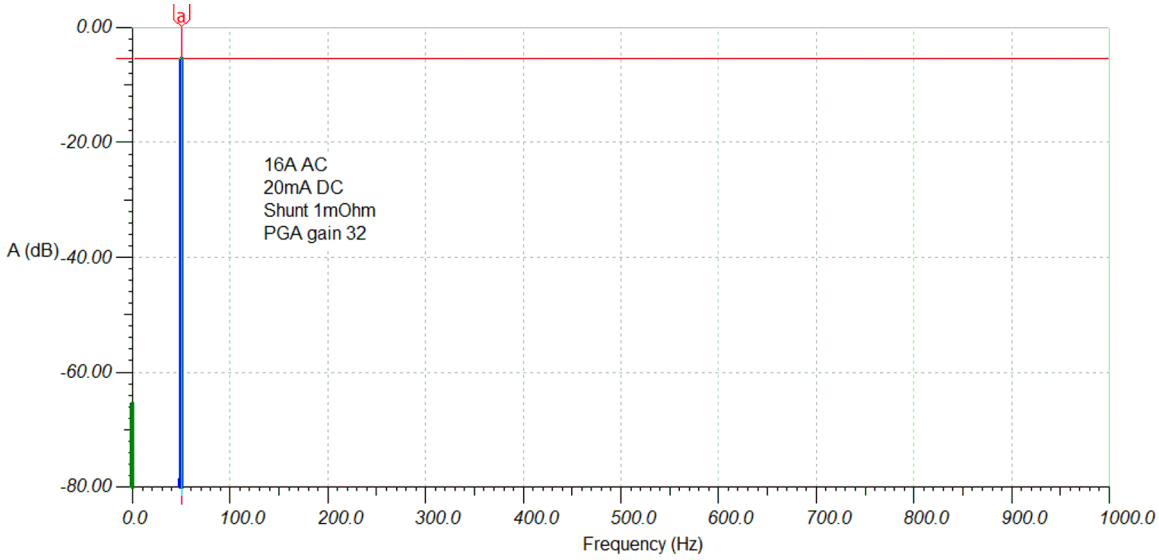

Figure 3-1. FFT DC in AC with PGA Gain = 32, VREF = 1.2 V

To improve the DC in AC sensing and the dynamic range further, introduce a preconditioning circuit in front of the ADC with the following behavior:

- DC gain to amplify the DC value (for example, 8x corresponding to 18 dB)
- AC gain to adjust the AC fundamental to ADC full scale (1.68x corresponding to 4.54 dB)
- Individual DC and AC gain settings
- Flat AC passband already starting at 50 Hz

Such a preconditioning circuit brings the AC fundamental to full scale. The even higher gain for the DC energy increases the DC value by a higher factor and so reduces the required dynamic range and improves the DC energy bin SNR.

3.1 First Order Shelving Filter

The preconditioning requirements can be targeted with a shelving filter. The easiest approach is a first order circuit. As we are gaining up low frequencies and are dealing with small signals, a low noise OPAMP with auto-zero technology was selected, OPA387. Due to the auto zero feature, the OPAMP removes the 1/f noise and has a flat noise power spectral density of only 8 nV/sqrt(Hz). The circuit further incorporates a matching resistor divider at the non-inverting input to reduce the Ib current based offset error. The shown filter structure is an inverting structure. The output polarity is reversed.

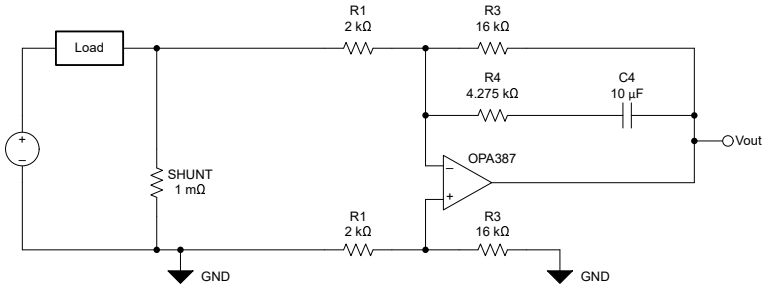

Figure 3-2. First Order Shelving Filter Circuit

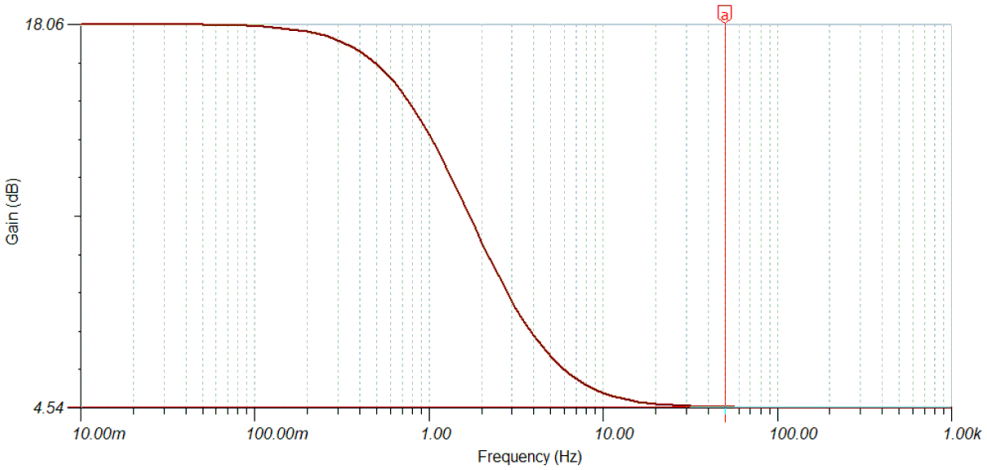

Figure 3-3. Frequency Response of the First Order Shelving Filter

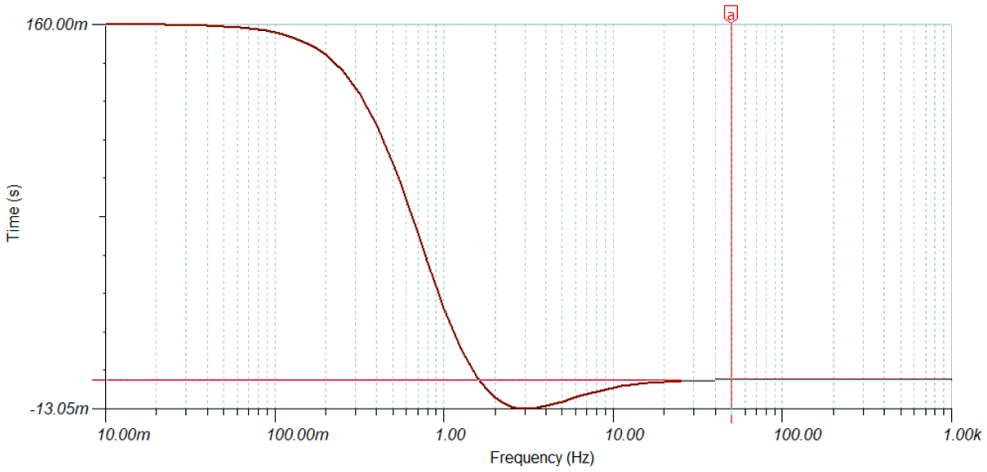

Figure 3-4. Group Delay of the First Order Shelving Filter

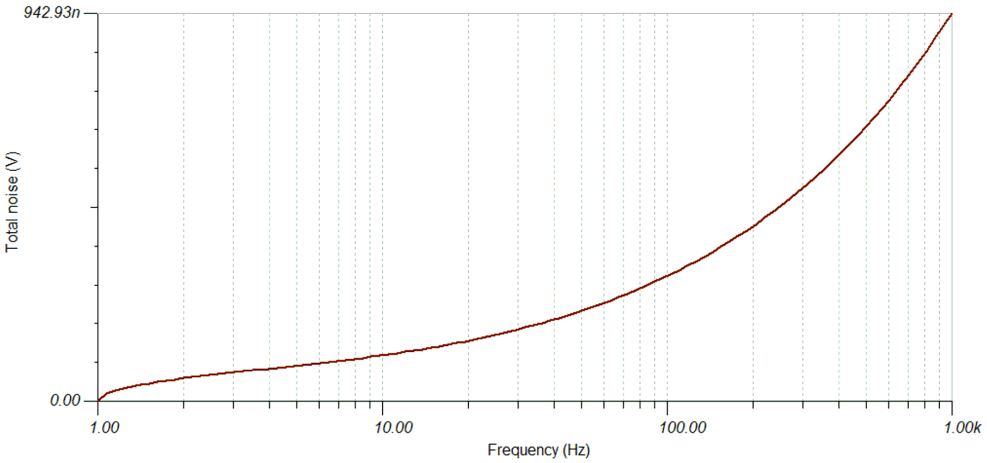

Figure 3-5. Total Output Noise of the First Order Shelving Filter

Looking at the group delay of such filter, one can see that the response time for detecting a DC failure is about 160 ms. For many applications, 160 ms is not acceptable.

3.2 Second Order Shelving Filter

Improvements can be achieved by introducing the suggested second order shelving filter. Due to the additional pole, a much faster group delay at DC can be achieved in the range of 20 ms. The frequency plot indicates a smaller transition band between DC and AC allowing to position this at a higher frequency closer to the AC passband and to detect the change in DC (wander) much faster. Again, the circuit incorporates a matching resistor divider at the non-inverting input to reduce the Ib current based offset error. The shown filter structure is an inverting structure. The output polarity is reversed.

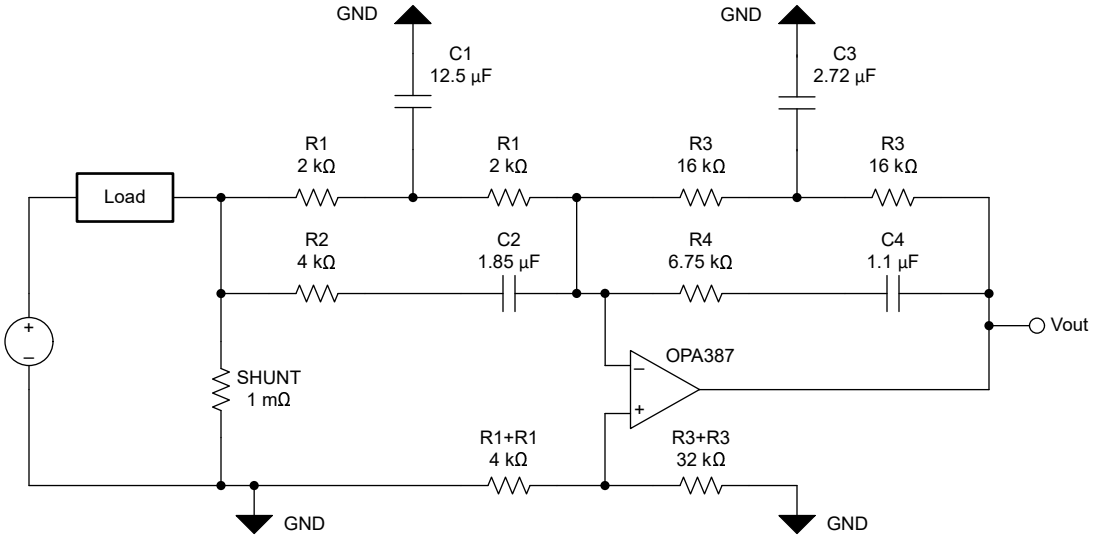

Figure 3-6. Second Order Shelving Filter Circuit

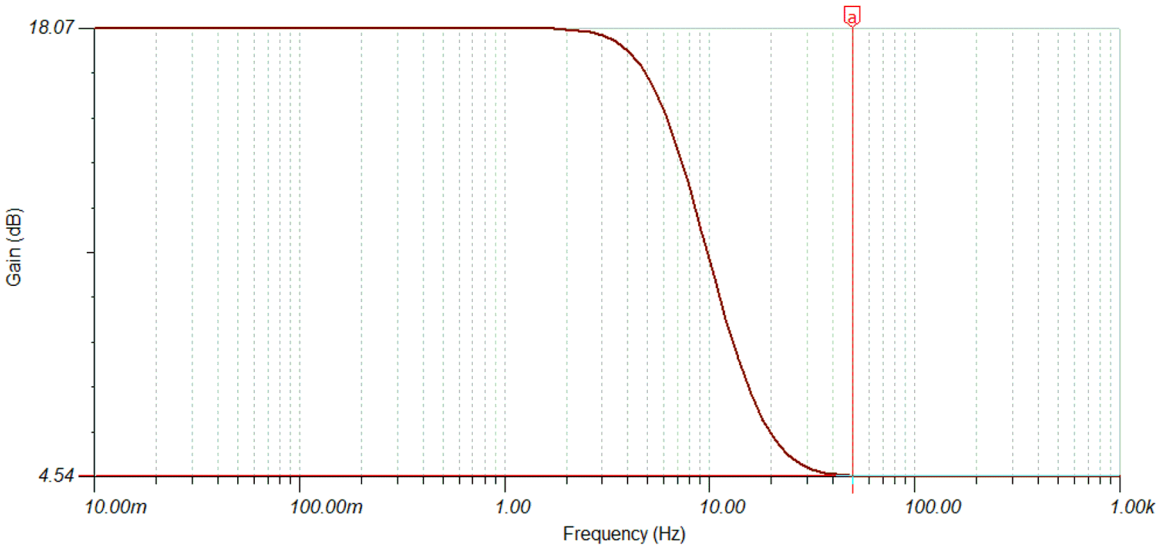

Figure 3-7. Frequency Response of the Second Order Shelving Filter

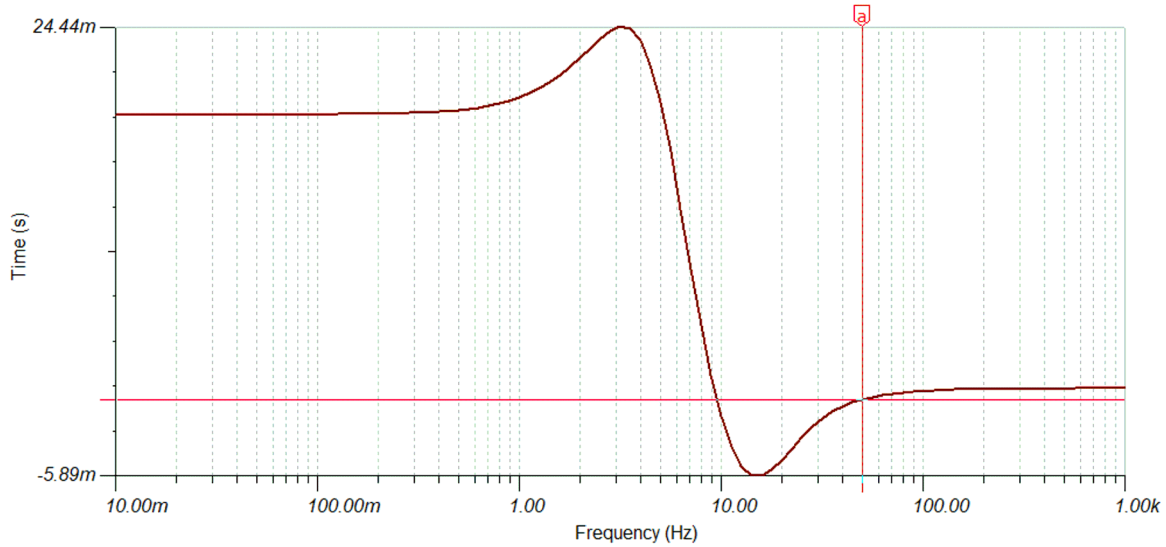

Figure 3-8. Group Delay of the Second Order Shelving Filter

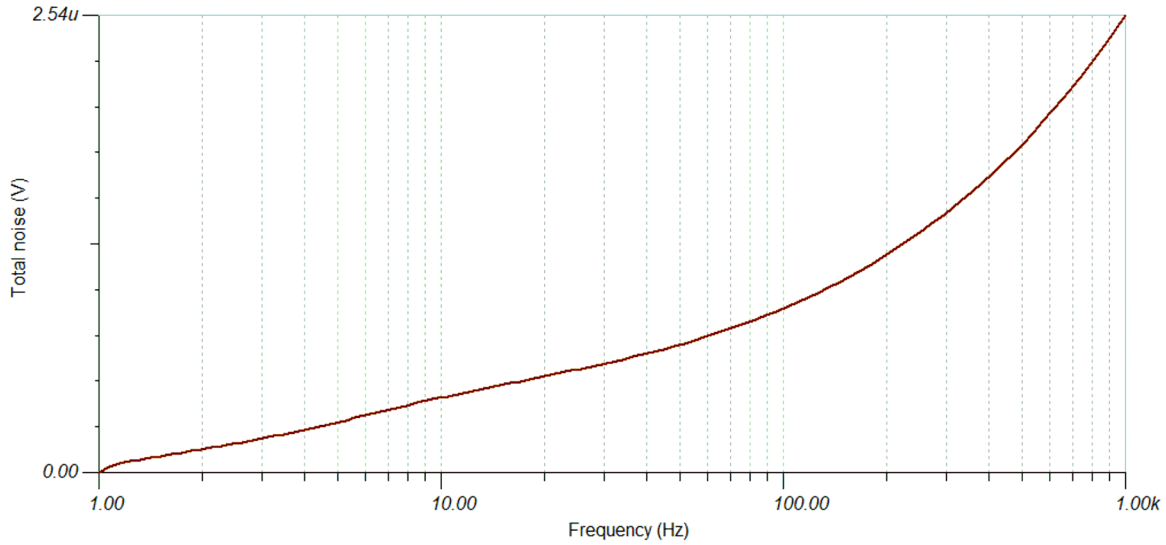

Figure 3-9. Total Output Noise of the Second Order Shelving Filter

3.3 Noise Contribution of the Second Order Shelving Filter

The second order shelving filter comes at the penalty of more components and a slightly higher total noise due to the additional components. When selecting the component values, a compromise between the resistor value, capacitor value, and the total noise must be found. How the noise is distributed in the frequency spectrum is of interest. If FFTs are computed with 50 Hz wide frequency bins, the noise energy in the particular frequency bin matters. When sampling a system, the spectrum becomes periodic with the sampling frequency. From this sampling frequency, energy aliases back to the B0 bin. Therefore, the average noise in the B0 frequency bin was also computed with 50-Hz bandwidth. As expected due to the higher DC gain, the noise contribution in the DC band is the highest. From the plot below, we can estimate the output noise for the individual frequency bins. Again, B0 is the DC energy bin, B1 the AC fundamental bin, and Bn the AC harmonic bins.

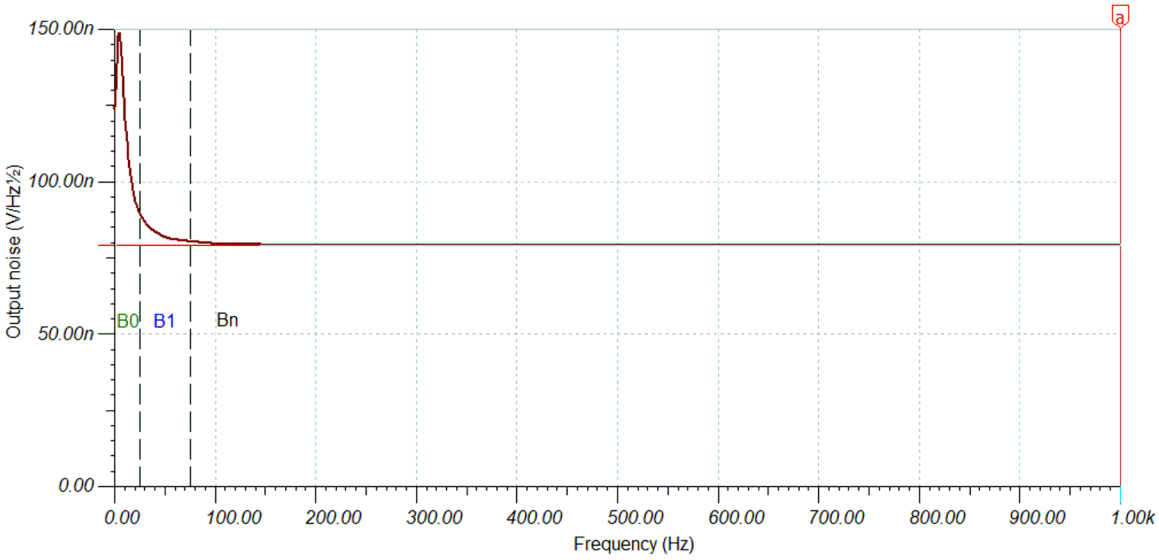

Figure 3-10. Noise Power Spectral Density Distribution Across FFT Bins

$$N\_B0 = \frac{120\ nV}{\sqrt{Hz}} \times \sqrt{50\ Hz} = 848\ nV \quad (4)$$

$$N\_B1 = \frac{83\ nV}{\sqrt{Hz}} \times \sqrt{50Hz} = 586\ nV \quad (5)$$

$$N\_Bn = \frac{79\ nV}{\sqrt{Hz}} \times \sqrt{50\ Hz} = 559\ nV \quad (6)$$

The output noise in the DC energy bin is approximately 1.6x higher than in the AC bins, but as we increase the DC signal content by a factor of 8x (18 dB), this increase still results in an improved SNR of 14 dB (5x) for the small DC signal.

3.4 DC and AC Gain

With the additional gain in the DC (+18 dB) and AC (+4.54 dB) bands, the ADC input receives a DC value of 160 uV and an AC value of 37.125 mV. With a PGA gain of 32, the DC value compared to the 1.2-V VREF results in +/-5.12 mV and the AC value reaches full scale +/-1.2 V.

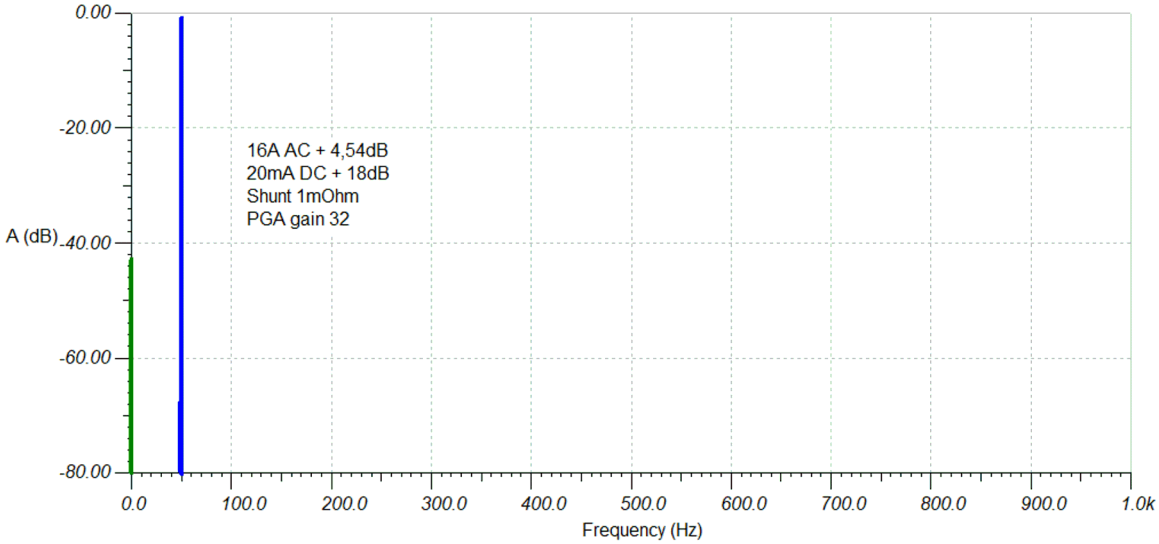

Figure 3-11. FFT DC in AC With PGA Gain = 32 and Filter Correction, VREF = 1.2 V

4 Design Procedure for the Second Order Shelving Filter

The second order shelving filter can be described by the following Laplace polynomial:

$$G(s) = -\frac{\left[s^2C_2C_1R_1R_1 + s(C_2R_2 + 2C_2R_1) + 1\right](sC_3R_3 + 2)(sC_4R_4 + 1)}{\left[s^2C_4C_3R_3R_3 + s(C_4R_4 + 2C_4R_3) + 1\right](sC_1R_1 + 2)(sC_2R_2 + 1)} \times \frac{R_3}{R_1} \quad (7)$$

$$G(s) = -\frac{[S_{0x12}][S_{03}][S_{04}]}{[S_{px34}][S_{p1}][S_{P2}]} \times gain \quad (8)$$

4.1 Definition of Boundary Conditions

The pole zero plot contains fist order poles and zeros as well as two complex second order poles and zeros.

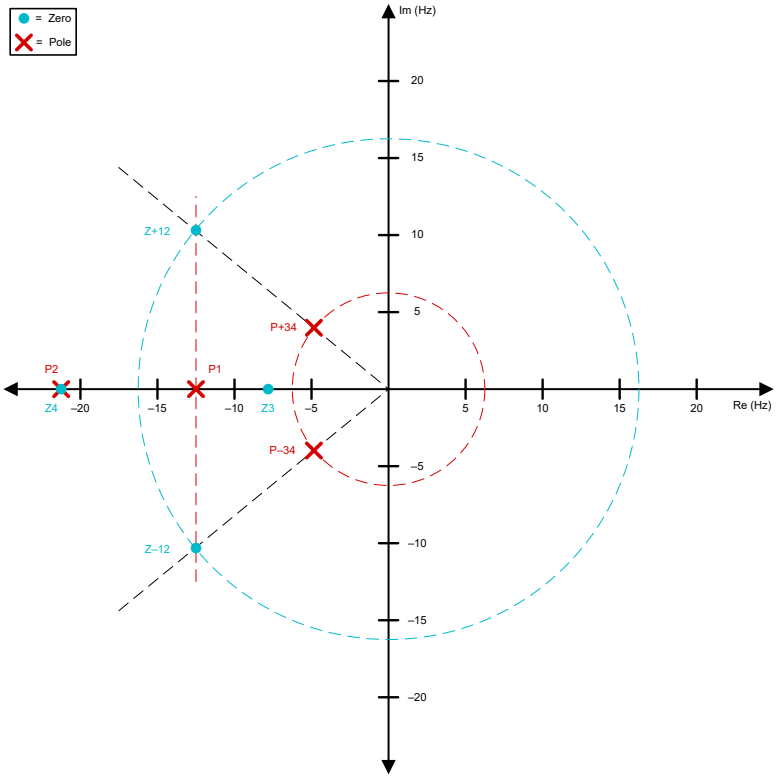

Figure 4-1. Pole-Zero-Plot of the Second Order Shelving Filter

For simplification we define:

$$Q_{0x12} = Q_{px34} = \frac{R_1}{(R_2 + 2R_1)}\sqrt{\frac{C_1}{C_2}} = \frac{R_3}{(R_4 + 2R_3)}\sqrt{\frac{C_3}{C_4}} \quad (9)$$

$$\varepsilon_{p1} = \varepsilon_{0x12} = -\frac{2}{C_1R_1} = -\frac{(C_2R_2 + 2C_2R_1)}{2C_2C_1R_1R_1} \quad R_2 = 2R_1 \quad (10)$$

$$\varepsilon_{p2} = \varepsilon_{04} = -\frac{2}{C_2R_2} = -\frac{1}{C_4R_4} \quad (11)$$

$$DC_{gain} = -\frac{R_3}{R_1} \quad (12)$$

$$AC_{gain} = -\frac{R_4}{R_2} = -\frac{C_2}{C_4} \quad (13)$$

4.2 Calculation of Component Values

Start values:

$$DC_{gain};\ AC_{gain};\ f_{p1};\ Q \geq 0.5;\ R_1;\ C_1 \tag{14}$$

1. Select f_{p1} (for example, 1/4th of lowest AC frequency); example 50 Hz AC to 12.5 Hz
2. Select $Q = 0.65$ for maximum gain flatness
3. Select C_1 based on component restrictions (large C)
4. Calculate R_1 based on the desired f_{p1} and component restrictions (small R)
5. Trade of large C versus small R for best noise

$$R_1 = \frac{2}{2\pi f_{P1} \times C_1} \tag{15}$$

6. Calculate R2:

$$R_2 = 2R_1 \tag{16}$$

7. Calculate R3:

$$R_3 = DC_{gain} \times R_1 \tag{17}$$

8. Calculate R4:

$$R_4 = AC_{gain} \times 2R_1 \tag{18}$$

9. Calculate C2:

$$C_2 = \frac{C_1}{(4Q)^2} \tag{19}$$

10. Calculate C3:

$$C_3 = \frac{C_1}{AC_{gain} \times \left(\frac{2 \times DC_{gain}}{DC_{gain} + AC_{gain}}\right)^2} \tag{20}$$

11. Calculate C4:

$$C_4 = \frac{C_1}{AC_{gain} \times (4Q)^2} \tag{21}$$

5 Influence of Component Tolerances

The component tolerances have to be taken into account when using discrete components to realize a filter. Simulations have been performed to understand the error contribution and the sensitivity of the circuit. In a first simulation, all resistor were selected with 1% tolerance and all combination cases plotted. The result is a worst case error contribution in the DC and AC pass band of about +/-0.2 dB. This contribution is equivalent to +/-2.4% gain error. In a second simulation, all capacitors were selected with 1% tolerance. This tolerance varies the frequency corners and the transition band slightly. For our FFT consideration, note how much gain error this adds to the DC or 50-Hz AC bin. The error contribution is in the range of +/-0.05 dB at 50 Hz which is equivalent to +/-0.6% gain error.

Those deviations can be acceptable if a system calibration can be performed. Care must be taken for the drift of the passives and, if needed, more accurate components must be selected.

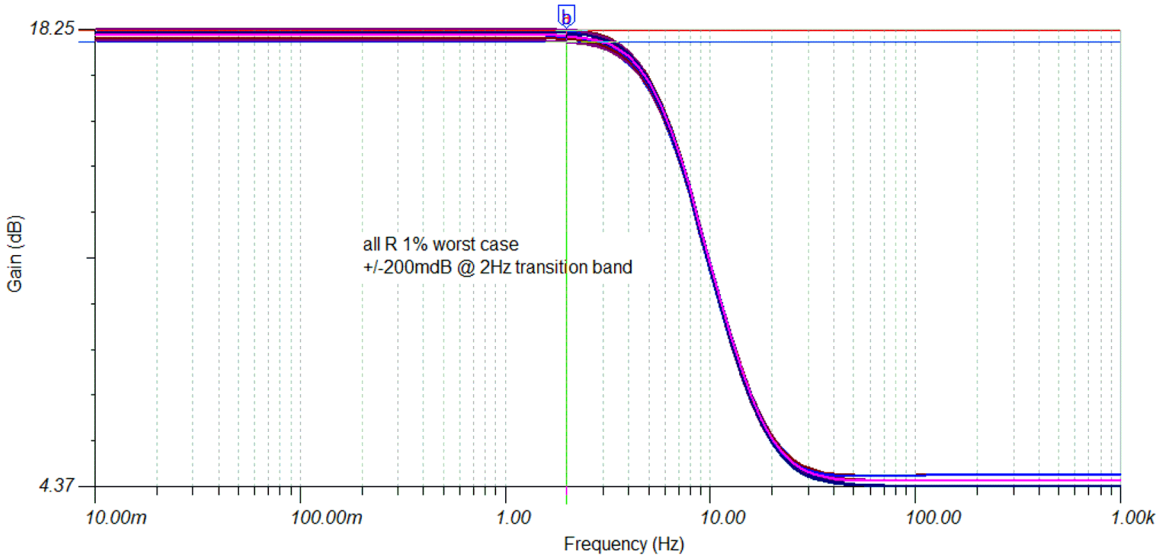

Figure 5-1. Frequency Response Worst Case Deviation With All R = 1%

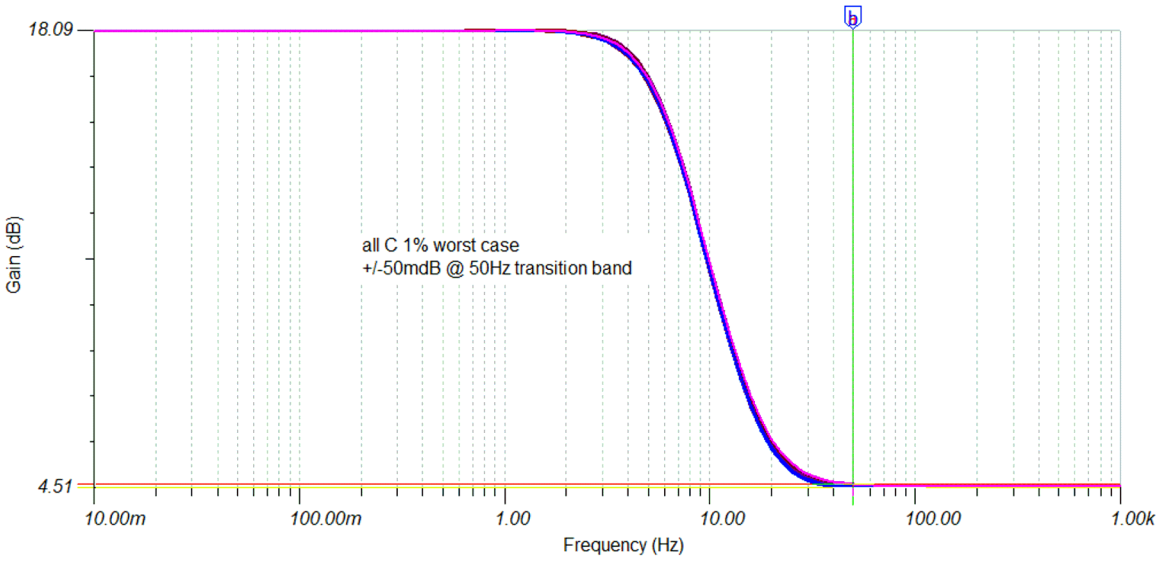

Figure 5-2. Frequency Response Worst Case Deviation With All C = 1%

6 Summary

The second order shelving filter offers the option to individually set the DC gain and the AC gain of a preconditioning circuit in front of an ADC when measuring current with shunts. The small voltages can be increased to improve the DC value amplitude and at the same time to adjust the AC value to full scale range. This increase reduces the dynamic range needed in the system. Due to the second order system, a much smaller group delay for the DC range can be achieved and the time to detect a DC fault reduced. For lowest error and minimal noise contribution, an auto-zero op amp must be selected like OPA387. With no 1/f noise contribution of such auto-zero op amp, the SNR within the DC energy bin can be improved.

7 References

- Texas Instruments, OPAx387 Ultra-High Precision, Zero-Drift, Low-Input-Bias-Current Op Amps data sheet.
- Texas Instruments, TINA-TI simulation tool.

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