Application Note
Impact of Current Noise in CMOS and JFET Amplifiers

TEXAS INSTRUMENTS

Art Kay, Gerardo Rivera Jr.

ABSTRACT

This application note looks at how current noise impacts the total system noise, and when it is a concern. The emphasis is on low current circuits where current noise is less than 10fA/$\sqrt{Hz}$. This application note uses simulations and basic calculations to explain the role current noise, source impedance, and parasitic capacitance have on current noise. A simplified explanation describing the device level origin of the noise is also covered. Finally, methods used to measure this noise as well as practical board level precautions for current noise are covered.

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1 Introduction

The input of all op amps have current noise sources as shown in Figure 1-1. The current noise will translate into voltage noise when it flows through the source impedance ($e_n = i_n R_s$). The source impedance itself will generate a thermal noise voltage proportionate to the source impedance. This thermal noise is given by Johnson's equation $e_n = \sqrt{4kTR_s}$. Current noise is a concern when it translates into a larger voltage noise than the thermal noise of the source impedance ($i_n R_s \geq \sqrt{4kTR_s}$).
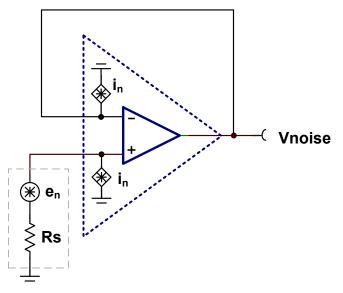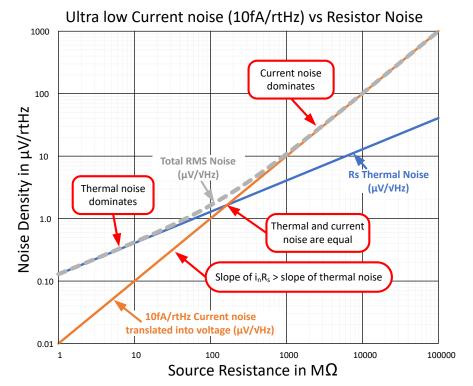

Figure 1-1. Current Noise Source and Voltage Noise Source

Both the current noise and voltage noise relationships are dependent on source resistance, so it is possible to plot current noise, thermal noise, and total noise versus source resistance. Note that thermal noise increases proportionate to the square root of resistance, whereas when current noise translates to a voltage it is directly proportionate to source resistance. Thus, current noise will increase at a faster rate than voltage noise with increasing resistance. Figure 1-2 shows current noise, voltage noise, and total noise versus source impedance for a 10fA/√Hz current noise source. Note that for low resistance values thermal noise dominates and at higher resistance values the current noise dominates. For any level of current noise there will always be a value of resistance above which the current noise will dominate because the slope of current noise is greater than the slope of voltage noise.

Table 1-1 shows the resistance where thermal and current noise are equal for different current noise sources. In this table, if the source resistance is less than the specified resistance, the impact of the current noise on overall noise is negligible. In general, if $R_s > 4kT/(i_n)^2$ then current noise will dominate.

Figure 1-2. Comparing Current and Thermal Noise Components in Total Noise

Table 1-1. Source Resistance Where Current and Voltage Noise are Equal

Current Noise	Source Resistance	Total Noise Density
0.1fA/√Hz	1.65 TΩ	233uV/√Hz
1fA/√Hz	16.5 GΩ	23.3uV/√Hz
10fA/√Hz	165 MΩ	2.33uV/√Hz
100fA/√Hz	1.65 MΩ	232nV/√Hz
1pA/√Hz	16.5 kΩ	23.2nV/√Hz
10pA/√Hz	160Ω	2.33nV/√Hz

2 Current Noise Versus Frequency

Sometimes amplifier data sheets provide a plot for current noise density versus frequency, and in other cases current noise is specified in the specification table at a particular frequency. Generally, the plot of current noise versus frequency is given for devices where the current noise is larger in magnitude and has a flicker region. Figure 2-1 illustrates a typical bipolar device where the current noise is in hundreds of femtoamps and has a flicker region.
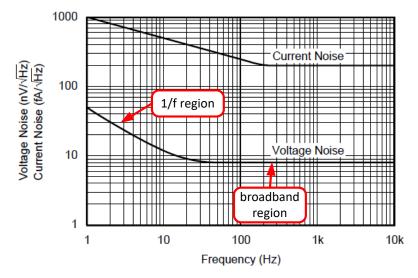

Figure 2-1. Current and Voltage Noise Density for a Typical Bipolar Device OPA277

Devices with low current noise generally give the noise in the specification table, but in some cases provide a graph of current noise versus frequency. Figure 2-2 illustrates a CMOS device where current noise density is provided versus frequency. Note that at low frequency the current noise is only 5fA/$\sqrt{\text{Hz}}$, but at about 2kHz the noise starts to increase. This increase in current noise is sometimes called blowback or f-squared noise. F-squared noise gets its name because the slope of the power spectrum is equal to f-squared in this region. This increase in noise is related to internal amplifier noises sources that interact with the amplifier input capacitance. To understand the increase, consider that capacitive reactance of the input capacitors will decrease with frequency translating to higher current noise (for example, $i_n = e_n/X_c$, where X_c decreases with frequency).
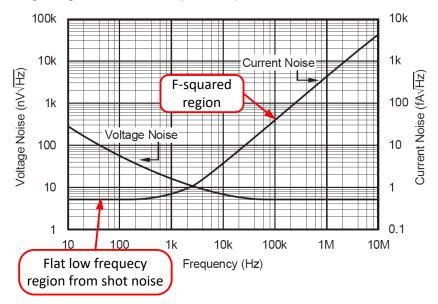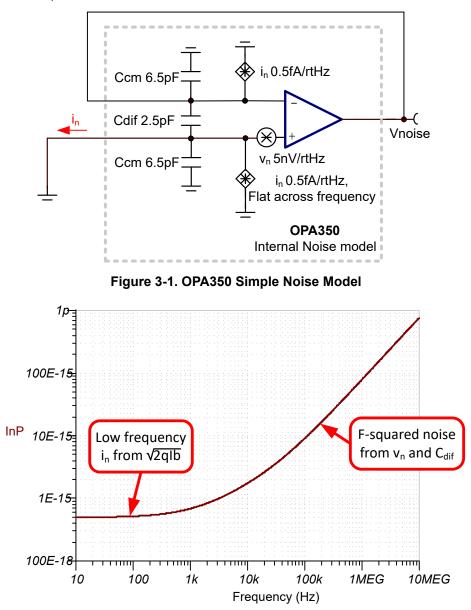

Figure 2-2. Current and Voltage Noise Density for a Typical Bipolar CMOS OPA350

3 How the SPICE Model Sets Current Noise

CMOS and JFET devices are often selected for their very low bias current and low current noise. However, in cases where current noise is specified versus frequency you might see the f-squared noise as shown in Figure 2-2. If low current noise was a key requirement in the design, the increased current noise at high frequency can be concerning. It is important to understand that all CMOS and JFET devices will have this effect so some extent, but it might not be specified. Typically, the amplifier model will show the f-squared noise as it is automatically generated when the amplifier voltage noise interacts with the input capacitance. Thus, you can generally use the model to estimate the impact of f-squared noise. Figure 3-1 illustrates a simple op amp model that uses current noise sources, a voltage noise source, input capacitance, and amplifier open loop gain. Note that this model uses current noise sources that are flat across frequency and the f-squared noise occurs as an interaction between the voltage noise source and differential input capacitance. If comparing the current noise simulation to the data sheet noise plot shown in Figure 2-2, shows that they are very similar but the data sheet noise is slightly higher. This can be due to additional sources of f-squared noise inside the device. Thus, in some cases the actual device can have some current noise not included in typical models. Also, the low frequency current noise is from the shot noise of the input leakage current on the ESD structures or any other semiconductor junction ($\sqrt{2qI_b}$).

Figure 3-1. OPA350 Simple Noise Model

Figure 3-2. Current Noise vs. Frequency for Simple Noise Model

4 Impact Current Noise has on a Non-inverting Amp With Large Source Impedance

Generally, the f-squared noise is a concern for systems with large source resistance or large feedback resistance. Doing a simple analysis using your source impedance can lead you to believe that the f-squared current noise will translate to a large voltage noise. However, to fully understand the system performance you need to look at all the parasitic capacitance. Frequently, the parasitic are ignored because they are in the picofarad range and generally do not have a significant performance impact. However, in this case the source impedance is large and comparable to the capacitive reactance of the parasitic.

For example, the consider the OPA350 with a 100MΩ source impedance. At low frequencies this device has a current noise of 0.5fA/√Hz. Considering Table 1-1, the low frequency current noise must be negligible with a 100MΩ source impedance, but higher frequency current can be a concern as current noise increases to hundreds of femtoamps. The model for this circuit is shown in Figure 4-1. In this figure, the current noise sees a current divider. Some of the current will flow into the common mode capacitance and some will flow into the source. Furthermore, the source resistance generates a noise current which depends on the common mode capacitance. Keep in mind that the reactance of the common mode capacitance is significantly smaller than source resistance at higher frequencies (at 1kHz, $X_c = 1/(2\pi(1kHz)(6.5pF)) = 24M\Omega$). Thus, from a current divider perspective most of the current will flow in the common mode capacitance. Also note that any PCB parasitic capacitance on the non-inverting input will be in parallel with C_{cm} and will further reduce the reactance $[X_{ccm} = 1/(2\pi f(C_{cm} + C_{par}))]$.
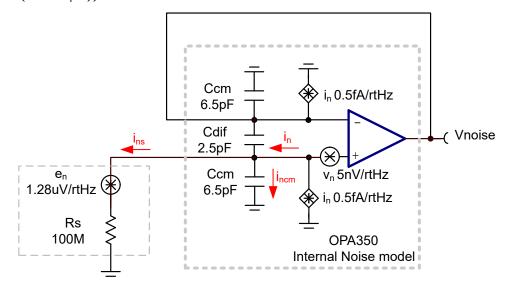

Figure 4-1. Noise Model for OPA350 with Large Source Impedance

For a better understanding of the interaction between the various sources and impedance in this circuit, it is useful to use superposition. First, look at the impact of the source resistor noise. Rs and the reactance of C_{cm} form a low pass filter. The noise voltage at the input of the amplifier will roll off at 245Hz ($f_c = 1/(2\pi R_s C_{cm}) = 245Hz$). You can also consider that this noise voltage creates a noise current of $i_{Rs} = e_{nr}/\sqrt{(R_s)^2 + (X_{ccm})^2}$ (see Figure 4-2)
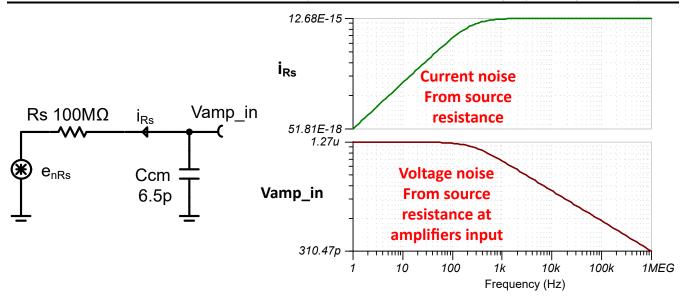
Figure 4-2. Impact of Noise From Source Resistance on Amplifier Input

Considering the noise current from the amplifier (i_n) will flow from the amplifier into a current divider with the reactance of C_{cm} in parallel with R_s. Notice that at low frequencies the current noise flowing through the resistor is the same as the current from the amplifier. However, at higher frequencies the capacitive reactance of the common mode capacitor is small in comparison to the source resistance so most of the current from the amplifier flows through C_{cm}.

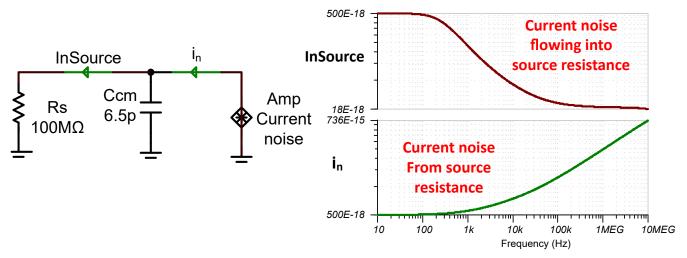**Figure 4-3. Amplifier Current Noise Current Divider Effect**

Figure 4-5 illustrates the overall noise for the OPA350 with a 100 MΩ source impedance. Notice that the output noise curve at low frequencies is mostly the thermal noise of the resistor. This makes sense according to Table 1-1, as the current noise at low frequency is 0.5fA/√Hz and 100 MΩ is low enough to minimize the impact of this low-level current noise. At higher frequencies however, you can expect the current noise to be more problematic as the noise is over 100fA/√Hz at 1MHz. However, this increase in current noise at higher frequencies is not seen by the load as the impedance of the common mode capacitor is small compared to the source impedance, so most of the current will in the common mode capacitance. In fact, the noise current flowing through the source impedance is mainly the thermal noise of the impedance ($i_{np} \approx e_{nr}/R_s = 1.28\mu V/100M\Omega = 12.8fA/rtHz$). Finally, notice that the amplifier output noise starts to roll-off at approximately 100Hz. This is because of the low pass filter formed by the source impedance and the common mode capacitance ($f_c = 1/(2\pi R_s C_{cm}) = 245Hz$). Thus, the noise as well as any input signal will be attenuated by the filter from the source impedance and common mode capacitance.
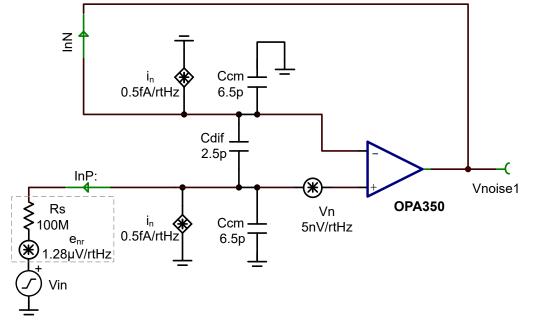
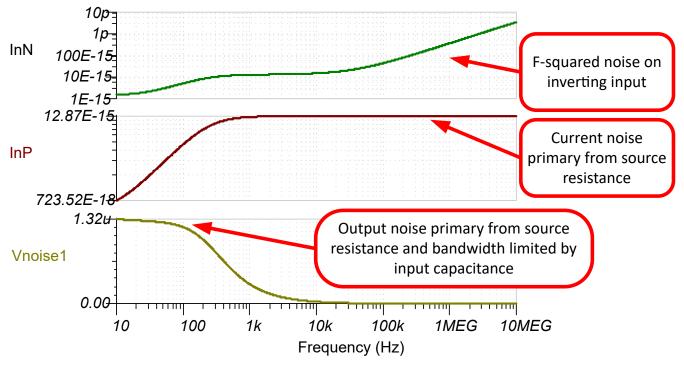**Figure 4-4. Schematic for Non-inverting OPA350 With 100 M Source Impedance**

Figure 4-5. Noise Simulation with 100 MΩ Source Resistance

5 Impact of Current Noise has on the Transimpedance Configuration

The previous section showed an example where a large source impedance is connected to the non-inverting amplifier input. A Ph sensor is a common example of a sensor that is normally connected to the non-inverting input and has impedance ranging from 10MΩ to 1000MΩ. The transimpedance amplifier is another common configuration that uses large impedance and considers current noise as an important error source. The most common application for a transimpedance amplifier is to translate the output current from a photodiode to a voltage. In many cases the photodiode current can be very low level, so a large feedback impedance is required.

In the case of the transimpedance amplifier, the amplifiers bandwidth is also severely limited with a large feedback resistor. The bandwidth of the current gain (V_{out}/i_{in}), is limited to 1.59kHz in this example ($f_c = 1/(2\pi R_f C_f) = 1.59 kHz$). Note that Cf is a combination of the parasitic capacitance of the feedback resistor and any external capacitor added. For the transimpedance amplifier some amount of feedback capacitance is required for amplifier stability. As with the non-inverting configuration, the bandwidth limit will roll-off the noise and signal gain long before the f-squared noise begins, so the f-squared noise cannot be seen in the output spectrum.
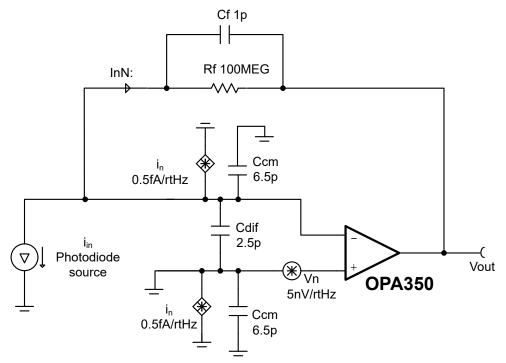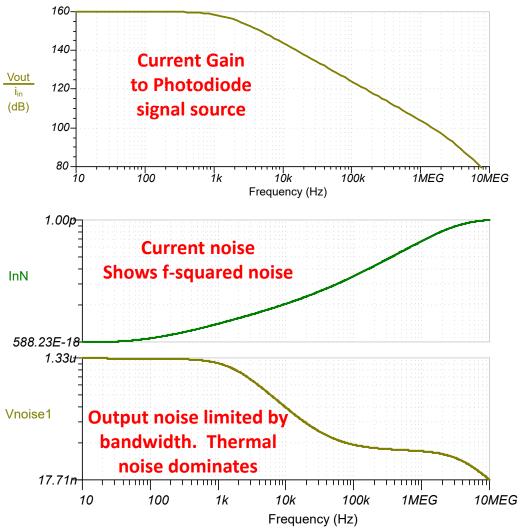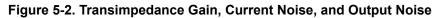

Figure 5-1. Transimpedance Amplifier Noise Model

Figure 5-2. Transimpedance Gain, Current Noise, and Output Noise

In comparing to the noninverting case, the current noise was divided between the source impedance path and the common mode and parasitic input capacitor path. However, in the case of the transimpedance amplifier, all the current noise is forced to flow through the feedback resistor. That is, for any current developed in the parasitic capacitance on the inverting node, an equal and opposite current will flow through the feedback network. Any additional parasitic capacitance on the inverting node will cause the f-squared noise to increase for the transimpedance amplifier. This capacitance on the inverting input will not directly impact the signal bandwidth but from a practical perspective this capacitance will need to be counterbalanced by increasing the feedback capacitor for amplifier stability. Increasing the feedback capacitor on the transimpedance amplifier will reduce bandwidth. On the other hand, increasing the parasitic capacitance non-inverting input will direct reduce the bandwidth for non-inverting amplifiers. The key point is that the non-inverting amplifier will has a slight advantage over the transimpedance amplifier from a current noise perspective. Figure 5-4 illustrates a comparison between the transimpedance and non-inverting configuration for total RMS noise.
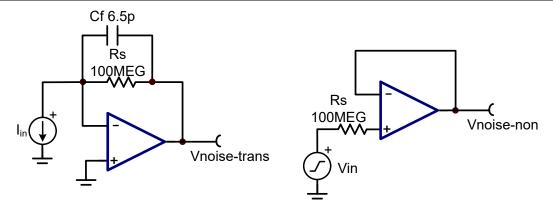
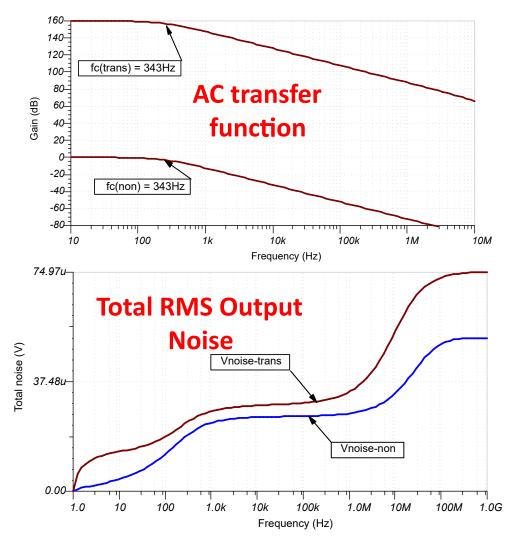Figure 5-3. Schematic for Comparing Inverting and Non-inverting Configuration

Figure 5-4. Comparing Transfer Function and Noise for Inverting and Non-inverting

6 Current Noise Correlation

In noise analysis noise sources are typically considered to be random and uncorrelated. For this reason, two noise sources will add as the square root sum of the square (RSS). Equation 1, shows how two random uncorrelated noise sources add. For two completely independent circuit elements you can assume that the noise will be uncorrelated. For example, the noise on two separate resistors will be uncorrelated. However, if a single noise source is coupled through different paths, the noise at the output of each path will be correlated to each other. For example, if a single noise source connects to two different amplifiers, the noise at the output of the amplifiers will be correlated to each other. Equation 2 shows how correlated noise sources add. The correlation factor indicates the degree to which the signals are correlated. If two signals have an identical wave shape they are directly correlated and the correlation factor is +1.0. The equation for this case simplifies to directly adding the two signals to each other ($e_{nTotal} = e_{n1} + e_{n2}$). On the other hand, when two signals have identical wave shape but one is inverted relative to the other, they are inversely correlated and the correlation factor is -1.0. The equation for this case simplifies to directly subtracting the two signals from each other ($e_{nTotal} = |e_{n1} - e_{n2}|$).

$$e_{nTotal} = \sqrt{e_{n1}^2 + e_{n2}^2} \tag{1}$$

e_{n1}, e_{n1} are random and uncorrelated noise sources

Where

e_{nTotal} is the combination of these signals

$$e_{nTotal} = \sqrt{e_{n1}^2 + e_{n2}^2 + 2Ce_{n1}e_{n2}} \tag{2}$$

Where

e_{n1}, e_{n1} are random noise sources

e_{nTotal} is the combination of these signals

C is the correlation factor ranging from -1.0 to +1.0

From an amplifier current noise perspective, there are some cases where the current noise may be correlated. Depending on the internal amplifier design, there may be a common voltage noise source that will couple to the amplifier inputs via the gate to source capacitance. Since this noise couples through capacitance, it acts as an f-squared noise component. In this case, the noise on both inputs originates from the same bias circuitry, so the noise is directly correlated. Matching the impedance, on both the inverting and non-inverting inputs of the amplifier, will translate the current noise into two equal directly correlated voltage noise values. The common mode rejection of the amplifier will effectively subtract the two noise sources from each other and cancel the noise. Of course, any amplifier can have multiple noise sources and not all of the noise will be correlated, so the noise will not completely cancel. Furthermore, many amplifiers will not have any significant correlation in the current noise, so balancing the impedance will not always improve noise.

In general, details on the correlation of noise are not published in amplifier data sheets, so the best way to confirm if balancing the impedance helps is through experimentation. Keep in mind that balancing the impedance can necessarily require adding additional resistors, and the resistors can contain uncorrelated voltage noise. The OPA392 is an example of a device that does have a strong correlation in the current noise.

7 Measuring Low Current Noise Levels

Placing a resistance on the non-inverting input of the op amp will translate current noise to voltage noise. Furthermore, when this resistor is increased so that $R_s > 4kT/(i_n)^2$ then current noise will be the dominant noise source. However, as discussed previously, when R_s is increased to be very large, the noise bandwidth and signal bandwidth of the amplifier is limited, so the increasing current noise from f-squared noise may not be significant. It is, however, possible to mathematically correct for the bandwidth limitations and subtract thermal noise from the source resistor to reveal the current noise over frequency. The following is a procedure that can be used to measure low levels of current noise and correct for the parasitic impedance. Table 7-1 defines the variables used in the test procedure.

1. Select a resistor that according to the bias current of the device. Bias current multiplied by the source impedance will set the DC voltage at amplifiers input. In this example we will choose 10 GΩ. This sets the output offset to 100 mV worst case for OPA350 (IB×Rs = 10 pA×10 GΩ = 100 mV). The low frequency current noise for this device is 0.5 fA/√Hz, so the source resistor maintains that current noise dominates ($R_s > 4kT/(i_n)^2 = 6.59G\Omega$).

2. Calibrate the noise floor of measurement system (for example, spectrum analyzer). This is done by measuring the noise without the amplifier installed. This reading can be subtracted from the noise measurement to correct for the noise floor.

3. Install the amplifier and measure the output noise.

4. The following steps mathematically correct for the thermal noise and for the parasitic impedance from the device and parasitic capacitance.

5. Determine the closed loop gain of the buffer: $G_{cl} = 1/\left[(f/GBW)^2 + 1\right]$

6. Divide output noise by the close loop gain: $e_{nRTI} = e_{nOUT}/G_{cl}$

7. Determine the impedance of the common mode and parasitic capacitance over frequency: $X_{ccm} = 1/\left(2\pi(C_{cm} + C_{par})f\right)$

8. Find the source resistor noise: $e_{nr} = \sqrt{4kTR_s}$

9. Find the source resistor noise at amplifiers input: $e_{nrRTI} = e_{nr}\left(X_{ccm}/\sqrt{X_{ccm}^2 + R_s^2}\right)$

10. Calculate the voltage noise at the amplifiers input from the current noise sources only. Do this by subtracting the amplifier voltage noise and source resistors thermal noise from measured noise RTI: $e_{n\_current} = \sqrt{(v_{nRTI})^2 - (e_{nrRTI})^2 - (e_{nAmp})^2}$. For the OPA320, the amplifier noise is 5nV/√Hz, so the calculation is: $e_{n\_current} = \sqrt{(step6)^2 - (step9)^2 - (5nV/\sqrt{Hz})^2}$. Figure 7-1 shows the results from each step over frequency.

11. Calculate the impedance seen looking from the non-inverting input to ground. This is the impedance that the voltage noise from step 10 sees. This is the parallel combination of the source resistance and reactance of the input capacitance. $Z_{input} = R_sX_{ccm}/\sqrt{X_{ccm}^2 + R_s^2}$

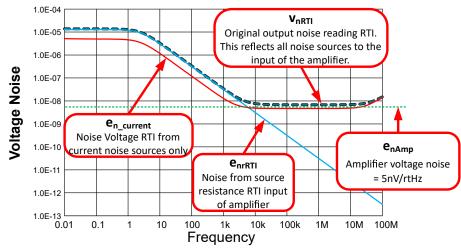12. Calculate input current noise: $i_n = e_{n\_current}/Z_{input}$

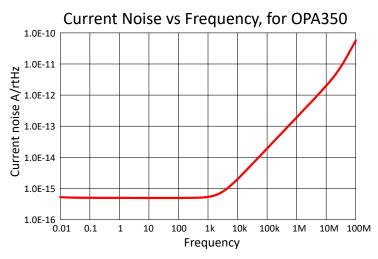**Figure 7-1. Voltage Noise Components Used in Current Noise Calculation**

Figure 7-2. Final Current Noise Based on Measured Amplifier Output Noise

Table 7-1. Variables Used in Measurement Procedure Equations

Variable	Definition
R_s	Source resistance
i_n	Amplifier current noise
G_{cl}	Closed loop gain
GBW	Amplifier gain bandwidth data sheet specification
C_{cm}	Amplifier common mode capacitance
C_{par}	PCB trace parasitic capacitance
X_{cm}	Impedance of the amplifier common mode capacitance and parasitic capacitance
e_{nOUT}	Measured output voltage noise
e_{nRTI}	Measured noise referred to the amplifier input
e_{nr}	Thermal noise of source resistance
e_{nRTI}	Thermal noise of source resistance referred to the input of the amplifier
$e_{n\_current}$	Voltage noise due to amplifier current noise referred to the input
Z_{input}	Impedance seen by amplifier input
i_n	Amplifier current noise

8 Low Current Noise and Bias Current Considerations

Applications requiring low current noise require special precautions to take full advantage of the device specifications. Failing to take these precautions can result is noise levels that are much greater than theory can predict. Note that the same concerns that apply to low current noise circuits also apply to low bias current circuits. Consider that, current noise as the AC variation in the bias current of the device. Any leakage paths tend to have low frequency variations that can create an error source that looks like low frequency noise.

One of the primary concerns for low current noise circuits, relates to the fact this type of circuit can interface with high impedance sensors and can use high impedance feedback networks. These high impedance can be impacted by any parasitic impedance. Normally the impedance of the PCB material between two resistor pins is considered to be effectively infinite. However, solder flux residue and other contaminants can create leakage paths that allow current flow beyond the expected bias current and current noise. For best results it is critical that the PCB is cleaned in an ultrasonic cleaner in accordance with the type of solder flux used. After the cleaning, the board should be baked at elevated temperature to eliminate any residual moisture. Furthermore, the board should be handled using ESD safe gloves or finger cots to avoid contaminating skin oil or other condiments. Avoid breathing on the board as saline moisture in breath can severely degrade performance. The board needs to be stored in a sealed low moisture container with a desiccant pack.

Even if the PCB is kept clean and moisture free, the PCB dielectric material can have some leakage. There is a design method called guarding, that surrounds sensitive nodes with a guard trace driven to the same potential as the sensitive signal trace. Since there is no potential difference between the signal trance and the surrounding guard trace, the leakage currents are minimized.

Besides leakage paths that need to consider interference sources when making low current noise measurements. Since the current levels are extremely low, any small pickup of interference signals can introduce large errors. Typically, a shielded enclosure is required to minimize noise pickup.

Finally, your application can call for very large resistor values (10M through 1T). Low drift precision resistors in this range can be very costly. These resistors are generally physically large through-hole components that can be damaged by improper handling and storage. Furthermore, any physical capacitors placed in parallel with high impedance need to be low leakage type (Polystyrene and Teflon). The reverences at the end of this document provide details on low Ib measurement.

9 Summary

Very low current noises do not impact overall noise performance unless the source impedance is very large. In the case of a 1fA/$\sqrt{Hz}$ current noise, the source resistance needs to be greater than 16.5 GΩ for current noise to make a significant contribution to overall noise. For CMOS and JFET devices, it is common for current noise to increase at higher frequencies. This increase in current noise is called f-squared noise. Circuits where the source impedance is high limit, the bandwidth below the frequency where current noise begins to increase. This bandwidth limitation tends to counterbalance the impact of the f-squared noise so that the total RMS noise is not impacted significantly by the f-squared noise.

10 References

1. EDN, *Design Femtoampere Circuits with Low Leakage, Part 1*, Grohe, P. 2011.
2. EDN, *Design Femtoampere Circuits with Low Leakage, Part 2*, Grohe, P. 2012.
3. EDN, *Design Femtoampere Circuits with Low Leakage, Part 3: Low-Current Design Techniques*, Grohe, P. 2012.

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