Application Brief

Space-Grade, Overcurrent Protection Circuit for TPS7H500x-SP Family of Devices Using the INA901-SP

Carolus Andrews

Design Goals

Input		Overcurrent Conditions	Output	Supply	Total Ionizing Dose	Single Event Immunity
$I_{load\ Min}$	$I_{load\ Max}$	I_{OC_TH}	V_{out_OC}	V_S	TID	SEL
10 A	20 A	21 A	2.1 V	5 V	50 krad (Si)	75 MeV × cm^2 / mg

Design Description

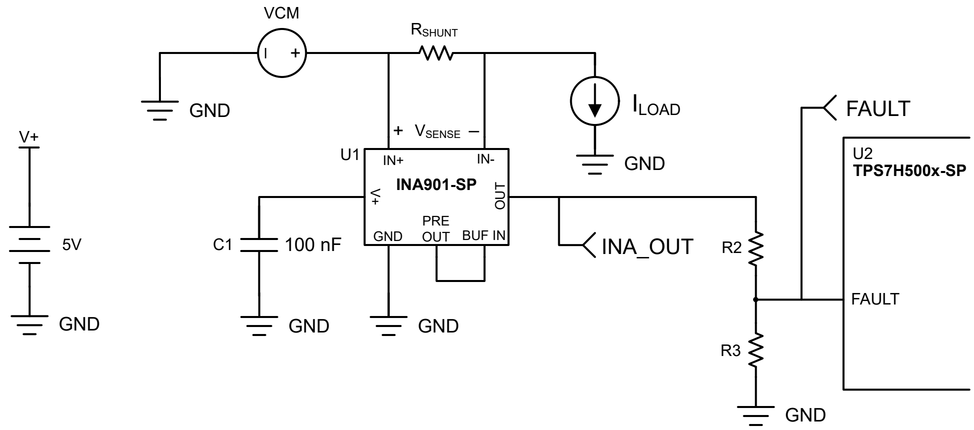
This is a unidirectional current-sensing design, generally referred to as overcurrent protection (OCP) that can provide an overcurrent alert signal to power off a system exceeding a threshold current. In this particular design, the normal operating load is from 10 A to 20 A. The overcurrent threshold for the design triggers when the FAULT pin of the TPS7H500x-SP reaches 0.6 V. The TPS7H500x-SP is a family of PWM controllers that provide a number of features beneficial for the design of DC-DC converter topologies intended for space applications. These devices feature built-in hysteresis, maintaining active shutdown until this value returns below 0.5 V, when active PWM resumed in the system. The full family of TPS7H500x-SP and their various characteristics are listed in the TPS7H500x-SP Device Comparison table.

TPS7H500x-SP Device Comparison

Device	Primary Outputs	Synchronous Rectifier Outputs	Dead-Time Setting	Leading Edge Blank Time Setting	Duty Cycle Limit Options
TPS7H5001-SP	2	2	Resistor Programmable	Resistor Programmable	50%, 75%, 100%
TPS7H5002-SP	1	1	Resistor Programmable	Resistor Programmable	75%, 100%
TPS7H5003-SP	1	1	Fixed (50-ns typical)	Fixed (50-ns typical)	75%, 100%
TPS7H5004-SP	2	0	N/A	Resistor Programmable	50%

To achieve the desired result, the design attenuates the output of the INA901-SP, monitoring the primary, to a precision voltage divider that triggers at the calculated overcurrent point to optimize error in the design against generated heat in the system.

The TPS7H500x-SP operates with a V_{IN} of 4 V to 14 V, while the INA901-SP operates from a single 2.7-V to 16-V supply, allowing for multiple design cases where both devices can operate from the same supply magnitude. For the purposes of this design, the INA901-SP is powered from a single 5-V supply rail. OCP can be applied to both high-side and low-side topologies. The design presented in this circuit is a high-side implementation, with the common-mode voltage (VCM) placed as a representation of an ideal voltage supply between 5 V and 28 V. This circuit is useful for telemetry, health monitoring and system diagnostics surrounding the TPS7H500x-SP. In addition to this functionality, the circuit implements the INA901-SP, which is a Radiation-Hardness-Assured (RHA), 50-krad(Si) capable device at Low Dose Rate, that is also Single Event Latch-up (SEL) Immune to 75 MeV-cm^2 / mg at 125°C. The TPS7H500x-SP family of devices is RHA, 100-krad(Si) capable device at Low Dose Rate, that is also SEL-immune to 75 MeV-cm^2 / mg at 125°C.



Design Notes

1. For accurate overcurrent applications, maintaining a stable power supply with minimized noise and glitches is important. To achieve this, use decoupling capacitor C1 to make sure the device supply is stable. Place the decoupling capacitor as close as possible to the supply pin of the INA901-SP.
2. If additional short-circuit-to-ground protection is needed in the circuit, fuses in series with the input pins can provide this functionality, but do not use resistors for this purpose. Addition of resistors to the input pins of the INA901-SP fundamentally changes the gain of the amplifier. However, the tolerance of the internal resistors fluctuates up to 30% (these resistors are matched to one another, rather than an absolute value), and thus this change in gain varies from device to device, and cannot be considered reliable design.

Design Steps

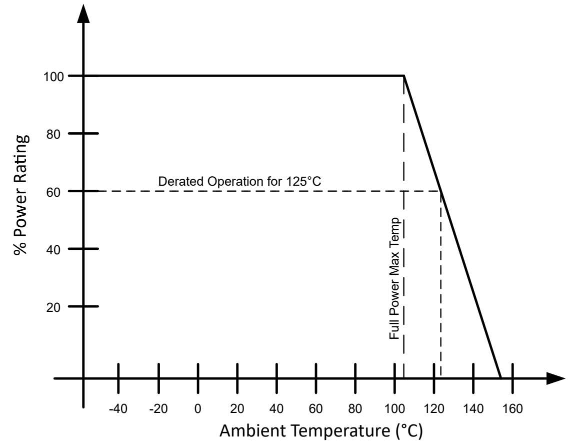
1. **Full Scale Range**: Determine the load range of conditions needing to be monitored. For the purposes of this design example, the load range is defined as 10 A to 20 A, with a desired overcurrent response (I_{TRIP}) occurring at 21 A. Select R_{SHUNT} with respect to the maximum range of current allowable to the input sense voltage, including the overcurrent value. Additional considerations are offset voltage on the lower end of measurement, including contributions from CMRR and PSRR, and power considerations in the shunt at the upper end of measurement. While designing with INA901-SP, for best performance, make sure that the I_{MIN} condition with the chosen shunt produces a sense voltage > 20 mV to comply with the *Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage* section of the *INA901-SP Radiation Hardened, –15-V to 65-V Common Mode, Unidirectional Current-Shunt Monitor* data sheet.
2. **Gain Options**: For the INA901-SP, only a 20 V / V option is available, so this condition is fixed for this design.
3. **Choosing a shunt resistor**: Given the design conditions defined in step 1, choose an appropriate shunt using the following equation. There is a 200-mV reduction on the supply voltage to make sure that the device meets swing-to-rail limitations of the device. Numerical values come from the previously-defined use case:

$$R_{SHUNT} \le \frac{V_{SWING-RAIL}}{I_{TRIP} \times GAIN} = \frac{4.8\ \mathrm{V}}{21\ \mathrm{A} \times 20\frac{\mathrm{V}}{\mathrm{V}}} = 11.43\ \mathrm{m\Omega}$$

The calculated value here is 11.43 mΩ, which is inconvenient from an E-standard manufactured value standpoint. Therefore, a shunt resistor value of 10 mΩ is chosen for the design, which corresponds to a calculated overcurrent point of 4.2 V. However, designing to the output maximum provides more utilization of the full scale range at the tradeoff of thermal constraints increasing proportionally with the resistance. The worst case power dissipation in the shunt resistor is given in the following equation:

$$P_{SHUNT} = I_{max}^2 \times R_{SHUNT} = 21\ \mathrm{A}^2 \times\ 0.01\ \Omega = 4.4\ \mathrm{W}$$

4. **Derating the shunt resistor:** For applications over temperature, power deratings must be taken into account for the chosen shunt. The following image shows a typical power derating curve for a resistor.



Typical Shunt Derating Curve

As the curve demonstrates, the maximum temperature this shunt is able to handle for the maximum rated load is approximately 105°C. For a 125°C application, the shunt is only able to handle 60% of the original rated power rating based on the curve information. From the calculated maximum, this demonstrates the proper choice of power rating of the chosen shunt is shown in the following equation.

$$P_{REQUIRED} > \frac{P_{max}}{Derating} = \frac{4.4\ W}{0.6} = 7.33\ W$$

This calculation shows that if this is the chosen shunt resistor, a product from this data sheet rated for at least 7.33 W needs to be selected to provide shunt survivability at the high end of the specified temperature range. Additional margin can also be added for robustness of this design. These numbers are not a standard for all shunts; these operating points differ from resistor to resistor. The numbers can also include additional data points and criterion such as coverings or heat sinks that allow extended range. See the data sheet of the intended shunt and design to make sure it is adequate for the design.

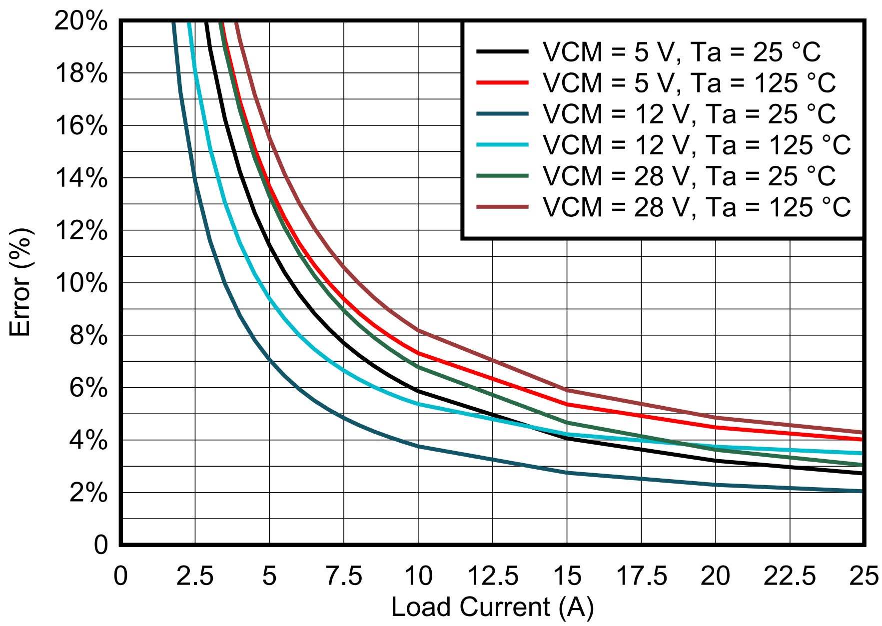
5. **Shifting the overcurrent point to the** TPS7H500x-SP: As determined in step 3, the actual overcurrent point based on the chosen shunt is 4.2 V. The overcurrent voltage must then be attenuated down to 0.6 V for the purposes of the FAULT pin of the TPS7H500x-SP. A simple voltage divider between R2 and R3 accomplishes this. Choose a value of 10 kΩ for R3, and solve the following equation for R2:

$$R_2 = \frac{R_3\left(V_{OUT,\ max} - 0.6\right)}{0.6} = \frac{10\ k\Omega(4.2\ V - 0.6)}{0.6} = 60\ k\Omega$$

Often, calculated resistor values do not directly align with available resistor choices. Here, 60 kΩ is not a standard value, and the closest standard value available is 59.7 kΩ. This choice adds another 0.5% error to the OCP point, and a design choice needs to be made whether this error is acceptable. Some 60-kΩ options do exist, but are typically more expensive, since these options are not standard values. For the purposes of this design, the choice of 60 kΩ is made at the expense of additional cost. Both resistors are chosen at 0.1% tolerance. If the design decision is to accept the error, always round down to the nearest standard value to avoid setting the overcurrent point above the intended target, potentially failing to trip at the indicated point.

6. **Error check**: A major source of error for current shunt monitors is offset error, especially at low measurements. This can also include contributions from common-mode rejection (CMR) and power supply rejection (PSR) abilities of the device. At the higher end of measurement, gain error typically dominates the measurement, since the sense voltage generated is typically large with respect to the offset, and thus minimizes the contribution. In overcurrent applications, offset is usually not an issue, but has bearing if the design decision is made to set the overcurrent point inside the full scale range for thermal relief of the shunt. The following equation shows the general form of all errors relating to a current sense amplifier, and the following image shows the total error curve for the completed design over 5-V, 12-V, and 28-V designs. The major difference of error here is the contribution from common-mode voltage change.

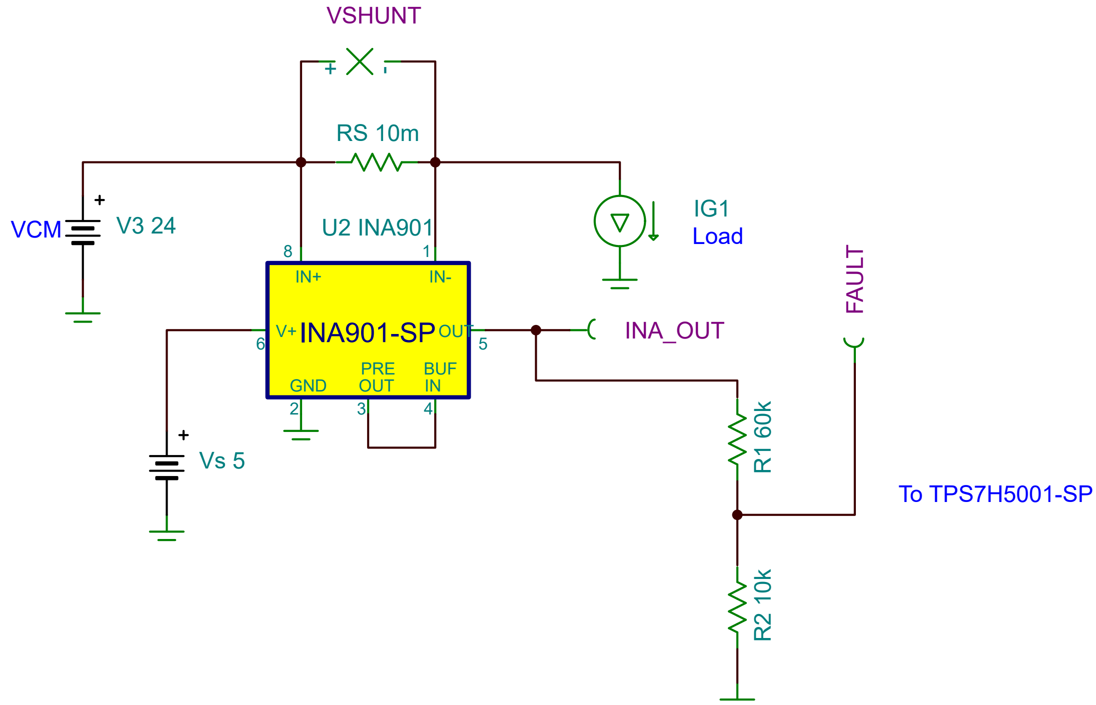
$$e_{\mathrm{TOTAL}} = \sqrt{e_{\mathrm{Vos}}^2 + e_{\mathrm{CMRR}}^2 + e_{\mathrm{PSRR}}^2 + e_{\mathrm{GAIN}}^2 + e_{\mathrm{Linearity}}^2 + e_{\mathrm{Shunt}}^2 + e_{\mathrm{Bias\ Current}}^2 + e_{\mathrm{other}}^2}$$



INA901-SP Total Output Error for Various VCM

The *other* portion of error in the error equation typically addresses additional external factors, such as the tolerances in the attenuation resistors. As shown in the curves, error increases based on the VCM of the circuit as the voltage deviates from the 12-V data sheet condition, which is the nominal common-mode operating point of the INA901-SP, manifesting as additional offset error referred to the input. Additional accuracy can be gained by providing a larger supply voltage and designing the overcurrent point further from the offset, but this comes with the challenge of increased thermals across the shunt, because the generated sense voltage is directly proportional to the produced heat in the shunt.

Design Simulations



INA901-SP TINA-TI Circuit Simulation Setup

Transient Simulation and Bench Test Results

As INA901 TINA-TI Simulation Results demonstrates, the design is confirmed, with the desired 4.2-V output voltage mapping to the desired 0.6-V FAULT trigger. This design was then implemented on the bench.

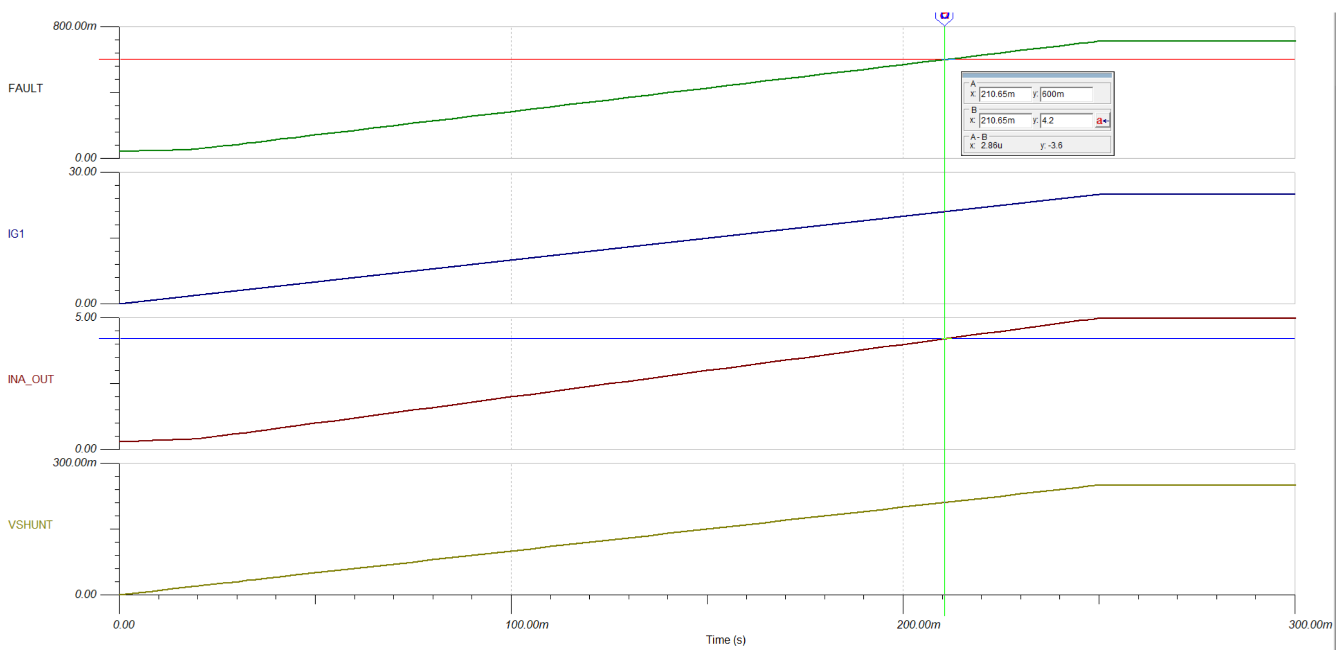
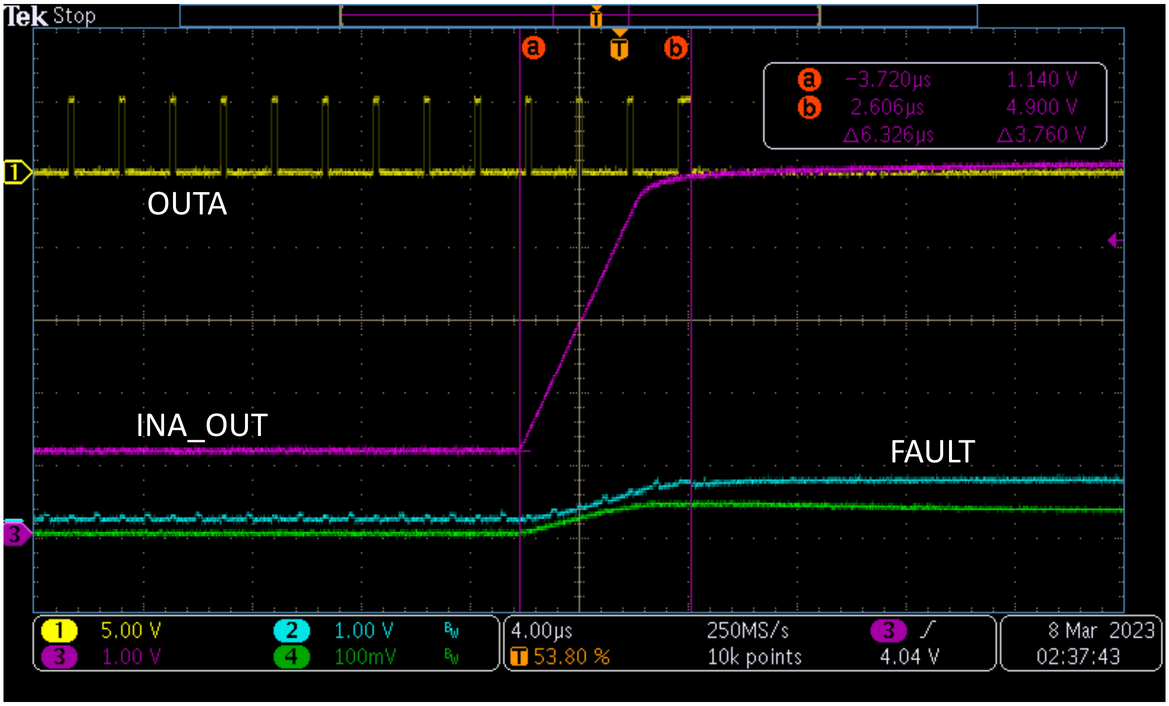


Figure 3. INA901 TINA-TI Simulation Results

In INA901-SP Bench Test of Transient Response, a step input of the INA901-SP from 60 mV_{SENSE} to 250 mV_{SENSE} is made, emulating a short circuit of the load, and the output response is examined. As the curves demonstrate, the time from the beginning of the event to shutdown of the PWM output is approximately 6 μs. From the slew up of the INA901-SP, it can be interpolated that the time between the critical trigger and OUTA shutdown is approximately 2 μs, which is in line with expected performance of the TPS7H500x-SP, shown in TPS7H500x-SP FAULT Pin Response Time.



INA901-SP Bench Test of Transient Response

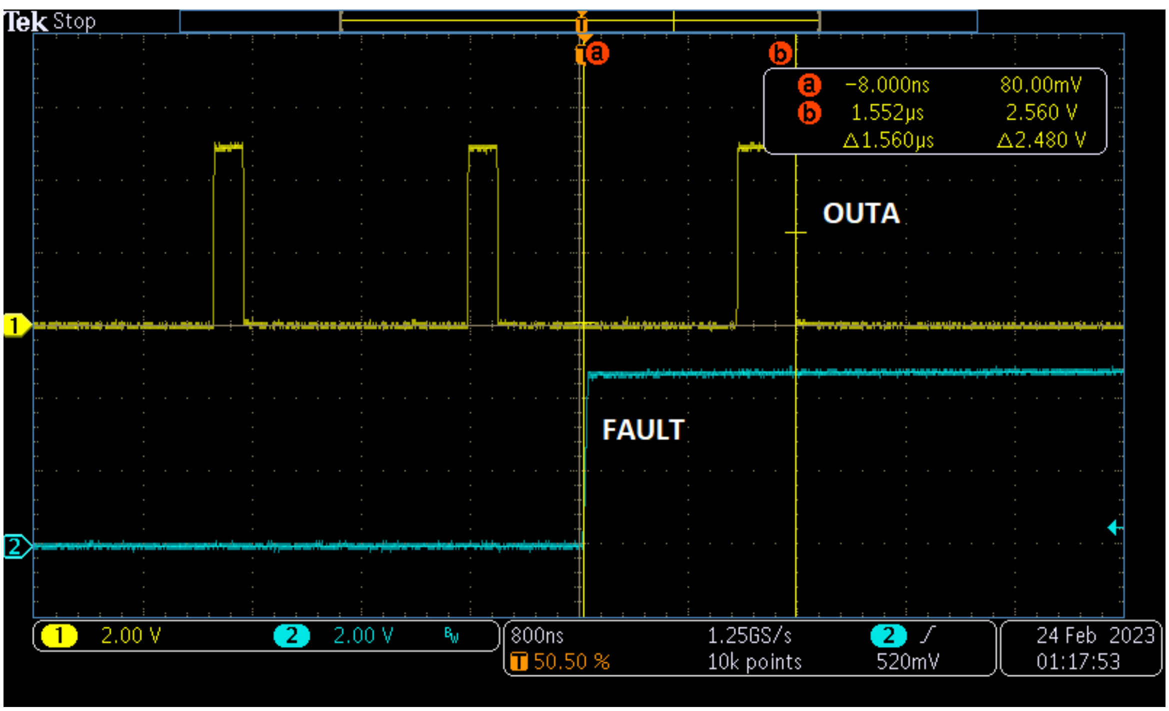


Figure 4. TPS7H500x-SP FAULT Pin Response Time

Design References

See the TI Precision Labs, *Current Sense Amplifiers* video series.

Design Featured Current Sense Amplifier

INA901-SP	
V_S	2.7 V to 16 V
V_{CM}	–15 V to 65 V
V_{OUT}	GND + 3 mV to V_S – 50 mV, typical
V_{OS}	±500 µV, typical
I_q	350 µA, typical
I_B	±8 µA, typical
TID Characterization (ELDRS-Free)	50 krad (Si)
SEL Immune to LET	75 MeV-cm^2 / mg

For less harsh radiation environments, TI also offers the INA240-SEP, which offers SEL immunity to 43 MeV-cm^2 / mg at 125°C. This device is ELDRS free to 30 krad (Si), and Total Ionizing Dose (TID) RLAT for Every Wafer Lot is up to 20 krad(Si):

Design Alternate Current Sense Amplifier

INA240-SEP	
V_S	2.7V to 5.5V
V_{CM}	–4 V to 80 V
V_{OUT}	GND + 1 mV to V_S – 50 mV, typical
V_{OS}	±5 µV, typical
I_q	1.8 mA, typical
I_B	±90 µA, typical
TID Characterization (ELDRS-Free)	30 krad (Si)
SEL Immune to LET	43 MeV-cm^2 / mg