Application Brief

How to Tune the S-Parameters of Your Analog Front-End Signal Chain

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Wide-bandwidth data-acquisition systems (for example, oscilloscopes and active probes) use an analog front-end (AFE) signal chain to capture high-frequency signals and fast-transient pulses. The key characteristics of a wide-band DAQ AFE include:

- Wide -3 dB bandwidth to measure a wide-frequency range of signals
- High-input impedance mode to prevent loading of the measured signals
- Low-noise to detect low-magnitude signals
- Superior distortion performance to maintain signal fidelity

When looking across the industry today one can find a wide variety of amplifiers and buffers which support bandwidths greater than 1 GHz, however, these bandwidths refer to the small-signal bandwidth (< 100 mV_{PP}) and are not suitable to be used in an AFE, designed for large signals (> 1 V_{PP}) in magnitude.

The BUF802 device is an open-loop, unity-gain buffer with a JFET-input stage that offers low-noise, high-impedance buffering for data acquisition system (DAQ) front-ends. The BUF802 supports DC to 3.1 GHz of bandwidth for a 1 V_{PP} signal while offering excellent distortion and noise performance across the frequency range. The BUF802 can be used in a composite loop circuit with a precision amplifier as shown in Figure 1 for applications where wide-bandwidth and high-precision is desired.

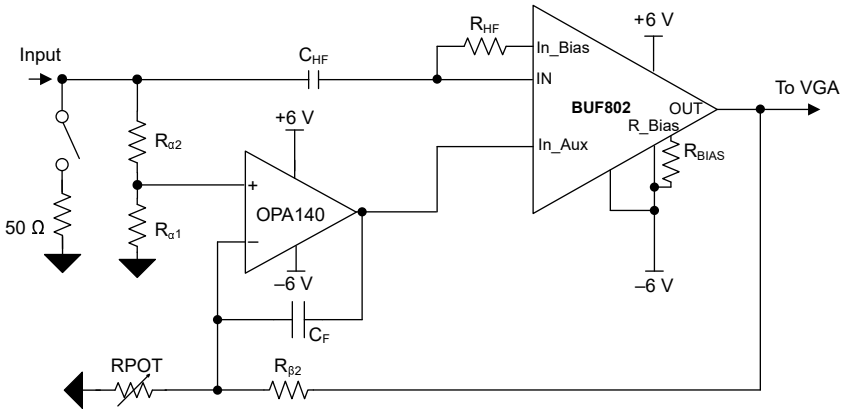

Figure 1. Generic Composite Loop Front-End Stage with OPA140 and BUF802

This article explains tuning of the S-parameters, to achieve a flat frequency response and impedance matching for your front-end design.

Composite Loop Circuits

A composite loop circuit interleaves two different and often complementary sub-circuits to create a single seamless circuit block whose resulting performance is a combination of each sub-circuits benefits. The composite loop in Figure 2 splits the input signal into low frequency and high frequency components, taking each signal component to the output through two different circuits (transfer functions) and recombines them to reproduce a net output signal. The Low-frequency path gives the net transfer function good DC precision and the BUF802 (High-frequency path) allows the net transfer function to achieve a wide-bandwidth. One of the challenges of the circuit in Figure 2 is to smoothly interleave the two paths to achieve wide-bandwidth as well as good DC precision. Any mismatch in the transfer functions of the two paths will lead to a discontinuity in the

net transfer function frequency response resulting in a loss of signal fidelity. The BUF802 uses an innovative architecture to simplify the design challenges discussed previously of interleaving the two signal paths.

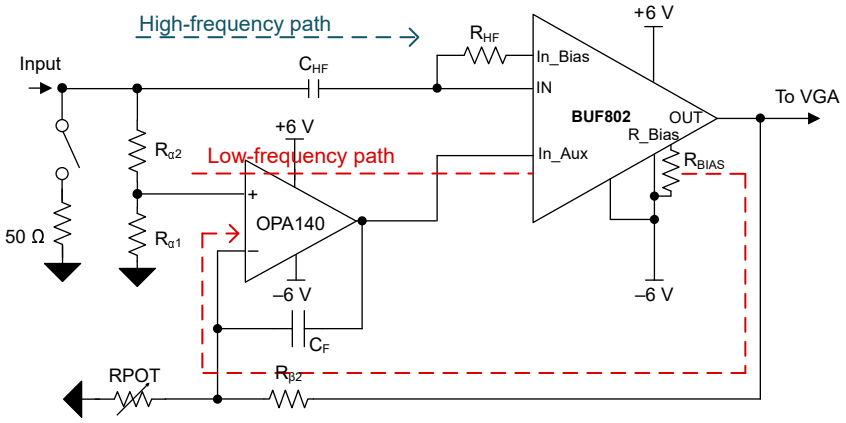

Figure 2. Composite Loop Low- and High-frequency Paths

S-Parameters Fundamentals

Scattering parameters or S-parameters provide a framework for describing networks based on the ratio of input transmission signals and reflected signals as shown in Figure 3. S_{11} represents ratio of the power reflected from port 1 (b_1/a_1, while a_2=0). S_{21} represents ratio of the power transferred from port 1 to port 2 (b_2/a_1, while a_2=0). For a unidirectional device such as a buffer (with port 1 as the input and port 2 as the output), S_{11} is the input port voltage reflection coefficient describing the level of input-impedance matching while S_{21} is the forward voltage gain and describes the frequency response.

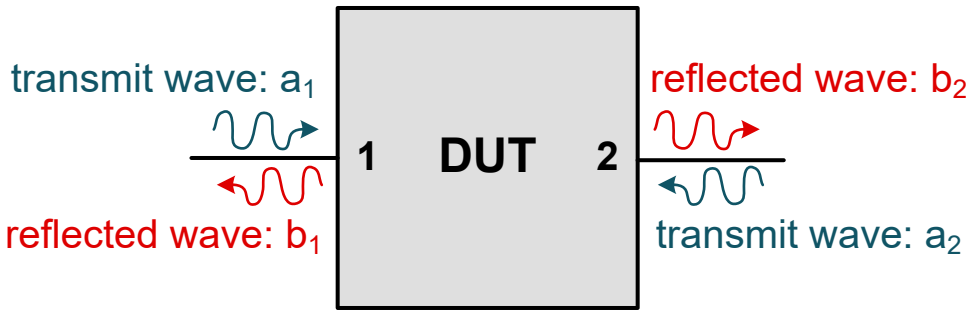

Figure 3. Two-Port Network Wave Quantities

S-parameters are usually represented as a function of frequency. For a detailed analysis of S-parameters check out the blog *So, What are S-Parameters Anyway?*

Tuning Circuit for the S_{21}

To achieve the desired S_{21} across the frequency range the following conditions need to be met:

- Reduction of Peaking and Achieving Wide-Bandwidth
- Achieving Smooth Transition Between Low- to High-frequency

Reduction of Peaking and Achieving Wide-Bandwidth

Figure 4 shows a composite loop circuit with input parasitics caused by the PCB and the DUT (BUF802). The parasitic inductance of the PCB trace (L_S) can interact with the input capacitance of the BUF802 (C_{IN}) to create a resonant LC circuit resulting in a peaked frequency response as shown in Figure 5. To reduce L_S, minimize the trace length from the input port to the BUF802s input. Figure 5 demonstrates the effect of a long trace on S_{21}.

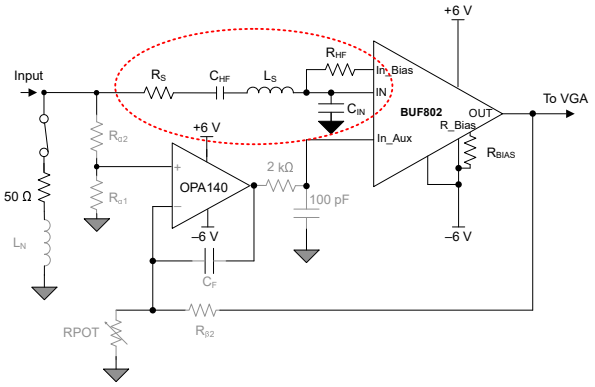

Figure 4. Input Parasitic Network

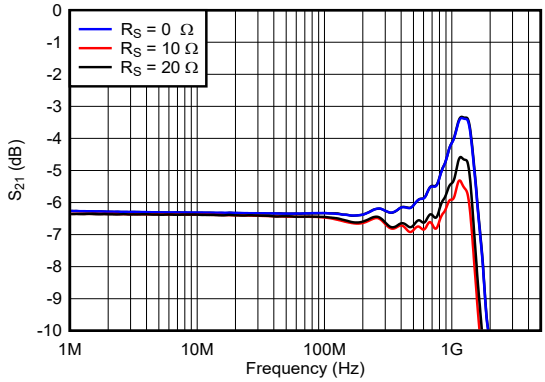

Figure 5. Peaking in S_{21} due to L_S and C_{IN} Resonance

The peaking due to the resonance between L_S and C_{IN} can be dampened by the insertion of a series dampening resistor R_S as shown in Figure 4. Besides helping in dampening S_{21} peaking, R_S also helps with improvement of S_{11}. The exact math behind improvement of S_{11} is discussed in *Tuning of the S_{11} Parameter*.

The series input capacitor C_{HF} forms a voltage divider with C_{IN} reducing the gain of High-frequency path. It is therefore important to make C_{HF} >> C_{IN} to ensure the voltage divider does not attenuate the incoming AC signals.

The BUF802 can achieve a -3 dB bandwidth of 3.1-GHz for 1 V_{PP} signals. The addition of R_S to reduce S_{21} peaking also reduces the bandwidth due to the addition of the RC pole caused by R_S and C_{IN}. This effect is seen in Figure 6.

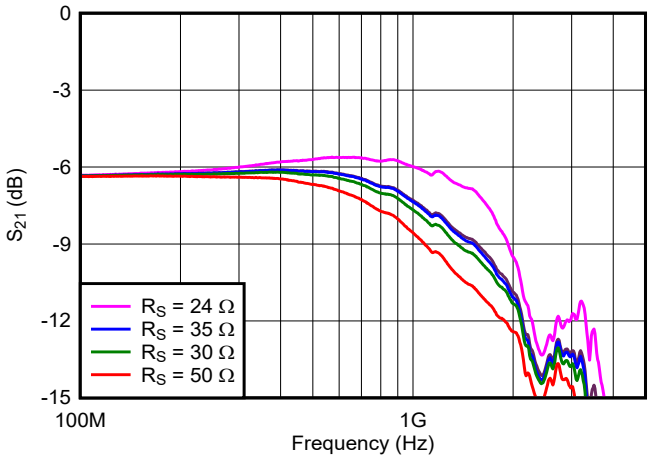

Figure 6. S_{21} Input Response with Varying R_S

Table 1 summarizes the previous points.

Table 1. Impact of R_S Value on the AFE

Increasing R_S	Decreasing R_S
Protects BUF802 against transients	Increases bandwidth
Reduces peaking of S_{21}	Improves S_{11} at lower frequency
Improves S_{11} at higher frequencies	Reduces output noise

Achieving a Smooth Transition Between the Low- and High-Frequency Regions

The BUF802 can be used as a standalone buffer, Buffer Mode (BF Mode), or in a composite loop with a precision amplifier. Composite Loop Mode (CL Mode), helps to achieve both DC precision and wide, large-signal bandwidth. Operating the BUF802 in CL Mode with a precision amplifier requires the S21 responses (Gain) of the two different sub-circuits to be matched to maintain a smooth transition between the low-frequency and high-frequency response. A smooth transition can be achieved by adhering to the following two conditions:

1. $\alpha/\beta = G$ (where $\alpha = R_{\alpha2} / (R_{\alpha2} + R_{\alpha1})$, $1/\beta = 1 + (R_{\beta2} / RPOT)$ as shown in Figure 7 and G = DC Gain of BUF802)
2. High-frequency response pole (f_{HF})<< low-frequency pole (f_{LF})

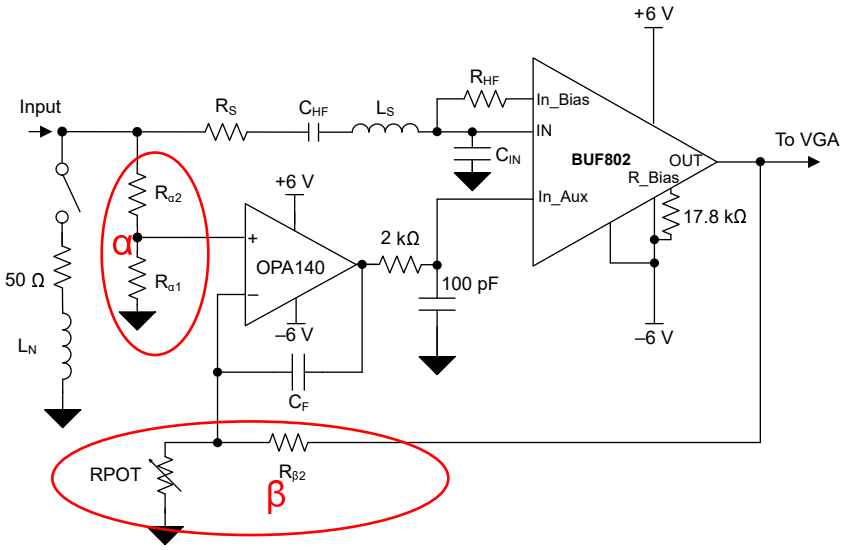

Figure 7. α and β Resistor Network

For the first condition the low-frequency region is determined solely by the precision circuit. The incoming signal is divided down in amplitude by the ratio α and is further gained up by 1/β, by the precision amplifier. Therefore, in the low-frequency region:

$$S_{21} \text{ (at low-frequency)} = \alpha * 1/\beta \quad (1)$$

The Gain (G) can be found in the BUF802 data sheet and is typically 0.96 V/V.

$$S_{21} \text{ (at high-frequency)} = G \quad (2)$$

To maintain a constant S_{21} across frequency make **G = α/β** by adjusting the value of RPOT.

The high-frequency pole of the BUF802 (f_{HF}) path is created by C_{HF} and R_{HF} as is shown in Equation 3. The low-frequency pole (f_{LF}) of the precision amplifier path is a function of the Gain Bandwidth Product (GBW) of the precision amplifier, the auxiliary path gain (G_{AUX}) and the parasitic input capacitance of the BUF802 and is shown in Equation 4.

$$f_{HF} = 1/ (2 \times \pi \times R_{HF} \times C_{HF}) \quad (3)$$

$$f_{LF} = \text{GBW (precision amplifier)} \times G_{AUX} \times \beta \quad (4)$$

The composite loop transition region should be designed so that the high-frequency pole (f_{HF}) falls at a much lower frequency than the low-frequency pole (f_{LF}). This ensures a sufficient overlap in the crossover frequency region and simplifies the complex transfer function into simple poles and zeros.

In addition to the two conditions mentioned previously C_F (compensation capacitor) needs to be tuned to ensure sufficient compensation of the precision amplifier. The C_F value is calculated using the formula in Equation 5.

$$C_F = C_{INPA} * (g\ R_{\alpha 1}/R_{\beta 2} - 1) \quad (5)$$

where C_{INPA} is the common mode input capacitance of the precision amplifier.

Figure 8 shows the effect of C_F tuning for its three different values.

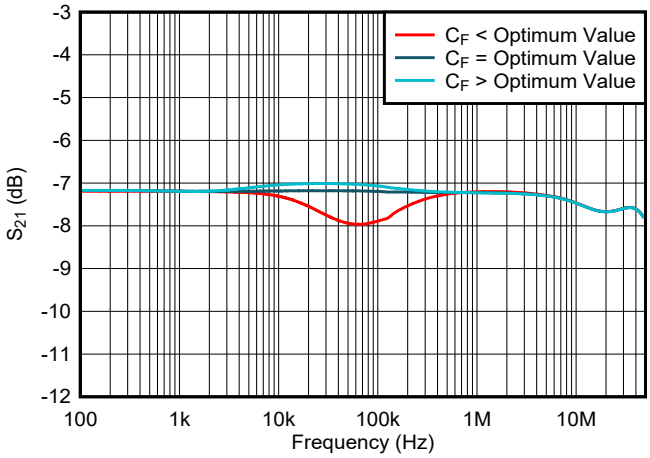

Figure 8. Tuning Output Response with Different C_F Value

Refer to section 9.2.1.2 in the BUF802 data sheet for the design procedure of a 1-GHz AFE using the previous equations.

Tuning Circuit for the Desired S_{11}

Impedance matching is important to reduce reflections and preserve signal integrity. An S_{11} better than -15 dB across the frequency of interest is considered an acceptable target spec. While a 50-Ω termination helps achieve the desired S_{11}, it is important to have a high input impedance option to measure a signal without loading the previous driving stage. Hence, data acquisition systems can have a selectable 50- Ω input and 1-MΩ input termination option. The JFET-input stage of the BUF802 offers G-Ω's of input impedance and can therefore be terminated with an external 1 MΩ resistor without affecting performance. If a 50 Ω termination is required it can be switched in via a relay as shown in Figure 9. The BUF802 therefore has the flexibility to be used in both 1-MΩ and 50-Ω terminated systems.

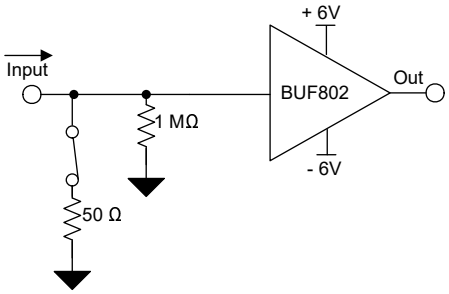

Figure 9. BUF802 with Optional 1 MΩ / 50 Ω Termination

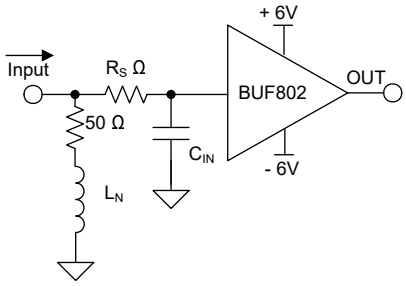

Figure 10. Effective Input Impedance with R_S and L_N

While it is possible to mount an exact 50-Ω termination to achieve the resistance at the input of the front-end composite loop circuit, the parasitic capacitance of the BUF802 (C_{IN}) appears in parallel with the 50-Ω resistance resulting in a non-ideal termination across frequency.

The parasitic input capacitance of the BUF802 (C_{IN}) is 2.4 pF. The input impedance of the BUF802 at a particular frequency (X_{CF}) can be calculated using the formula:

$$X_{CF} = 1/ (2\pi * f *2.4\ pF) \quad (6)$$

Therefore, the net input impedance seen by the signal will be:

$$X_{CF} \,||\, 50\ \Omega \quad (7)$$

For example, at f = 1 GHz, X_{CF} is equal to 66.3 Ω. Therefore, the net input impedance seen by the signal is 66.3 Ω || 50 Ω = 28.5 Ω.

The addition of R_S (to reduce S_{21} peaking), and, the addition of a series termination inductor (L_N) (see Figure 10) results in a net input impedance as shown in Equation 8.

$$\text{Net input impedance} = (50\ \Omega + X_L) \,||\, (R_S + X_{CF}) \quad (8)$$

Where $X_L = 2\pi * f * L_N$

With f = 1 GHz, R_S = 30 Ω, L_N = 6.8 nH, C_{IN} = 2.4 pF and using Equation 8.

$$\text{Input impedance} = (50\ \Omega + 42.7\ \Omega) \,||\, (30\ \Omega + 66.3\ \Omega) \approx 48\ \Omega. \quad (9)$$

While R_S can be increased to bring the input impedance to an exact 50 Ω, we are limited by the maximum R_S value as discussed in Table 1. Figure 11, shows S_{11} vs frequency for different values of R_S.

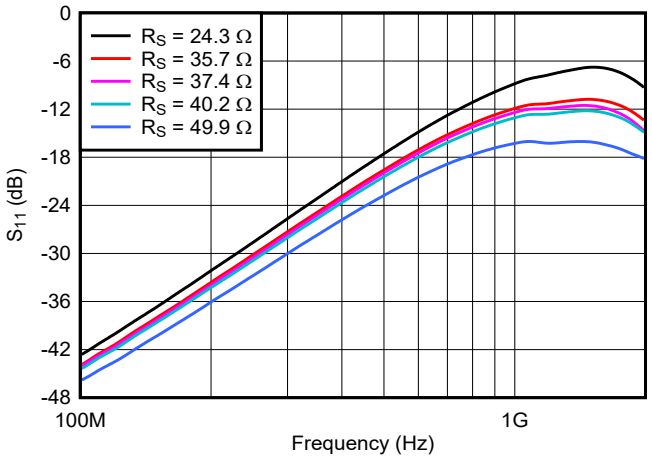

Figure 11. S_{11} with Varying R_S

Additional Information

- For more details on discrete implementation design challenges and how the BUF802 alleviates these problems, read the *Simplify Analog Front-End Designs with Hi-Z Buffers* blog post.
- BUF802 TINA-TI / SPICE model.
- The *Flexible 3.2-GSPS Multi-Channel AFE Reference Design for DSOs, Radar and 5G Wireless Test Systems* illustrates the performance of the BUF802 in a composite loop AFE design with measurement analysis.
- For more information on how to set up the EVM, check out the *BUF802EVM Video*.

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