Functional Safety Information

INA28x-Q1
Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for the INA282-Q1, INA283-Q1, INA284-Q1, INA285-Q1, and INA286-Q1 (SOIC-8 and VSSOP-8 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

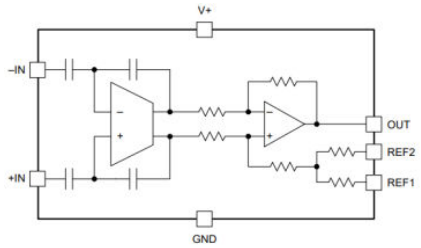

Figure 1-1. Functional Block Diagram

The INA282-Q1 to INA286-Q1 were developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOIC-8 Package

This section provides Functional Safety Failure In Time (FIT) rates for the SOIC-8 package of the INA28x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	10
Die FIT Rate	3
Package FIT Rate	7

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 16.2 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 VSSOP-8 Package

This section provides Functional Safety Failure In Time (FIT) rates for the VSSOP-8 package of the INA28x-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	7
Die FIT Rate	3
Package FIT Rate	4

The failure rate and mission profile information in Table 2-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 16.2 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA28x-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT open (Hi-Z)	10%
OUT to GND	20%
OUT to V+	15%
OUT functional, not in specification	50%
Pin to pin short, any two pins	5%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the INA28x-Q1 (SOIC-8 and VSSOP-8 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2 and Table 4-6.)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = –40°C to +125°C
- V_S = 5 V
- V_{IN+} = 12 V
- V_{REF1} = V_{REF2} = 2.048 V

4.1 SOIC-8 Package

Figure 4-1 shows the INA28x-Q1 pin diagram for the SOIC-8 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA28x-Q1 data sheet.

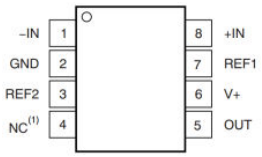

Figure 4-1. Pin Diagram (SOIC-8) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
–IN	1	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, normal operation.	B for High side or D for low side
GND	2	Normal Operation.	D
REF2	3	If intended connection is anything other than GND, functionality will be affected.	D if REF2=GND by design; C otherwise
NC	4	Normal Operation.	D
OUT	5	Output shorts to ground. When left in this configuration for a long time, under high supplies self heating could cause dice junction temperature to exceed 150 degrees Celsius.	B
V+	6	Power supply shorted to ground.	B
REF1	7	If intended connection is anything other than GND, functionality will be affected.	D if REF1=GND by design; C otherwise
+IN	8	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, input pins are shorted.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
–IN	1	Differential input voltage is not well defined.	B
GND	2	GND is floating. Output will be incorrect as it is no longer referenced to GND.	B
REF2	3	Device loses reference voltage.	C
NC	4	Normal Operation.	D
OUT	5	Output can be left open, there is no effect on the IC.	B
V+	6	No power supply to device. Device may be biased through inputs. Output will be close to GND.	B
REF1	7	Device loses reference voltage.	C
+IN	8	Differential input voltage is not well defined.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
–IN	1	GND	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, normal operation.	B
GND	2	REF2	If REF2=GND by design then normal operation, otherwise may affect functionality.	C
REF2	3	NC	Functionality will not be affected if NC pin is not connected, or connected to a potential that is equal to that of REF2 by design. Otherwise functionality will be affected.	C
NC	4	OUT	Normal operation if NC is not connected.	B if NC pin is connected; D if NC pin is not connected
OUT	5	V+	Output shorts to supply. When left in this configuration for a long time, under high supplies self heating could cause dice junction temperature to exceed 150 degrees Celsius.	B
V+	6	REF1	Functionality will be affected if REF1 equals to anything but V+ by design.	D if RE1=V+ by design; otherwise C
REF1	7	+IN	If high voltage (>18V) is present, damage will occur.	A
+IN	8	–IN	Input differential voltage=0V.	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
–IN	1	In high-side configuration, a short from the bus supply to V+ will occur. High current will flow from bus supply to V+ or vice versa. Device could be damaged.	A for High side or B for low side
GND	2	Power supply shorted to GND.	B
REF2	3	If intended connection is anything other than V+, functionality will be affected.	D if REF2=V+ by design; C otherwise
NC	4	Normal operation.	D
OUT	5	Output shorts to supply. When left in this configuration for a long time, under high supplies self heating could cause dice junction temperature to exceed 150 degrees Celsius.	B
V+	6	Normal operation.	D
REF1	7	If intended connection is anything other than V+, functionality will be affected.	D if REF1=V+ by design; C otherwise
+IN	8	In high-side configuration, a short from the bus supply to V+ will occur. High current will flow from bus supply to V+ or vice versa. Device could be damaged.	A for High side or B for low side

4.2 VSSOP-8 Package

Figure 4-2 shows the INA28x-Q1 pin diagram for the VSSOP-8 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA28x-Q1 data sheet.

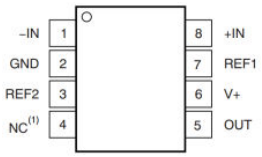

Figure 4-2. Pin Diagram (VSSOP-8 Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
–IN	1	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, normal operation.	B for High side or D for low side
GND	2	Normal Operation.	D
REF2	3	If intended connection is anything other than GND, functionality will be affected.	D if REF2=GND by design; C otherwise
NC	4	Normal Operation.	D
OUT	5	Output shorts to ground. When left in this configuration for a long time, under high supplies self heating could cause dice junction temperature to exceed 150 degrees Celsius.	B
V+	6	Power supply shorted to ground.	B
REF1	7	If intended connection is anything other than GND, functionality will be affected.	D if REF1=GND by design; C otherwise
+IN	8	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, input pins are shorted.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
–IN	1	Differential input voltage is not well defined.	B
GND	2	GND is floating. Output will be incorrect as it is no longer referenced to GND.	B
REF2	3	Device loses reference voltage.	C
NC	4	Normal Operation.	D
OUT	5	Output can be left open, there is no effect on the IC.	B
V+	6	No power supply to device. Device may be biased through inputs. Output will be close to GND.	B
REF1	7	Device loses reference voltage.	C
+IN	8	Differential input voltage is not well defined.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
–IN	1	GND	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, normal operation.	B
GND	2	REF2	If REF2=GND by design then normal operation, otherwise may affect functionality.	C
REF2	3	NC	Functionality will not be affected if NC pin is not connected, or connected to a potential that is equal to that of REF2 by design. Otherwise functionality will be affected.	C
NC	4	OUT	Normal operation if NC is not connected.	B if NC pin is connected; D if NC pin is not connected
OUT	5	V+	Output shorts to supply. When left in this configuration for a long time, under high supplies self heating could cause dice junction temperature to exceed 150 degrees Celsius.	B
V+	6	REF1	Functionality will be affected if REF1 equals to anything but V+ by design.	D if RE1=V+ by design; otherwise C
REF1	7	+IN	If high voltage (>18V) is present, damage will occur.	A
+IN	8	–IN	Input differential voltage=0V.	C

Table 4-9. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
–IN	1	In high-side configuration, a short from the bus supply to V+ will occur. High current will flow from bus supply to V+ or vice versa. Device could be damaged.	A for High side or B for low side
GND	2	Power supply shorted to GND.	B
REF2	3	If intended connection is anything other than V+, functionality will be affected.	D if REF2=V+ by design; C otherwise
NC	4	Normal operation.	D
OUT	5	Output shorts to supply. When left in this configuration for a long time, under high supplies self heating could cause dice junction temperature to exceed 150 degrees Celsius.	B
V+	6	Normal operation.	D
REF1	7	If intended connection is anything other than V+, functionality will be affected.	D if REF1=V+ by design; C otherwise
+IN	8	In high-side configuration, a short from the bus supply to V+ will occur. High current will flow from bus supply to V+ or vice versa. Device could be damaged.	A for High side or B for low side

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2020) to Revision A (November 2020) **Page**

- Added INA283-Q1, INA284-Q1, INA285-Q1 and INA286-Q1 devices to the document..... 1

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