TLV9002 Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for TLV9002 to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

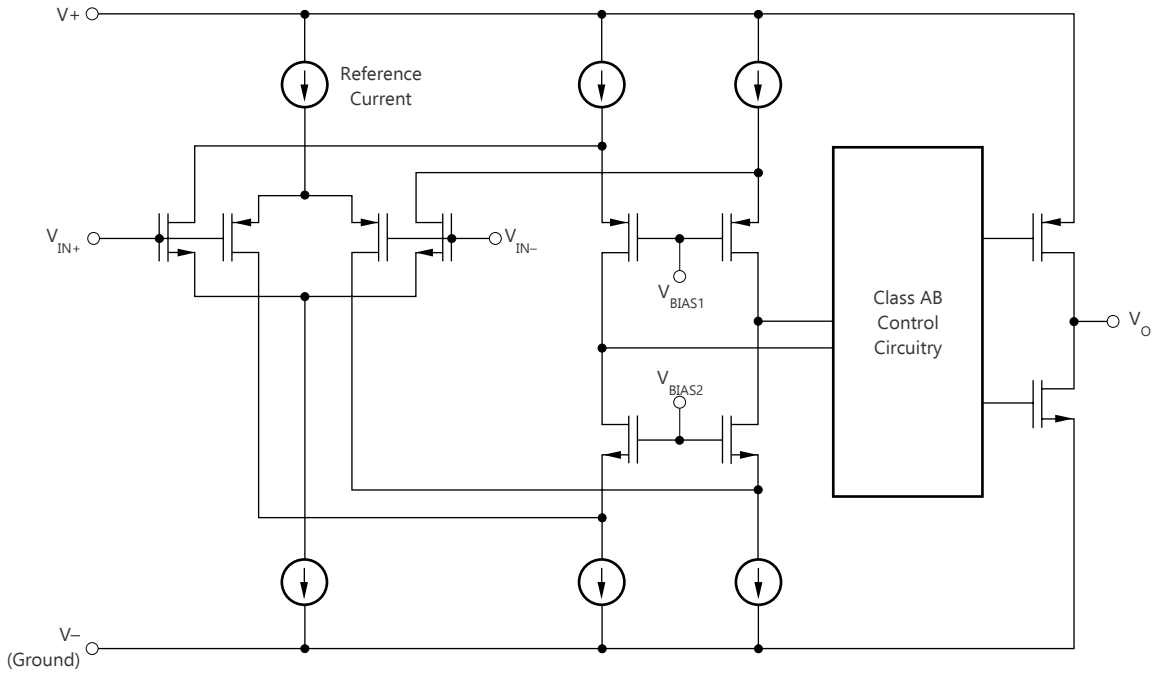

Figure 1. Functional Block Diagram

TLV9002 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the TLV9002 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)				
Package	TSSOP-8	VSSOP-8	SOIC-8	SOT23-8	WSON-8
Total Component FIT Rate	9	7	10	5	5
Die FIT Rate	3	3	3	3	3
Package FIT Rate	6	4	7	2	2

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 50 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op Amp, Comparators, Voltage Monitors	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TLV9002 in Table 3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Out open (HIZ)	20%
Out saturate high	25%
Out saturate low	25%
Out functional not in specification voltage or timing	30%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TLV9002. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5 and Table 9)
- Pin open-circuited (see Table 6 and Table 10)
- Pin short-circuited to an adjacent pin (see Table 7 and Table 11)
- Pin short-circuited to supply (see Table 8 and Table 12)
- Pin short-circuited to thermal pad (see Table 13)

Table 5 through Table 13 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4.

Table 4. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Single-supply operation is used. For example, V+ = 5 and V- = 0V.

4.1 [PW] TSSOP-8, [DGK] VSSOP-8, [D] SOIC-8, [DDF] SOT23-8 Packages

Figure 2 shows the TLV9002 pin diagram for the TSSOP-8, VSSOP-8, SOIC-8, and SOT23-8 packages. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the TLV9002 datasheet.

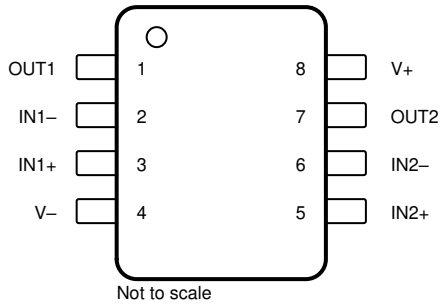

Figure 2. Pin Diagram for TSSOP-8, VSSOP-8, SOIC-8, and SOT23-8 packages

Table 5. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	May cause device to overheat.	B
IN1-	2	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
IN1+	3	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
V-	4	Normal operation.	D
IN2+	5	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
IN2-	6	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
OUT2	7	May cause device to overheat.	B
V+	8	Diodes from input to V+ may turn on due to input signal and cause electrical overstress (EOS).	B

Table 6. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Output cannot be used by application.	C
IN1-	2	Floating input, circuit will likely not function as expected.	C
IN1+	3	Floating input, circuit will likely not function as expected.	C
V-	4	Lowest voltage pin will try to power internal ground via ESD diode to ground.	B
IN2+	5	Floating input, circuit will likely not function as expected.	C
IN2-	6	Floating input, circuit will likely not function as expected.	C
OUT2	7	Output cannot be used by application.	C
V+	8	Highest voltage pin will try to power internal ground via ESD diode to V+.	B

Table 7. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	IN1-	Negative feedback, creates unity gain buffer.	C
IN1-	2	IN1+	No damage to device. Application circuit will not work.	C
IN1+	3	V-	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
V-	4	IN2+	Input at V- (GND) is valid input, however, desired application result is unlikely. Pins are not adjacent to each other.	C
IN2+	5	IN2-	No damage to device. Application circuit will not work.	C
IN2-	6	OUT2	Negative feedback, creates unity gain buffer.	C
OUT2	7	V+	May cause device to overheat.	B
V+	8	OUT1	May cause device to overheater. Pins are not adjacent to each other.	B

Table 8. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	May cause device to overheat.	B
IN1-	2	Input at V+ is a valid input, however, desired application result is unlikely.	C
IN1+	3	Input at V+ is a valid input, however, desired application result is unlikely.	C
V-	4	Diodes from input to V- may turn on due to input signal and cause electrical overstress (EOS).	B
IN2+	5	Input at V+ is a valid input, however, desired application result is unlikely.	C
IN2-	6	Input at V+ is a valid input, however, desired application result is unlikely.	C
OUT2	7	May cause device to overheat.	B
V+	8	Normal operation.	D

4.2 [DSG] WSON -8 Package

Figure 3 shows the TLV9002 pin diagram for the WSON-8 package. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the TLV9002 datasheet.

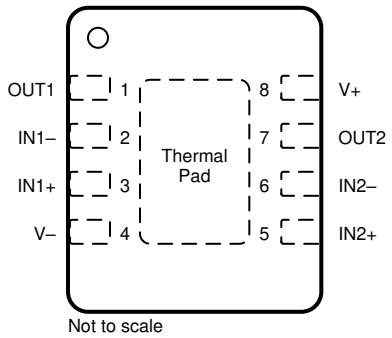

Figure 3. Pin Diagram (WSON-8 Package)

Table 9. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	May cause device to overheat.	B
IN1-	2	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
IN1+	3	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
V-	4	Normal operation.	D
IN2+	5	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
IN2-	6	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
OUT2	7	May cause device to overheat.	B
V+	8	Diodes from input to V+ may turn on due to input signal and cause electrical overstress (EOS).	B
PAD	Thermal Pad	Pad is normally connected to V- (GND) or open.	D

Table 10. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Output cannot be used by application.	C
IN1-	2	Floating input, circuit will likely not function as expected.	C
IN1+	3	Floating input, circuit will likely not function as expected.	C
V-	4	Lowest voltage pin will try to power internal ground via ESD diode to ground.	B
IN2+	5	Floating input, circuit will likely not function as expected.	C
IN2-	6	Floating input, circuit will likely not function as expected.	C
OUT2	7	Output cannot be used by application.	C
V+	8	Highest voltage pin will try to power internal ground via ESD diode to V+.	B
PAD	Thermal Pad	Pad is normally connected to V- (GND) or open.	D

Table 11. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	IN1-	Negative feedback, creates unity gain buffer.	C
IN1-	2	IN1+	No damage to device. Application circuit will not work.	C
IN1+	3	V-	Input at V- (GND) is valid input, however, desired application result is unlikely.	C
V-	4	IN2+	Input at V- (GND) is valid input, however, desired application result is unlikely. Pins are not adjacent to each other.	C
IN2+	5	IN2-	No damage to device. Application circuit will not work.	C
IN2-	6	OUT2	Negative feedback, creates unity gain buffer.	C
OUT2	7	V+	May cause device to overheat.	B
V+	8	OUT1	May cause device to overheater. Pins are not adjacent to each other.	B

Table 12. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	May cause device to overheat.	B
IN1-	2	Input at V+ is a valid input, however, desired application result is unlikely.	C
IN1+	3	Input at V+ is a valid input, however, desired application result is unlikely.	C
V-	4	Diodes from input to V- may turn on due to input signal and cause electrical overstress (EOS).	B
IN2+	5	Input at V+ is a valid input, however, desired application result is unlikely.	C
IN2-	6	Input at V+ is a valid input, however, desired application result is unlikely.	C
OUT2	7	May cause device to overheat.	B
V+	8	Normal operation.	D
PAD	Thermal Pad	May cause overheating or device damage.	A

Table 13. Pin FMA for Device Pins Short-Circuited to Thermal Pad

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	May cause device to overheat or device damage.	B
IN1-	2	Desired application result is unlikely and leakage may occur.	B
IN1+	3	Desired application result is unlikely and leakage may occur.	B
V-	4	Normal operation.	D
IN2+	5	Desired application result is unlikely and leakage may occur.	B
IN2-	6	Desired application result is unlikely and leakage may occur.	B
OUT2	7	May cause device to overheat or device damage.	B
V+	8	May cause device to overheat or device damage.	A

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