INA240-Q1 Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for INA240-Q1 (TSSOP-8 and SOIC-8 packages) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

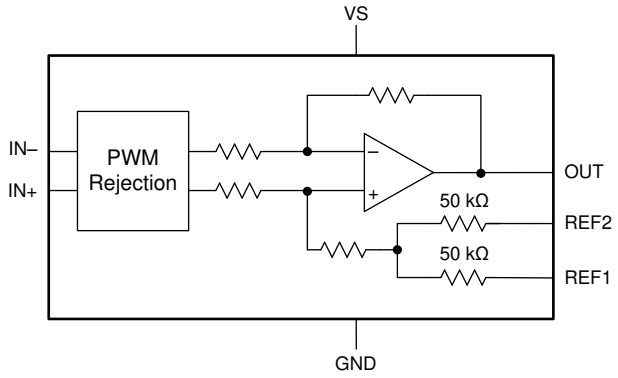

Figure 1. Functional Block Diagram

INA240-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 TSSOP-8 Package

This section provides Functional Safety Failure In Time (FIT) rates for the TSSOP-8 package of INA240-Q1 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	8
Die FIT Rate	2
Package FIT Rate	6

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 13 mW
- Climate type: World-wide Table 8
- Package factor: Lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	BICMOS Analog mixed < 50V	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 SOIC-8 Package

This section provides Functional Safety Failure In Time (FIT) rates for the SOIC-8 package of INA240-Q1 based on two different industry-wide used reliability standards:

- Table 3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	9
Die FIT Rate	2
Package FIT Rate	7

The failure rate and mission profile information in Table 3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 13 mW
- Climate type: World-wide Table 8
- Package factor: Lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	BICMOS Analog mixed < 50V	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA240-Q1 in Table 5 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 5. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT open (Hi-Z)	10%
OUT to GND	20%
OUT to VS	15%
OUT functional, not in specification	50%
Pin to pin short, any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the INA240-Q1 (TSSOP-8 and SOIC-8 packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 7 and Table 11)
- Pin open-circuited (see Table 8 and Table 12)
- Pin short-circuited to an adjacent pin (see Table 9 and Table 13)
- Pin short-circuited to VS (see Table 10 and Table 14)

Table 7 through Table 14 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 6.

Table 6. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_S = 5 V
- V_{IN+} = 12 V
- $V_{REF1} = V_{REF2} = V_S / 2$

4.1 TSSOP-8 Package

Figure 2 shows the INA240-Q1 pin diagram for the TSSOP-8 package. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the INA240-Q1 datasheet.

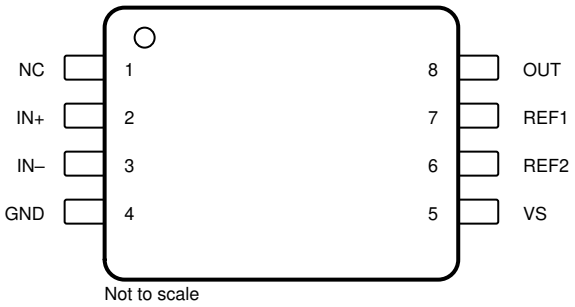

Figure 2. Pin Diagram (TSSOP-8 Package)

Table 7. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
NC	1	Normal operation.	D
IN+	2	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, input pins are shorted.	B
IN-	3	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, normal operation.	B for high-side; D for low-side
GND	4	Normal operation.	D
VS	5	Power supply shorted to GND.	B
REF2	6	If intended connection is anything other than GND, functionality will be affected.	D if REF2=GND by design; B otherwise
REF1	7	If intended connection is anything other than GND, functionality will be affected.	D if REF1=GND by design; B otherwise
OUT	8	Output shorted to GND.	B

Table 8. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
NC	1	This pin has an internal weak pull down. Even though possible, the likelihood of malfunction is very low.	C
IN+	2	IN+ will be at the same potential as IN-. Differential input voltage is effectively 0V.	B
IN-	3	IN- will be at the same potential as IN+. Differential input voltage is effectively 0V.	B
GND	4	GND is floating. Output will be incorrect as it is no longer referenced to GND.	B
VS	5	No power supply to device. Device may be biased through inputs. Output will be close to GND.	B
REF2	6	Output common-mode voltage is not defined. Output will not maintain a linear relationship with differential input voltage.	B
REF1	7	Output common-mode voltage is not defined. Output will not maintain a linear relationship with differential input voltage.	B
OUT	8	Output can be left open. There is no effect on the IC, but the output will not be measured.	C

Table 9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
NC	1	2 - IN+	High bus voltage may exceed specification of NC pin and cause damage.	A
IN+	2	3 - IN-	IN+ will be at the same potential as IN-. Differential input voltage is effectively 0V.	B
IN-	3	4 - GND	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, normal operation.	B for high-side; D for low-side
GND	4	5 - VS	Power supply shorted to GND.	B
VS	5	6 - REF2	If intended connection is anything other than REF2, functionality will be affected.	D if REF2=VS by design; B otherwise
REF2	6	7 - REF1	If intended connection is anything other than REF1, functionality will be affected.	D if REF1=REF2 by design; B otherwise
REF1	7	8 - OUT	Device loses proper reference, functionality is affected.	B
OUT	8	1 - NC	Output shorted to GND if NC is connected to GND as recommended.	B

Table 10. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
NC	1	Additional small amount of current is drawn by the internal pull-down resistor.	D
IN+	2	In high-side configuration, a short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. Device could be damaged. In low-side configuration, device power supply shorted to GND.	A for high-side; B for low side
IN-	3	In high-side configuration, a short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. Device could be damaged. In low-side configuration, device power supply shorted to GND.	A for high-side; B for low side
GND	4	Power supply shorted to GND.	B
VS	5	Normal operation.	D
REF2	6	If intended connection is anything other than VS, functionality will be affected.	D if REF2=VS by design; B otherwise
REF1	7	If intended connection is anything other than VS, functionality will be affected.	D if REF1=VS by design; B otherwise
OUT	8	Output shorted to power supply.	B

4.2 SOIC-8 Package

Figure 3 shows the INA240-Q1 pin diagram for the SOIC-8 package. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the INA240-Q1 datasheet.

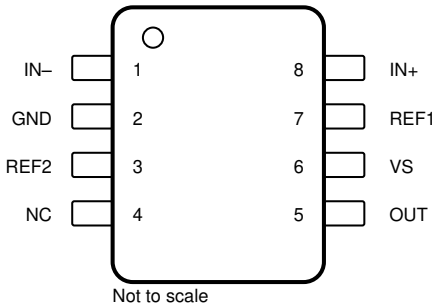

Figure 3. Pin Diagram (SOIC-8 Package)

Table 11. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN-	1	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, normal operation.	B for high-side; D for low-side
GND	2	Normal operation.	D
REF2	3	If intended connection is anything other than GND, functionality will be affected.	D if REF2=GND by design; B otherwise
NC	4	Normal operation.	D
OUT	5	Output shorted to GND.	B
VS	6	Power supply shorted to GND.	B
REF1	7	If intended connection is anything other than GND, functionality will be affected.	D if REF1=GND by design; B otherwise
IN+	8	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, input pins are shorted.	B

Table 12. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN-	1	IN- will be at the same potential as IN+. Differential input voltage is effectively 0V.	B
GND	2	GND is floating. Output will be incorrect as it is no longer referenced to GND.	B
REF2	3	Output common-mode voltage is not defined. Output will not maintain a linear relationship with differential input voltage.	B
NC	4	This pin has an internal weak pull down. Even though possible, the likelihood of malfunction is very low.	C
OUT	5	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
VS	6	No power supply to device. Device may be biased through inputs. Output will be close to GND.	B
REF1	7	Output common-mode voltage is not defined. Output will not maintain a linear relationship with differential input voltage.	B
IN+	8	IN+ will be at the same potential as IN-. Differential input voltage is effectively 0V.	B

Table 13. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN-	1	2 - GND	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, normal operation.	B for high-side; D for low-side
GND	2	3 - REF2	If intended connection is anything other than GND, functionality will be affected.	D if REF2=GND by design; B otherwise
REF2	3	4 - NC	REF2 shorted to GND if NC is connected to GND as recommended. If intended connection is anything other than GND, functionality will be affected.	D if REF2=GND by design; B otherwise
NC	4	5 - OUT	Output shorted to GND if NC is connected to GND as recommended.	B
OUT	5	6 - VS	Output shorted to power supply.	B
VS	6	7 - REF1	If intended connection is anything other than VS, functionality will be affected.	D if REF1=VS by design; B otherwise
REF1	7	8 - IN+	REF1 is shorted to bus voltage. If high voltage is present, damage will occur.	A
IN+	8	1 - IN-	IN+ will be at the same potential as IN-. Differential input voltage is effectively 0V.	B

Table 14. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN-	1	In high-side configuration, a short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. Device could be damaged. In low-side configuration, device power supply shorted to GND.	A for high-side; B for low side
GND	2	Power supply shorted to GND.	B
REF2	3	If intended connection is anything other than VS, functionality will be affected.	D if REF2=VS by design; B otherwise
NC	4	Additional small amount of current is drawn by the internal pull-down resistor.	D
OUT	5	Output shorted to power supply.	B
VS	6	Normal operation.	D
REF1	7	If intended connection is anything other than VS, functionality will be affected.	D if REF1=VS by design; B otherwise
IN+	8	In high-side configuration, a short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. Device could be damaged. In low-side configuration, device power supply shorted to GND.	A for high-side; B for low side

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2020) to A Revision	Page
• Changed to latest report format, including FIT Rate, FMD, and Pin FMA	1

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