Application Note

Designing for TLV90xxS Operational Amplifiers With Shutdown

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ABSTRACT

This document discusses the shutdown variants of the TLV90xx device family. Amplifiers with the shutdown feature allow the designer to choose when the amplifier is enabled, thereby offering power saving benefits. This is especially useful in battery powered applications. Topics covered include shutdown parameters, transient behaviors, enable time and shutdown time factors, device performance while in shutdown and signal muxing with shutdown devices.

Table of Contents

List of Figures

List of Tables

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1 Introduction

A feature that is becoming more common in modern operational amplifiers (op amps) is the ability to enable and disable the device. Texas Instruments (TI) currently has over 60 op amps with shutdown functionality and more on the way. This application note will provide an explanation of various shutdown parameters and design considerations for the TLV90xxS family of devices including the TLV900xS, TLV905xS and TLV906xS.

Amplifiers with shutdown functionality are well suited to applications that are battery powered and require portions of their system to turn off to save power. Examples of such systems include smoke detectors, PIR sensors, field transmitters and remote sensors. "Low power" amplifiers that do not have shutdown functionality typically have some tradeoffs, such as exchanging low quiescent current for very low bandwidth. On the other hand, amplifiers with shutdown functionality can offer low current consumption when not in use and greater bandwidth when in use. Despite requiring a bit more control, they can mitigate this power for performance tradeoff.

Amplifiers with shutdown functionality allow the user to "enable" and "disable," or "shutdown," the device even while the supply rails remain powered. When the amplifier is enabled, it functions as expected by amplifying the difference between the inverting and non-inverting inputs by the open loop gain (A_{OL}) and consuming the full amount of quiescent current (I_Q). When the amplifier is in shutdown, it consumes much less quiescent current and the output becomes high impedance.

Devices that are in a single or dual channel package usually have one $\overline{SHDN}$ pin per amplifier. Quad package devices typically come with two $\overline{SHDN}$ pins: one for controlling channels 1 and 2 and another for controlling channels 3 and 4. Figure 1-1 and Figure 1-2 show example pinouts for a dual channel shutdown device (TLV9062S) and a quad channel shutdown device (TLV9064S).

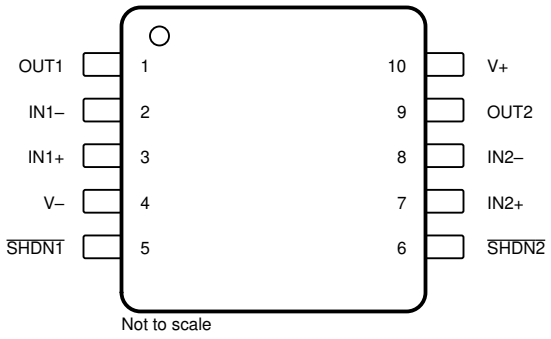

Figure 1-1. TLV9062S DGS Package

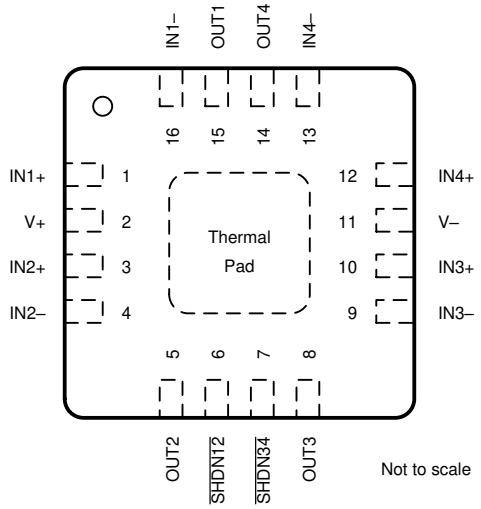

Figure 1-2. TLV9064S RTE Package

2 Shutdown Specifications

For the TLV90xxS family of products, the shutdown specifications are given in the “Electrical Characteristics” table of the device data sheet as shown for the TLV906xS in Figure 2-1 below. Not all TI op amps with shutdown functionality have the same information in their respective data sheets. However, most will specify the quiescent current when disabled, threshold voltages for the shutdown state, and enable/disable times. Definitions for the shutdown parameters follow in Table 2-1.

Electrical Characteristics (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = 1.8 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current per amplifier	V_S = 5.5 V, I_O = 0 mA		538	750	µA
		V_S = 5.5 V, I_O = 0 mA, T_A = –40°C to 125°C			800	
SHUTDOWN						
I_{QSD}	Quiescent current per amplifier	V_S = 1.8 V to 5.5 V, all amplifiers disabled, $\overline{SHDN}$ = Low		0.5	1.5	µA
Z_{SHDN}	Output impedance during shutdown	V_S = 1.8 V to 5.5 V, amplifier disabled		10 || 8		GΩ || pF
$V_{SHDN\_THR\_HI}$	High level voltage shutdown threshold (amplifier enabled)	V_S = 1.8 V to 5.5 V		(V–) + 0.9 V	(V–) + 1.1 V	V
$V_{SDHN\_THR\_LO}$	Low level voltage shutdown threshold (amplifier disabled)	V_S = 1.8 V to 5.5 V	(V–) + 0.2 V	(V–) + 0.7 V		V
t_{ON}	Amplifier enable time (shutdown)(2)	V_S = 1.8 V to 5.5 V, full shutdown; G = 1, V_{OUT} = 0.9 × V_S / 2, R_L connected to V–		10		µs
t_{OFF}	Amplifier disable time(2)	V_S = 1.8 V to 5.5 V, G = 1, V_{OUT} = 0.1 × V_S / 2, R_L connected to V–		0.6		µs
	$\overline{SHDN}$ pin input bias current (per pin)	V_S = 1.8 V to 5.5 V, V+ ≥ $\overline{SHDN}$ ≥ (V+) – 0.8 V		130		pA
		V_S = 1.8 V to 5.5 V, V– ≤ $\overline{SHDN}$ ≤ V– + 0.8 V		40		

(2) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

Figure 2-1. TLV906xS Electrical Characteristics Table Shutdown Specifications

Table 2-1. Shutdown Parameter Definitions

Symbol	Parameter	Definition
I_{QSD}	Quiescent current per amplifier	The current that a single channel consumes while it is disabled
Z_{SHDN}	Output impedance during shutdown	The impedance looking back into the output pin of the amplifier while the amplifier has power at the rails but is in the disabled, or shutdown, state
$V_{SHDN\_THR\_HI}$	High level voltage shutdown threshold (amplifier enabled)	The voltage level applied to the $\overline{SHDN}$ pin that enables the amplifier
$V_{SHDN\_THR\_LO}$	Low level voltage shutdown threshold (amplifier disabled)	The voltage level applied to the $\overline{SHDN}$ pin that disables the amplifier
t_{ON}	Amplifier enable time (shutdown)	The time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches 90% of the final output voltage
t_{OFF}	Amplifier disable time	The time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches 10% of the final output voltage
	$\overline{SHDN}$ pin input bias current (per pin)	The amount of current that typically flows into the $\overline{SHDN}$ pin

Some shutdown specifications are similar but different from specifications for amplifiers in normal operation. For example, the previously defined quiescent current during shutdown, I_{QSD}, is similar to quiescent current, I_Q. However, the test condition for the TLV906xS specifies that I_{QSD} testing is done with all device channels disabled. As shown in Figure 2-1 above, the TLV906xS devices have a typical quiescent current of 0.5 µA while in the full shutdown state with all channels off. This is less than 0.1% of their typical I_Q per channel of 538 µA while enabled.

Similarly, Z_{SHDN} is reminiscent of the amplifier's open-loop output impedance while the amplifier is enabled (Z_O). Z_{SHDN} is specified in Figure 2-1 as a parallel combination of a resistance (R_{SHDN}) and a capacitance (C_{SHDN}). When plotted over frequency, it resembles the curve shown in Figure 2-2. At DC, this impedance is equal to the resistance given in the specification table, 10 GΩ in this case. As the frequency increases, the capacitance begins to dominate the response and reduces the overall output impedance. For the TLV906xS devices, this impedance falls to 200 kΩ at 100 kHz.

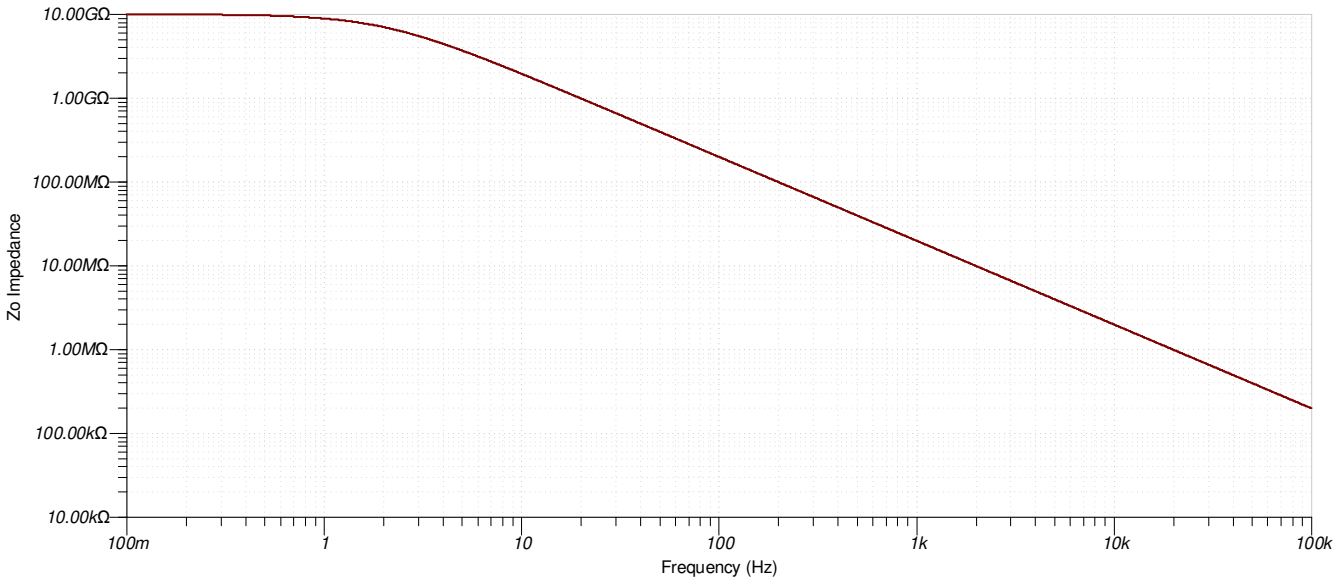

Figure 2-2. Output Impedance During Shutdown

Finally, the shutdown devices feature threshold voltages, specified by $V_{SHDN\_THR\_HI}$ and $V_{SHDN\_THR\_LO}$, that define the enable and disable regions via the $\overline{SHDN}$ pin. Between these voltages is an undefined state where the amplifier may be on, off, or some combination of the two states. The threshold voltages for the TLV90xxS devices are defined relative to the supply voltage. However, other devices may give absolute voltages for a specific supply. Figure 2-3 illustrates the $\overline{SHDN}$ pin regions using the threshold values from the TLV906xS data sheet with the grey striped area representing the undefined state. The left bar shows the minimum and maximum threshold values from the data sheet and the right bar shows the typical threshold values. To ensure proper operation, the minimum and maximum thresholds should be met during design.

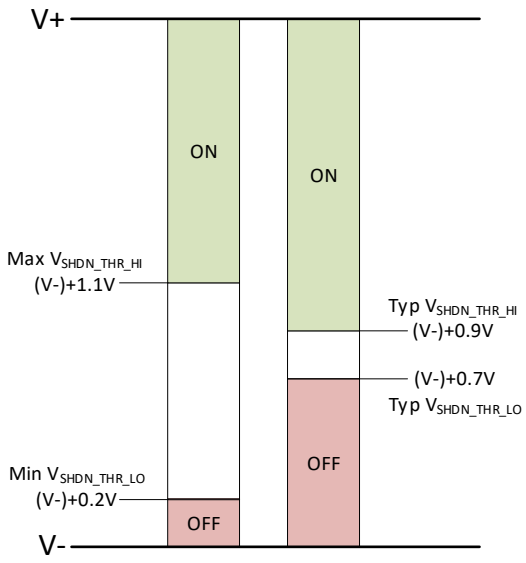

Figure 2-3. Shutdown Threshold Graphic

3 $\overline{SHDN}$ Pin Limits and Connections

The maximum input voltage that can be safely applied to the $\overline{SHDN}$ pin is given in the “Absolute Maximum Ratings” section of the data sheet under the "Signal input pins" row. Care must be taken not to exceed this limit to avoid damage to the part. For the TLV90xxS devices, the absolute maximum voltage rating of the shutdown pin is 500 mV above V+ and the minimum voltage is 500 mV below V–. The $\overline{SHDN}$ pin should be tied to V+ if it is unused. Some TI amplifiers with shutdown capability have an internal pull-up resistor from the $\overline{SHDN}$ pin to VCC, which allows the $\overline{SHDN}$ pin to be left unconnected. However, this should only be done if it is mentioned as a valid setup in the data sheet.

4 Output Behavior During Enable and Shutdown

As mentioned above, there is a time delay from when a signal is applied to the $\overline{SHDN}$ pin to when the amplifier enters the desired state. This was defined previously as t_{ON} or t_{OFF}. Figure 4-1 shows a typical enable transient response for the TLV9052S device, where the device is configured as specified in the "Shutdown" portion of the data sheet. Two enabling plots are shown: one from partial shutdown and one from full shutdown. A partial shutdown state means having one half the channels in the part enabled and the other half in shutdown. For full shutdown, all channels are disabled. Note that when the part comes out of partial shutdown, it has a significantly faster enable time. This occurs because some of the internal bias circuitry is left on to power the already enabled channel(s).

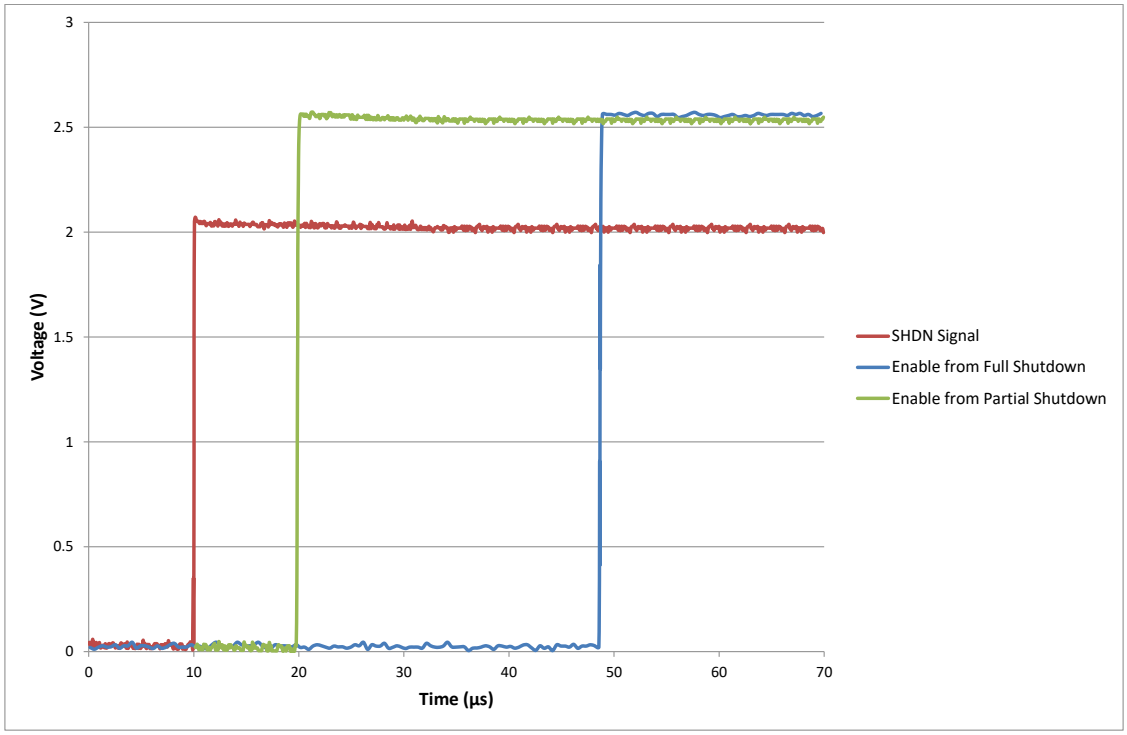

Figure 4-1. TLV9052S Enable From Full Shutdown and From Partial Shutdown

Similarly, Figure 4-2 shows channel 1 of the device being disabled when configured as outlined in the data sheet. Note that there is no distinction between disable times for putting the part into full shutdown versus partial shutdown. This is because each channel shuts down separately. Thus, only one shutdown time specification is required.

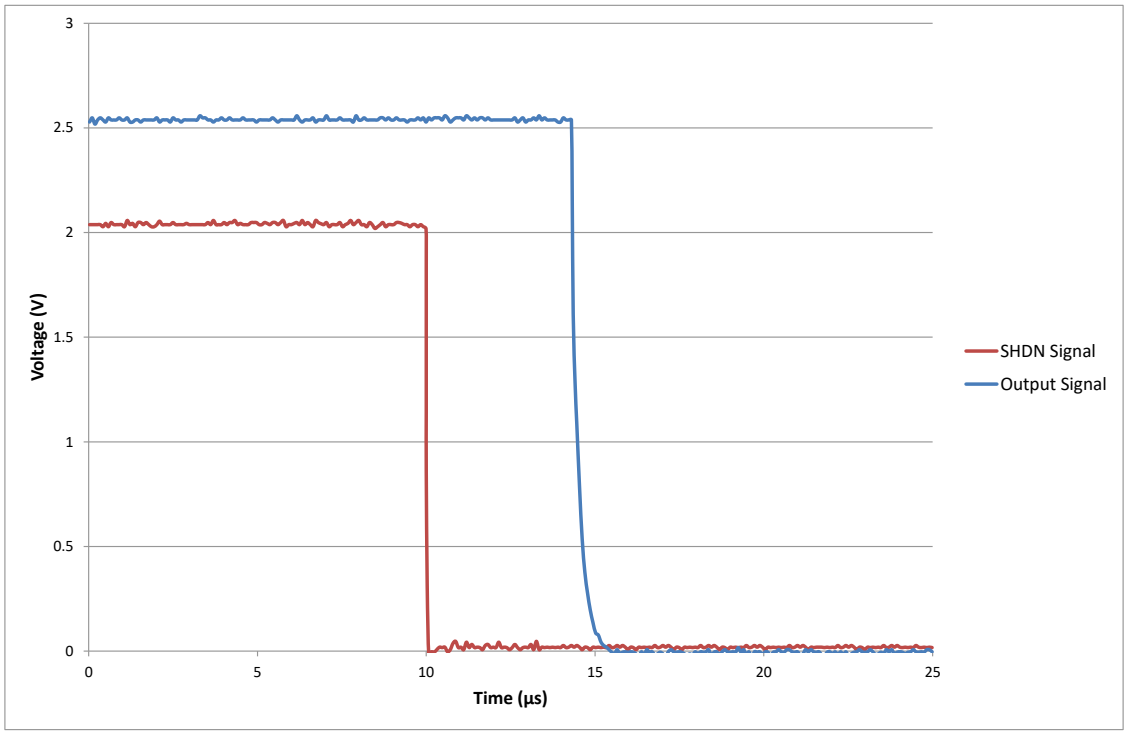

Figure 4-2. TLV9052S Shutdown

Not all amplifiers enable in the same fashion. Some amplifiers have internal circuitry which allows for a controlled power up response. This circuit is called a power-on reset (POR) circuit and its purpose is to hold the output

to a known state while the device enables. The POR function helps to prevent downstream logic from being inadvertently triggered.

For the TLV90xxS family of devices, the POR circuitry is non-functional when the device is powered off. The POR is activated when a startup current level is reached as the supply voltage is first applied. The POR circuit remains on while the amplifier is held in the shutdown state via the $\overline{SHDN}$ pin. Once the enable signal is sent to the $\overline{SHDN}$ pin, the POR circuitry holds the output until an internal biasing current reaches a threshold level. Then, the POR turns off and the amplifier is enabled.

In this manner, the TLV900xS, TLV905xS and TLV906xS devices can protect their outputs from unwanted behavior when the $\overline{SHDN}$ pin goes high to enable the device. Op amps that do not have POR circuitry may have a small glitch appear on the output when coming out of shutdown. This is more common in older parts.

5 Enable Time and Shutdown Time Factors

5.1 Quiescent Current

It is generally the case that amplifiers in the TLV90xxS family with higher quiescent current specifications will have faster enable and shutdown times. Note that this is not universally true for all amplifiers. There are a variety of factors that determine these times. But for these devices of similar structure, selecting a part with faster enable and shutdown times generally means the device will consume more power.

Table 5-1. Data Sheet Quiescent Current vs Enable and Shutdown Times

Device	Quiescent Current (I_Q)	Gain Bandwidth Product (GBW)	Enable Time (Full Shutdown, t_{on})	Enable Time (Partial Shutdown, t_{on})	Disable Time (t_{off})
TLV900xS	60 µA	1 MHz	70 µs	50 µs	4 µs
TLV905xS	330 µA	5 MHz	35 µs	10 µs	6 µs
TLV906xS	538 µA	10 MHz	10 µs	—	0.6 µs

5.2 Temperature

An amplifier's enable and disable times and behaviors also depend on other factors. For example, differing temperatures can provide small yet noticeable shifts in these times. In general, higher temperatures mean both faster enable times and faster shutdown times due to lower voltage threshold levels of the device's transistors. The threshold voltage is inversely proportional to the temperature. Note that this relationship is not exact due to higher order effects.

The table below illustrates this effect by showing and disable times of a TLV9002S device at key temperatures. This data was taken with channel 1 of the device in a unity gain buffer configuration with a 2.5-V input, a 10-kΩ load, and a $\overline{SHDN}$ pin that was toggled between 0 and 2 V. Channel 2 of the device was left always enabled in a unity gain configuration with a 2.5-V input and no external load. Notice that there is about a 15% difference in enable and shutdown times from –40°C to 125°C.

Table 5-2. TLV9002S Enable and Shutdown Times Across Temperature

—	–40°C	0°C	25°C	85°C	125°C
Enable Time	40.8 µs	39.4 µs	38.6 µs	36.8 µs	35.4 µs
Shutdown Time	3.38 µs	3.22 µs	3.22 µs	3.04 µs	2.88 µs

5.3 Load

Another important factor in determining the shutdown time of an amplifier is the output load. When the amplifier is disabled via the $\overline{SHDN}$ pin, there is some amount of charge available at the output pin. This output charge corresponds to the output voltage and is dependent on the load seen at the output. When the amplifier is in the shutdown state, the load is effectively comprised of the loading components, the feedback components, and the parasitic components seen at the amplifier's inputs and outputs. To complete the shutdown process, the output charge must dissipate so the output voltage may transition from the previous output voltage to the shutdown output voltage. Because this charge dissipates through the load, the shutdown time is dependent on the load component(s).

With this in mind, consider the following three scenarios for an amplifier in a unity gain buffer configuration: a purely resistive load, no load, and a purely capacitive load. Figure 5-1 displays an example graphic for this scenario. On the left is the amplifier during normal operation. On the right is the effective circuit which models the amplifier's behavior while the part is in shutdown. C_{CM} and C_{ID} model the common mode input capacitance and the differential input capacitance of the amplifier. C_{SHDN} and R_{SHDN} represent the output impedance of the part while in shutdown.

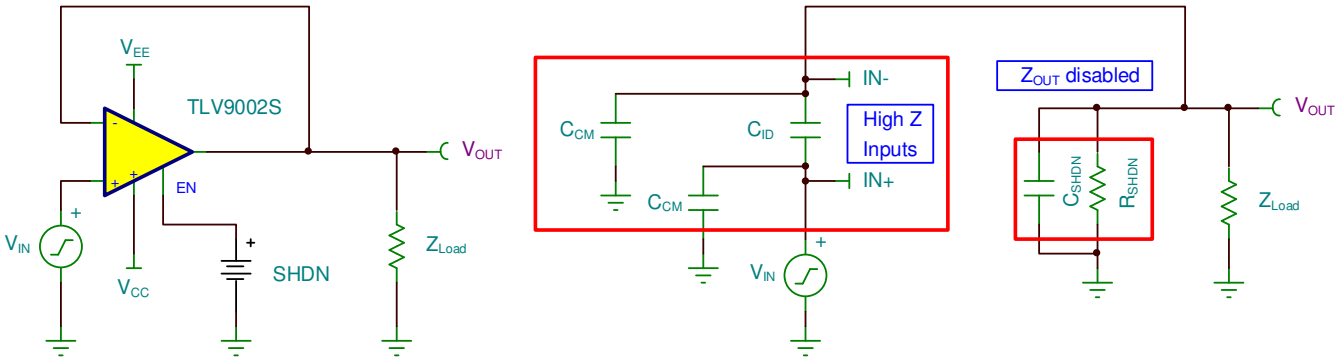

Figure 5-1. Buffer Circuit

In the case where the load component, Z_{LOAD}, is purely resistive and much smaller than R_{SHDN}, 10 kΩ for example, the amplifier will experience the fastest shutdown time for the three types of output loads. This is because the output charge is established only by the relatively small parasitic capacitances of the part, such as C_{SHDN}, and this charge has a purely resistive pulldown path to ground via the output load. The expected output signal during shutdown would look like a fast RC response from the starting output voltage to ground.

In the case where there is no output load, the output charge stored on the parasitic capacitances would still be relatively small. However, the charge would have to be displaced to ground through the very large R_{SHDN}, which forms a significant RC combination with the parasitic capacitances, or through parasitic and leakage paths in the amplifier. Thus, the expected shutdown time would be significantly longer for this load scenario. Note that parasitic board capacitance can contribute to this parasitic output capacitance.

The worst-case of the three scenarios, however, would be a purely capacitive load. For this case, even a typical load of 10 pF could significantly increase the time taken by the part to fully shut down. Under this condition, the output charge would be significantly higher than before with both the parasitic and load capacitances now storing output charge. Additionally, the load capacitor would further increase the size of the RC combination formed by R_{SHDN} and C_{SHDN} and offer no lower resistive path to ground. Consequently, the amplifier would take a long time to displace the charge stored at the output.

Figure 5-2 shows the shutdown times for the aforementioned configurations. All data was gathered using a TLV9062S on a 5-V single-supply in a unity buffer gain configuration with a 2.5-V input. The $\overline{SHDN}$ pin of channel 1 was toggled while channel 2 was left on. Note that the 10-kΩ load shutdown time is much faster than the other load times and that the curve nearly overlaps with the $\overline{SHDN}$ pin signal curve on this time scale.

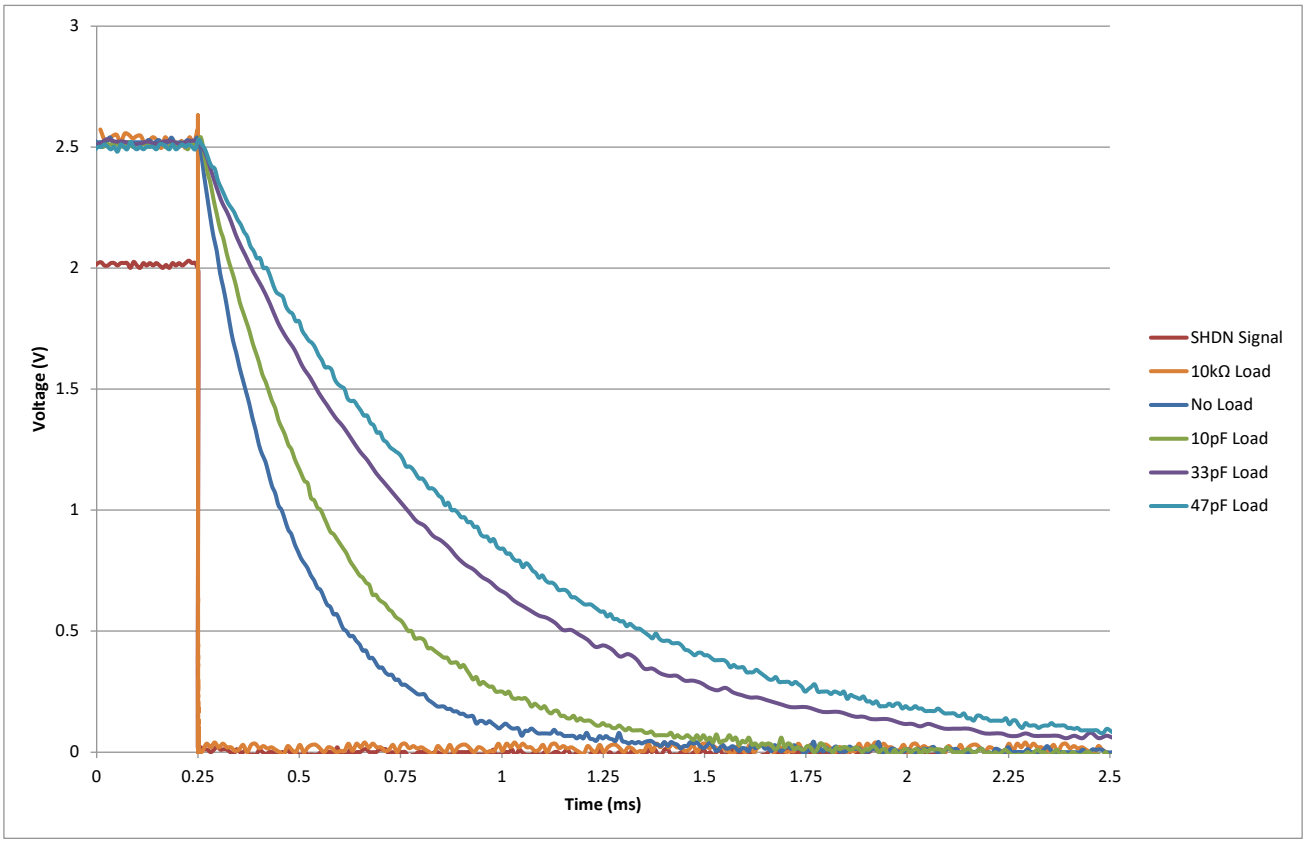

Figure 5-2. Load and Shutdown TLV9062S

Table 5-3. Load vs Experimental Enable and Shutdown Times for the TLV9062S

Output Load	Enable Time	Shutdown Time
10 kΩ	5.20 µs	604 ns
No Load	5.20 µs	536 µs
10 pF	5.20 µs	752 µs
33 pF	5.20 µs	1.35 ms
47 pF	5.20 µs	1.61 ms

5.4 Feedback Path

A similar analysis can be done to determine the effects of closed-loop impedance and gain on shutdown times. Consider three different types of closed-loop configurations:

- Unity gain buffer
- Non-inverting amplifier with a gain of 11 and feedback resistors of 18 kΩ (R_f) and 1.8 kΩ (R_i)
- Non-inverting amplifier with a gain of 11 and feedback resistors of 180 kΩ (R_f) and 18 kΩ (R_i)

An example circuit for the non-inverting configuration is shown in Figure 5-3. Again, the left portion of the image shows the configuration during enabled operation while the right portion shows the effective circuit when the amplifier is in shutdown mode.

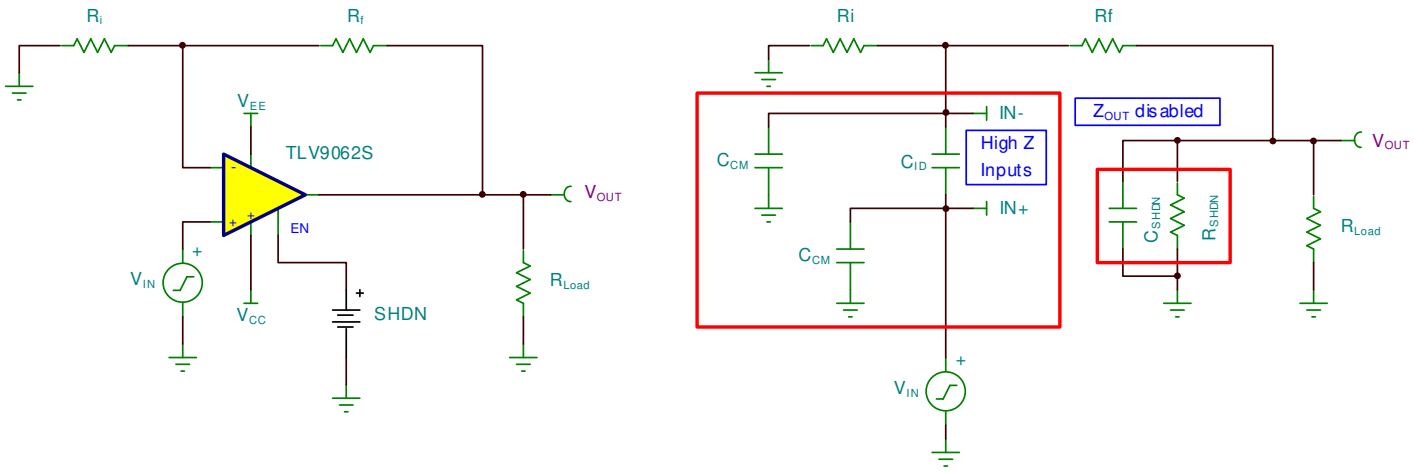

Figure 5-3. Non-Inverting Amplifier Circuit

Notice that when the amplifier is turned off, the feedback resistors, R_f and R_i, offer a resistive pulldown path to ground for the output. Similar to the case of the purely resistive load, this alternative path to ground can shorten shutdown times. However, the key here is that the shutdown time is heavily influenced by the total resistance in the feedback network and not by the gain set by the resistor ratio. In other words, the closed loop gain is not the dominant factor. The reason for this, as in the case of the output load examples, is that excessively large feedback resistors will form significant RC combinations with parasitic capacitances and lead to longer shutdown times.

Figure 5-4 displays the shutdown behavior of the TLV906xS for a unity gain buffer and gain of 11 V/V using two different feedback resistances. The measurements were taken on channel 1 while channel 2 remained on at all times.

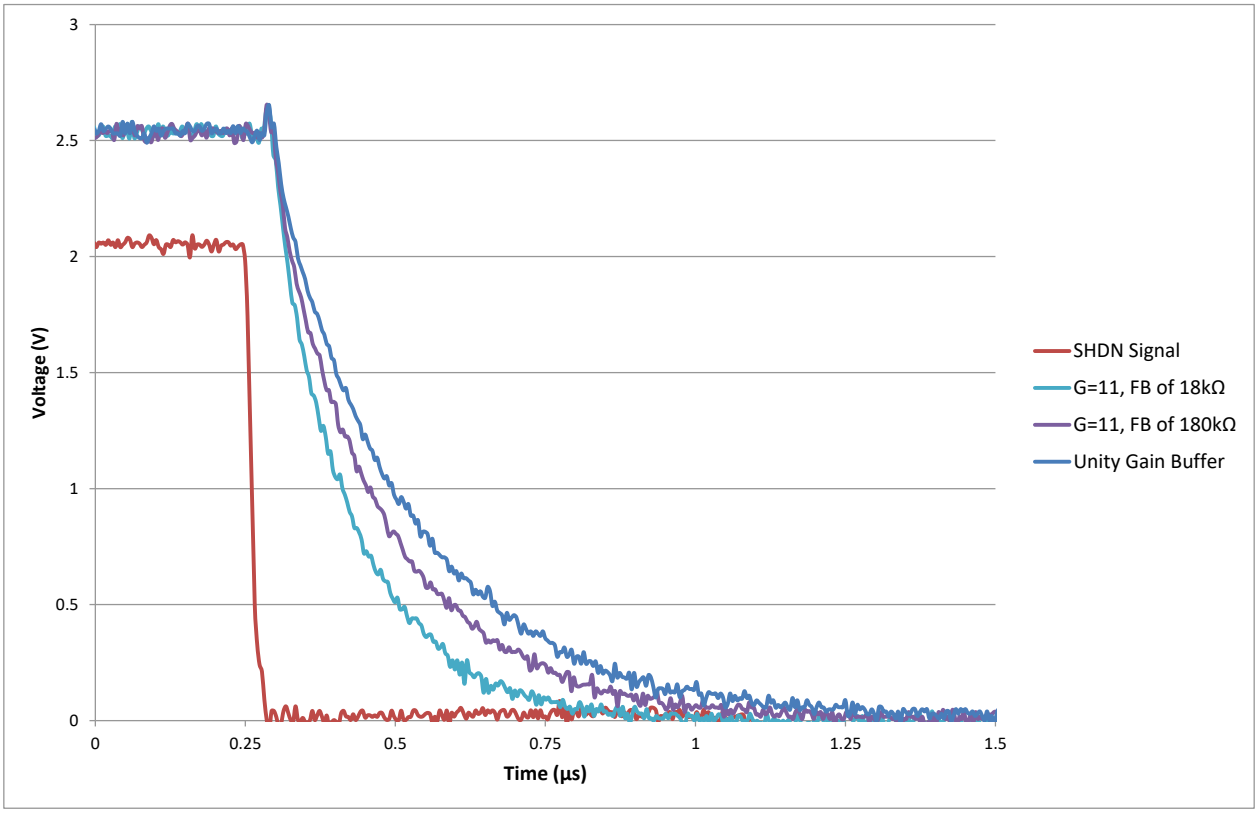

Figure 5-4. Closed-Loop Configuration and Shutdown TLV9062S

6 Impact on Commonly Used Circuit Configurations

Designers must take into account the effects of a disabled TLV90xxS device on their circuit, such as the input signal unexpectedly appearing at the output node due to the amplifier's parasitic input capacitance. This section will discuss how to model circuits with a disabled amplifier. It will also demonstrate the effects of a disabled amplifier on the performance for a few, common configurations.

To model a disabled amplifier in a circuit, one should:

1. Replace the inputs of the op amp with high impedance nodes.
2. Model the common mode and differential input capacitance of the amplifier with parasitic capacitors. Use the capacitances C_{CM} and C_{ID} provided in the data sheet for these components.
3. Model the output pin of the op amp as a resistor and a capacitor in parallel. Match their values to the Z_{SHDN} specification provided in the data sheet.

6.1 Inverting Amplifier Circuit

Figure 6-1 displays an inverting amplifier circuit configuration and its equivalent model when the amplifier is placed in the shutdown mode. Notice that op amps with shutdown functionality in an inverting amplifier configuration will not block the input signal from reaching the output of the circuit when the amplifier is disabled. This is due to the path that is present from the input to the output through the feedback network while the op amp is disabled.

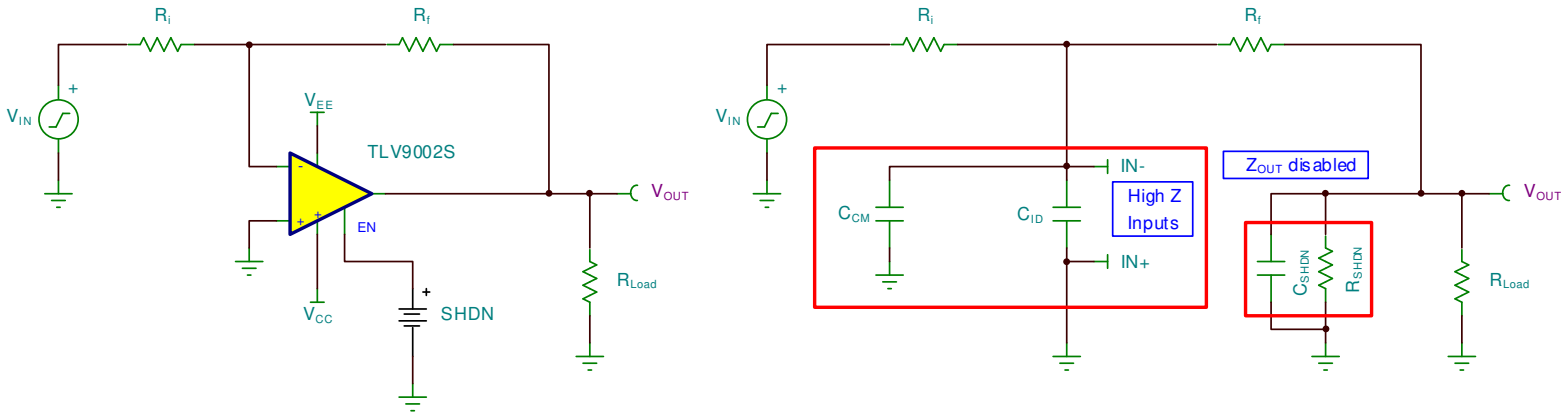

Figure 6-1. Inverting Amplifier Circuit

The fraction of the signal that is seen at the output will depend on the input signal frequency, the values of the resistors in the feedback network, the output load, the parasitic input capacitance and the output impedance of the amplifier when it is disabled. Consider an inverting amplifier circuit with a resistive load as an example. For this circuit, the voltage divider created by R_i+R_f and R_{Load} in parallel with R_{SHDN} will set the maximum amount of signal from V_{IN} that can be seen at V_{OUT}. Note that R_{SHDN} is typically very large, such that it can be ignored for this calculation. At high frequencies, the output impedance of the op amp itself will start to roll off, causing a low pass filter behavior at the output.

To see these effects simulated, consider an example of an inverting amplifier circuit in a gain of –1 V/V using the TLV9002S in shutdown mode. The circuit can be modeled using the setup in Figure 6-1. Set R_i and R_f to 1 kΩ and R_{Load} to 10 kΩ. From the TLV9002S data sheet specifications, C_{ID} is 1.5 pF, C_{CM} is 5 pF, C_{SHDN} is 2 pF, and R_{SHDN} is 10 GΩ. Now an AC simulation is run to measure the response of the circuit. The result is shown in Figure 6-2.

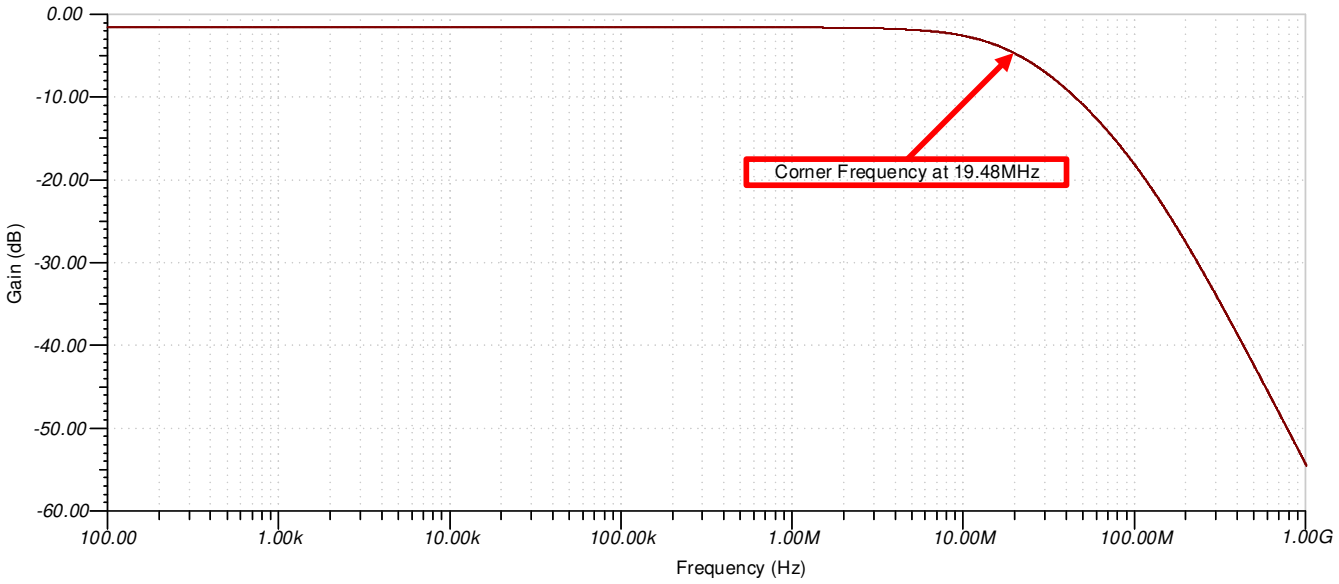

Figure 6-2. Inverting Amplifier AC Response

The simulation result shows a corner frequency of 19.48 MHz and a slope of –40 dB/dec at high frequencies due to the double pole. Notice that at low frequencies the input signal is attenuated by the ratio set by the sum of the feedback resistors and the load resistor. These form a DC path from input to output. Performing a voltage division calculation will yield an expected low frequency gain of 833 mV/V, or –1.58 dB. This demonstrates an important design consideration. This configuration may not significantly block or attenuate input signals from reaching the output while the amplifier is disabled. Thus, it is important to ensure that the output signal level during op amp shutdown is appropriate for the application.

6.2 Non-Inverting Amplifier Circuit

Figure 6-3 displays a non-inverting amplifier circuit configuration and its equivalent model when the amplifier is placed in the shutdown mode. In contrast to the inverting configurations, disabling the amplifier in a non-inverting configuration ensures there is no resistive path for the input signal to reach the output node. Thus, only a smaller portion of the input signal will appear on the output when the amplifier is disabled. It is important to remember that the amplifier does have a differential input capacitance (C_{ID}) that connects the input pins and provides a path for some signal to reach the output, especially at higher frequencies.

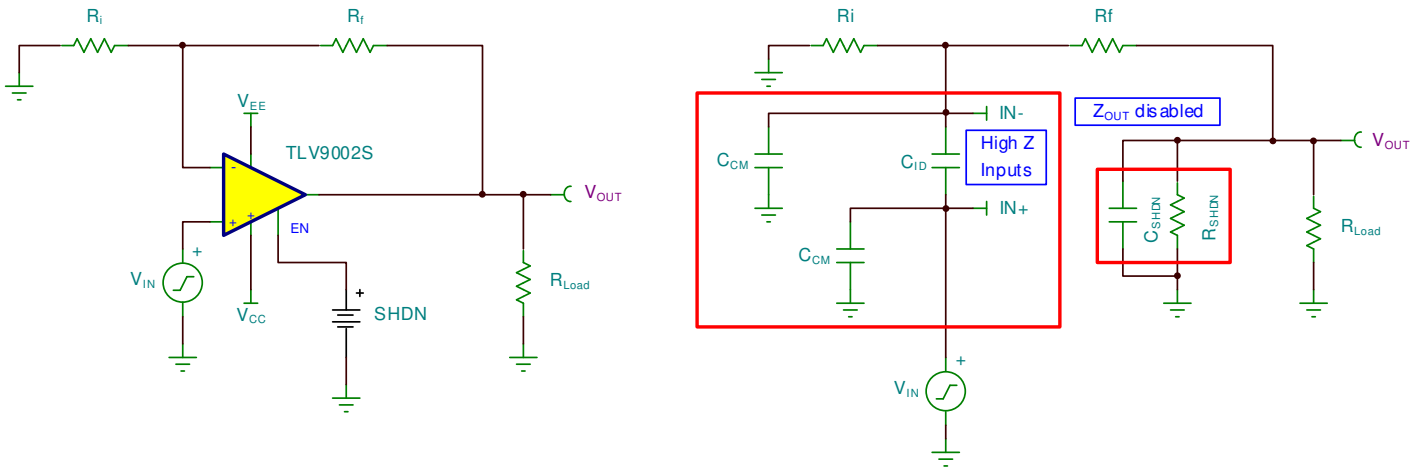

Figure 6-3. Non-Inverting Amplifier Circuit

Figure 6-4 displays the AC response of the output voltage while the amplifier is in shutdown. The amplifier is in a non-inverting configuration with a gain of +2 V/V. Once again, set R_i and R_f to 1 kΩ and R_{Load} to 10 kΩ. From the TLV9002S data sheet specifications, C_{ID} is 1.5 pF, C_{CM} is 5 pF, C_{SHDN} is 2 pF, and R_{SHDN} is 10 GΩ.

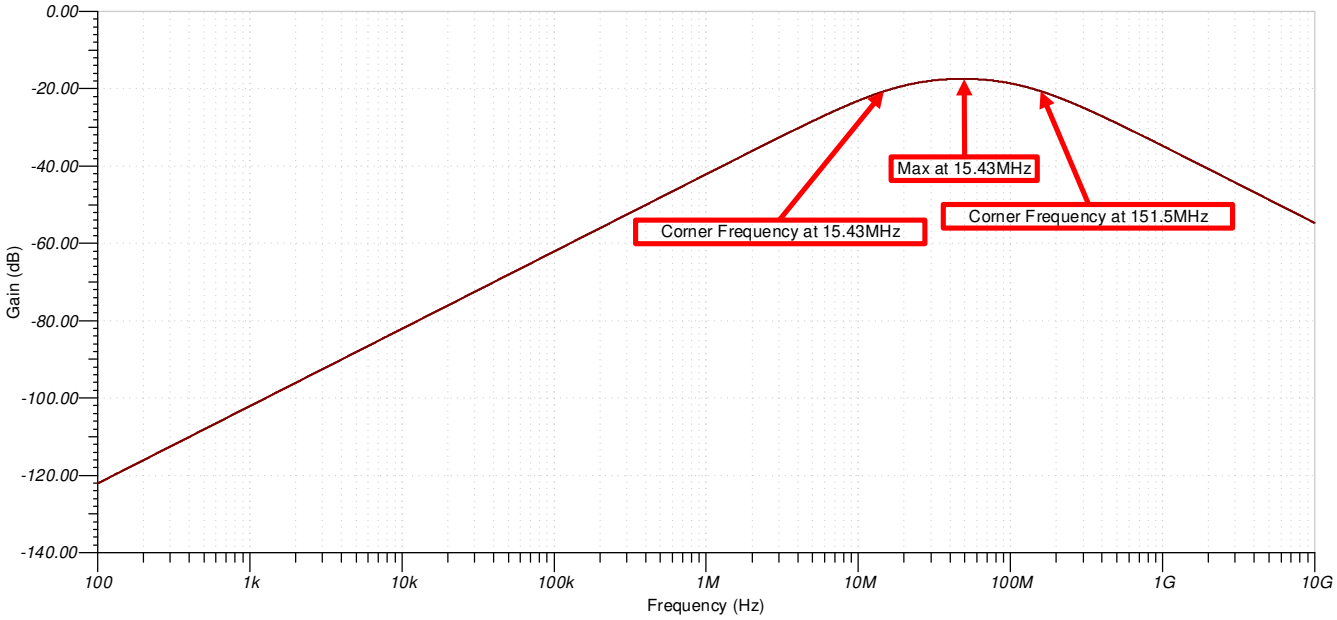

Figure 6-4. Non-Inverting Amplifier AC Response

The first corner frequency is 15.42 MHz, which is well outside the bandwidth of the TLV9002S. Comparing this plot to that of the inverting amplifier, it is apparent that the maximum gain of this configuration is smaller by about 15 dB. Furthermore, for the bandwidth of the TLV9002S, the gain of the non-inverting circuit is at least 40 dB smaller than that of the inverting circuit. This simulation affirms the theory that an amplifier in shutdown mode will limit the input signal from reaching the output more when in a non-inverting configuration than in an inverting configuration. Most of the time, non-inverting circuits can be used with minimal worry about signals coupling through to the output. However, it is still a good idea to verify the frequency response of the circuit at any frequencies of interest and ensure no downstream issues will arise.

6.3 Buffer Circuit

Figure 6-5 displays an amplifier circuit in the buffer configuration and its equivalent model when the amplifier is placed in the shutdown mode. Similarly to the non-inverting configuration, the input signal can pass through the differential input capacitance between the input terminals of the op amp.

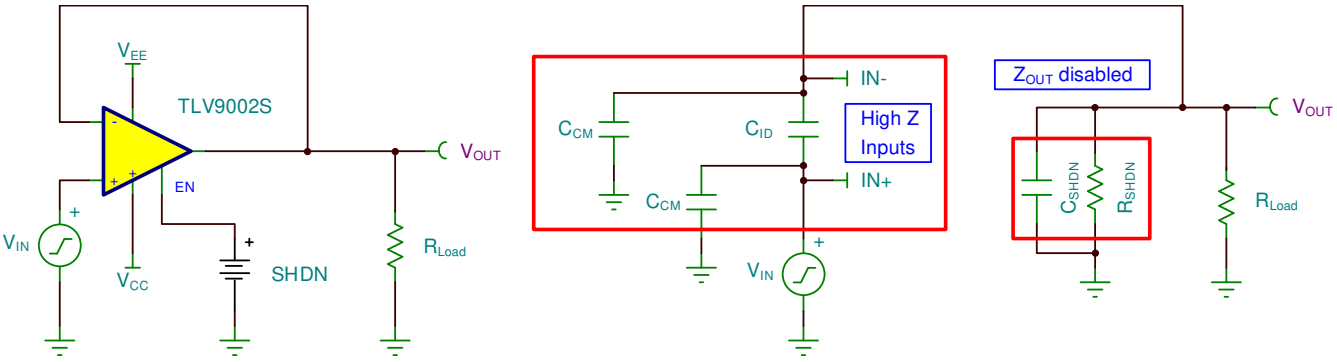

Figure 6-5. Buffer Circuit

This circuit behaves like a single stage high pass filter where the maximum level is set by the capacitor divider formed by C_{ID}, the C_{CM} parasitic capacitors, and C_{SHDN}. The pole frequency is set by the RC combination of the parallel capacitances of C_{CM}, C_{ID}, and C_{SHDN} with R_{Load}. The effect of R_{SHDN} is negligible assuming R_{SHDN} is much greater than R_{Load}, as is the case here.

C_{ID}, C_{CM}, C_{SHDN}, and R_{SHDN} cannot be changed as they are intrinsic values of the device. Thus, the output load must be modified in order to change the pole frequency. This can be verified through TINA-TI SPICE simulation. Again, the TLV9002S data sheet is used for the values of C_{ID}, C_{CM}, C_{SHDN}, and R_{SHDN} with a 10-kΩ load.

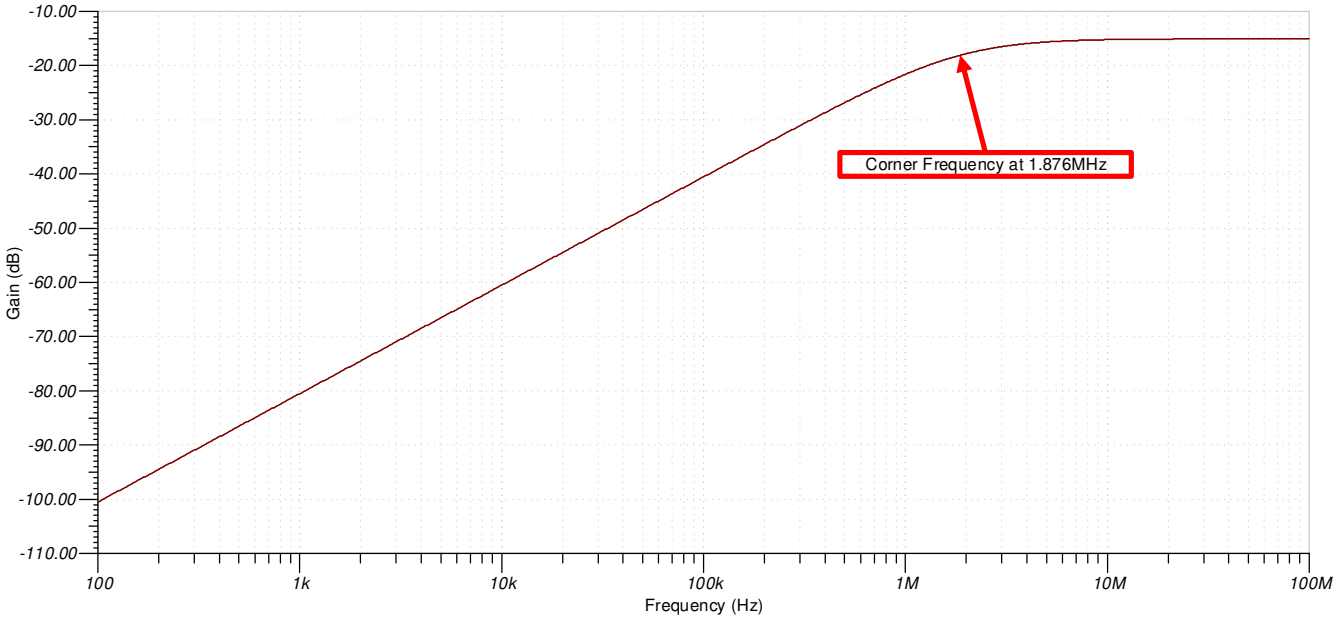

Figure 6-6. Buffer AC Response

Figure 6-6 shows the frequency response of this circuit. In this example scenario, input signals will be attenuated at about –15 dB for frequencies beyond the bandwidth of the TLV9002. However, this may not be the case for higher bandwidth devices. For such devices, high frequency noise can couple through to the output and, depending on the application, impact downstream circuitry.

7 Advanced Circuit Functionality Using Amplifiers With Shutdown

Analog signal chains often have a variety of analog input signals that are passed to an analog-to-digital controller (ADC). Oftentimes, there are more input signals than ADC input channels available, creating the need for an input signal multiplexer. Using a dedicated multiplexer for such a role has several advantages. For example, using a MUX can be simpler, require less control signals, and allow the user the option for both voltage and current multiplexing.

However, multiplexers may require amplifiers at both their inputs and outputs. Op amps at the input of a MUX help to protect any sensors or early portions of the signal chain from MUX switching and/or charge injection. Op amps at the output of a MUX are used to provide a low-impedance voltage drive for the inputs of the ADC. Therefore, using one or more multiplexers may entail a significant increase in the number of op amps required in an analog signal chain.

Operational amplifiers with shutdown capabilities may serve as an alternative to multiplexers in such cases. Because multi-channel shutdown op amps have the ability to selectively enable and disable channels, they can effectively multiplex a signal without needing additional amplifiers at their input(s) and output(s). Circuit designers can thus reduce their overall component count. When doing so however, the potential issues caused by shoot through current and input diode clamping must be taken into account. For more information on these and other topics on the subject, see TI's technical note on *Using Operational Amplifiers as Multiplexers in Cost-Optimized Designs*.

8 Conclusion

Op amps with shutdown functionality offer a great blend of performance during operation and power-saving during shutdown. However, a grasp of the finer details of these parts should be developed before they are used in designs. This application note explored the definitions of common terms, real world cause-effect relationships, and modeling techniques for these parts. With the help of this document, designers should feel confident incorporating the TLV90xxS family of parts into their designs.

9 References

1. To learn more about the design of many of these and other amplifier configurations, consult our *Analog engineer's circuit cookbook on amplifiers*.
2. For a large collection of amplifier circuits, see our *AN-31 amplifier circuit collection* application note.
3. Alternatively, more information on some of these circuits can be found in our app note entitled, *AN-20 an applications guide for op amps*.
4. To learn more about the characteristics of amplifiers, common techniques used in amplifier circuit design, and a variety of other amplifier topics, consult our Texas Instruments Precision Labs video series on amplifiers.
5. For specific questions regarding your design, reach out to our engineers via e2e, our online forum.
6. For a handy reference guide for your analog designs, check out the *Analog Engineer's Pocket Reference Guide* available for free in pdf form.
7. Use our Analog Engineer's Calculator to help crunch design equations.
8. Check out our Amplifier's Product Page to quickly sort through our products and find the amplifier(s) that best fit your needs.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2022) to Revision B (June 2022)	Page
• Updated Table 5-1 product specifications	8

Changes from Revision * (December 2019) to Revision A (March 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	3

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