*Analog Engineer's Circuit*

# *Voltage-to-current (V-I) converter circuit with MOSFET*

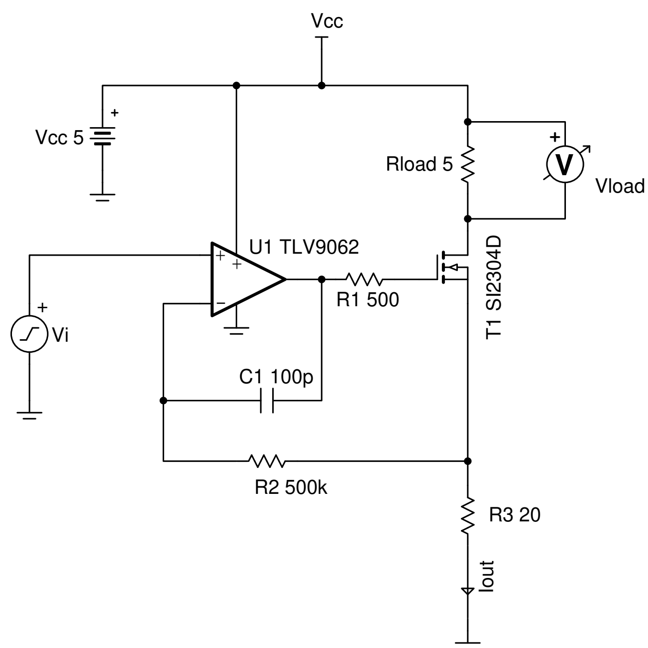
*Amplifiers*

## Design Goals

| Input | | Output | | Supply | |
|---|---|---|---|---|---|
| $V_{iMin}$ | $V_{iMax}$ | $I_{oMin}$ | $I_{oMax}$ | Vcc | Vee |
| 0V | 2V | 0mA | 100mA | 5V | 0V |

## Design Description

This single-supply, low-side, V-I converter delivers a well-regulated current to a load which can be connected to a voltage greater than the op-amp supply voltage. The circuit accepts an input voltage between 0V and 2V and converts it to a current between 0mA and 100mA. The current is accurately regulated by feeding back the voltage drop across a low-side current-sense resistor, $R_3$, to the inverting input of the op amp.




## Design Notes

1. A device with a rail-to-rail input (RRI) or common-mode voltage that extends to GND is required.
2. $R_1$ helps isolate the amplifier from the capacitive load of the MOSFET gate.
3. Feedback components $R_2$ and $C_1$ provide compensation to ensure stability during input or load transients, which also helps reduce noise. $R_2$ provides a DC feedback path directly at the current setting resistor ($R_3$) and $C_1$ provides a high-frequency feedback path that bypasses the MOSFET.
4. The input bias current will flow through $R_2$, which will cause a DC error. Therefore, ensure that this error is minimal compared to the offset voltage of the op amp.
5. Use the op amp in a linear operating region. Linear output swing is usually specified under the $A_{OL}$ test conditions provided in the op amp data sheet.

### Design Steps

1. Determine the transfer function.

$$I_o = \frac{V_i}{R_3}$$

2. Calculate the sense resistor, $R_3$.

$$R_3 = \frac{V_{iMax} - V_{iMin}}{I_{oMax} - I_{oMin}} = \frac{2V - 0V}{100mA - 0mA} = 20\Omega$$

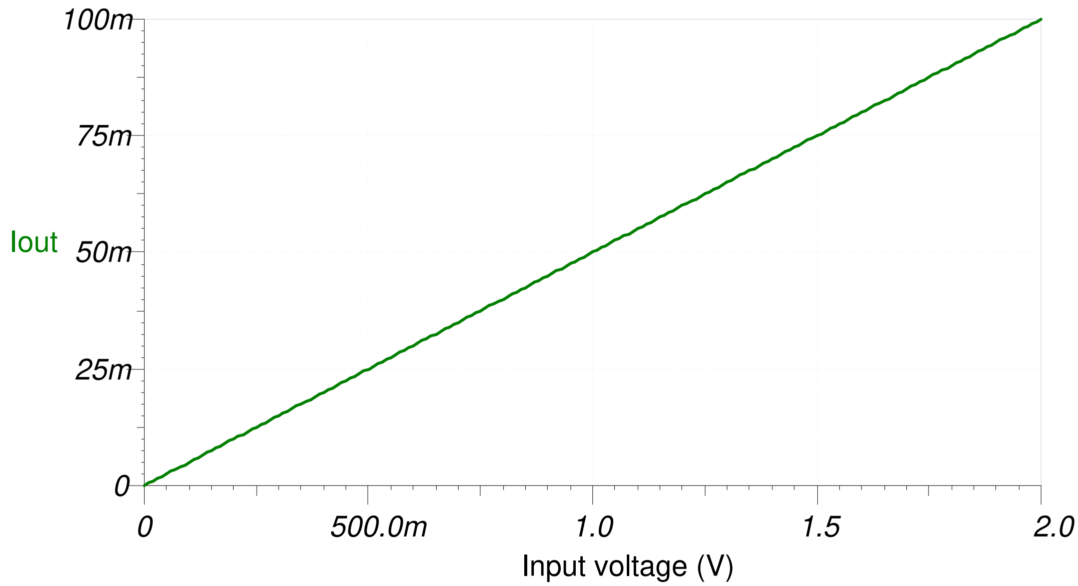
3. Calculate the maximum power dissipated into the sense resistor, $R_3$, to ensure the resistor power ratings are not exceeded.

$$P_{R_3} = \frac{V_{iMax}^2}{R_3} = \frac{2V^2}{20\Omega} = 0.2W$$

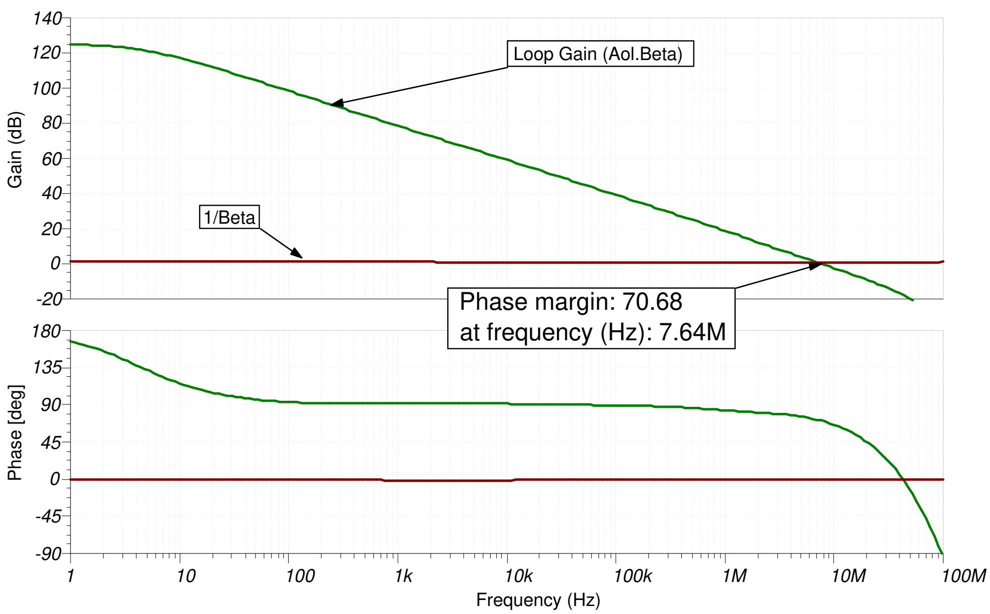
4. See the Design References section, [2] for the design procedure on how to properly size the compensation components, $R_1$, $R_2$, and $C_1$.

## Design Simulations

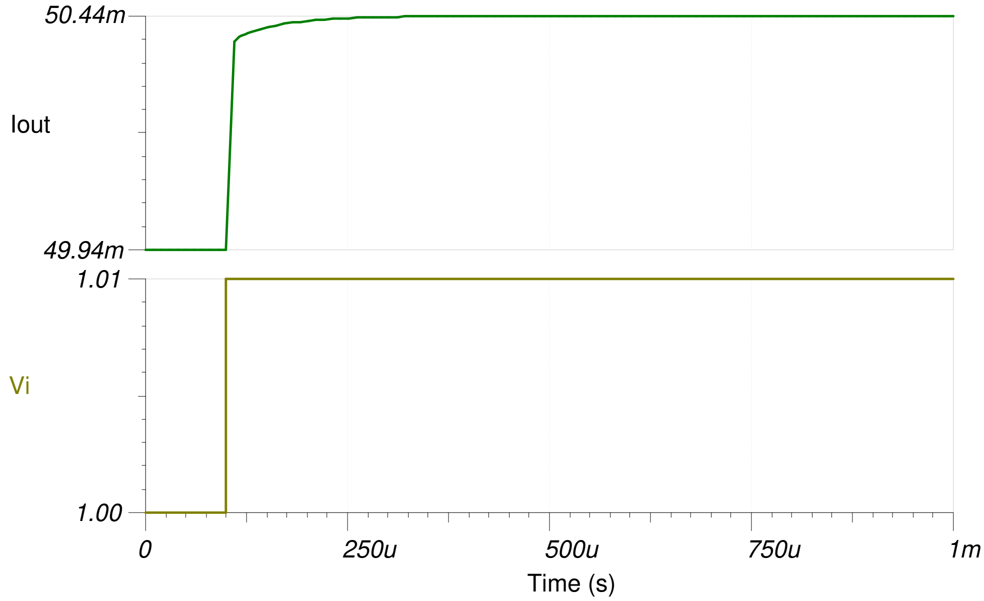
### DC Simulation Results




### Loop Stability Simulation Results

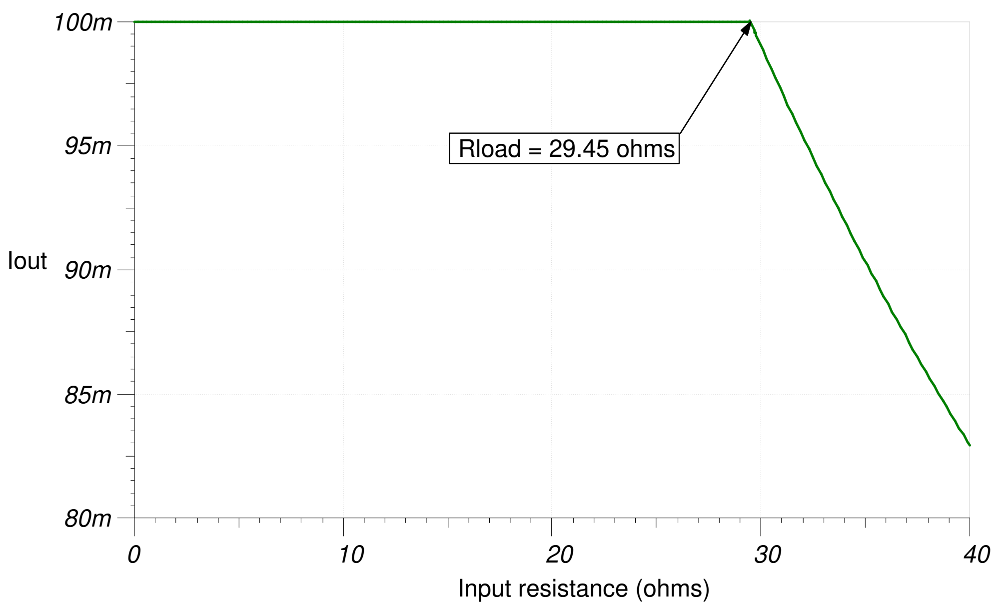


### Step Response




### Compliance Voltage

Set output to full-scale (100 mA) and test the maximum load resistance.



## Design References

1. See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.
2. TI Precision Labs

## Design Featured Op Amp

| TLV9062 | |
|---|---|
| $V_{ss}$ | 1.8 V to 5.5 V |
| $V_{inCM}$ | Rail-to-rail |
| $V_{out}$ | ($V_{cc}$ + 60mV) to (Vee – 60mV) at $R_L$ = 2kΩ |
| $V_{os}$ | 1.6mV |
| $I_q$ | 0.538mA |
| $I_b$ | 0.5pA |
| UGBW | 10MHz |
| SR | 6.5V/µs |
| #Channels | 1, 2, 4 |
| www.ti.com/product/TLV9062 | |

## Design Alternate Op Amp

| | TLV9042 | OPA2182 |
|---|---|---|
| $V_{ss}$ | 1.2V to 5.5V | 4.5V to 36V |
| $V_{inCM}$ | Rail-to-rail | ($V_{ee}$ – 0.1V) to ($V_{cc}$ – 2.5V) |
| $V_{out}$ | Rail-to-rail | Rail-to-rail |
| $V_{os}$ | ±0.6mV | ±0.45µV |
| $I_q$ | 0.01mA | 0.85mA |
| $I_b$ | ±1pA | ±50pA |
| UGBW | 350kHz | 5MHz |
| SR | 0.2V/µs | 10V/µS |
| #Channels | 1,2,4 | 2 |
| | www.ti.com/product/TLV9042 | www.ti.com/product/OPA2182 |

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