Analog Engineer's Circuit

Voltage-to-current (V-I) converter circuit with a Darlington transistor

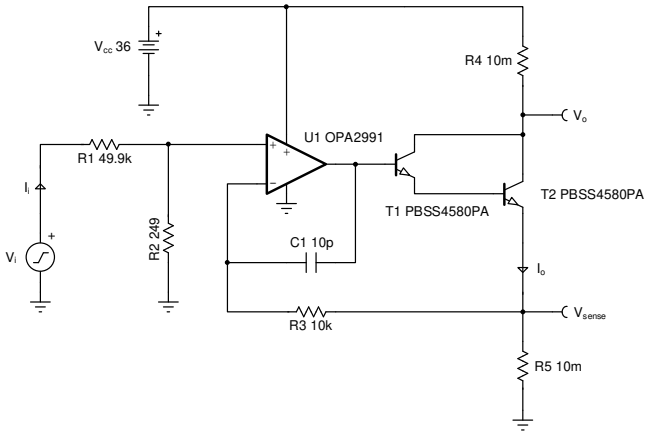
Amplifiers

Design Goals

Input			Output			Supply	
V_{iMin}	V_{iMax}	I_{iMax}	I_{oMin}	I_{oMax}	P_{R5Max}	V_{cc}	V_{ee}
0V	10V	200µA	0A	5A	0.25W	36V	0V

Design Description

This high-side voltage-to-current (V-I) converter delivers a well-regulated current to a load, R_4. The circuit accepts an input voltage from 0V to 10V and converts it to an output current from 0A to 5A. The current is regulated by feeding the voltage across a low-side, current-sense resistor back to the op amp. The output Darlington pair allows for higher current gain than when using a single, discrete transistor.



Design Notes

1. A resistor divider, formed by R_1 and R_2, is implemented at the input to limit the full-scale voltage at the non-inverting terminal of the amplifier and the output sense resistor (R_5).
2. The high current gain of the Darlington pair reduces the demand on the output current of the op amp.
3. Smaller values of R_4 and R_5 lead to an increased load compliance voltage and a reduction in power dissipated in the full-scale, output state.
4. Feedback components R_3 and C_1 provide frequency compensation to ensure the stability of the circuit during transients. They also help reduce noise. R_3 provides a DC feedback path directly at the current setting resistor, R_5, and C_1 provides a high-frequency feedback path that bypasses the NPN pair.
5. The input bias current will flow through R_3, which will cause a DC error. Therefore, ensure that this error is minimal compared to the offset voltage of the op amp.
6. Select an op amp whose linear output voltage swing includes at least $2 \times V_{be}+V_{sense}$. The output voltage of the op amp will be greater than the voltage at the sense resistor by approximaly double the base-to-emitter voltage, V_{be}.
7. Use the op amp in its linear operating region, specified under the A_{OL} test conditions of the data sheet.
8. If needed, an isolation resistor may be placed between the high-frequency feedback path and the base of T1 for stability.

Design Steps

The transfer function of this circuit is provided in the following steps:

$$I_o = V_i \times \frac{R_2}{R_5 \times (R_1 + R_2)}$$

1. Using the specifications for the maximum output power dissipation and the maximum output current, determine the maximum value of V_{sense}.

$$V_{R5Max} = V_{senseMax} = \frac{P_{R5Max}}{I_{oMax}} = \frac{0.25\ W}{5A} = 50mV$$

2. Calculate the sense resistance, R_5.

$$R_5 = \frac{V_{senseMax}}{I_{oMax}} = \frac{50mV}{5A} = 10m\Omega$$

3. Select values for R_1 and R_2 based on the maximum allowable input current, I_{iMax}, and the desired $V_{senseMax}$ voltage.

$$R_1 = \frac{V_{senseMax}}{I_{iMax}} = \frac{50mV}{200\mu A} = 250\Omega \approx 249\Omega (\text{Standard Value})$$

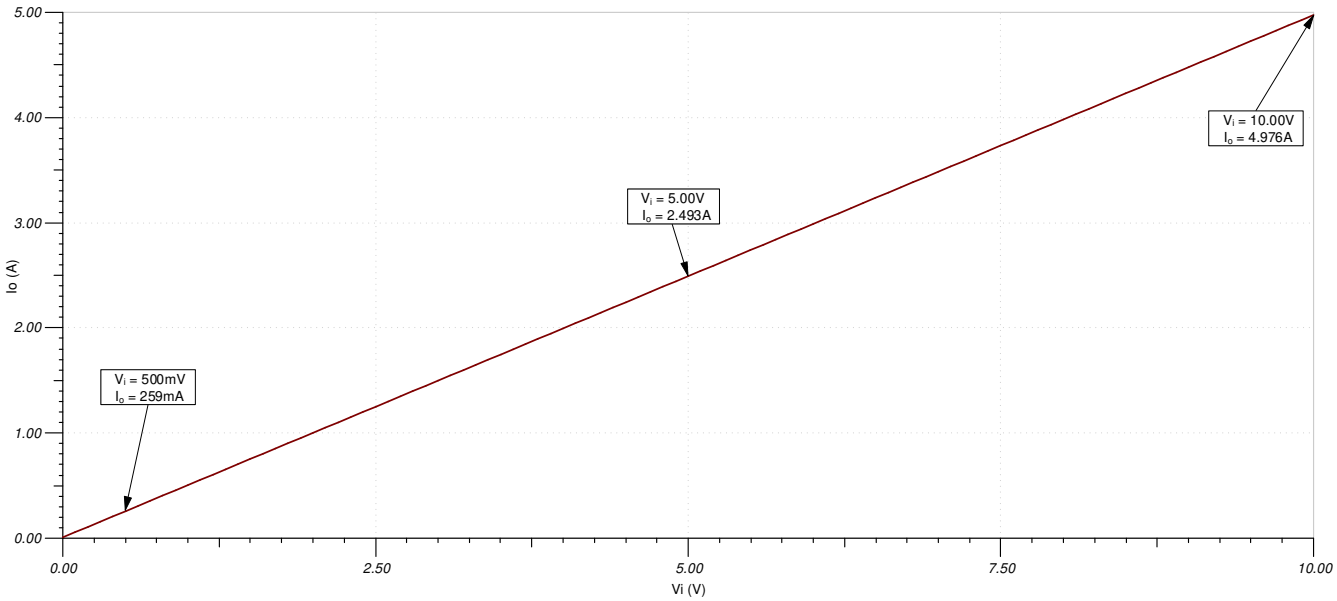
$$V_{senseMax} = V_{iMax} \times \left(\frac{R_2}{R_1 + R_2}\right)$$

$$R_2 = 49.6k\Omega \approx 49.9k\Omega\ (\text{Standard Value})$$

4. See the Design References section [2] for the design procedure on how to properly size the compensation components, R_3 and C_1.

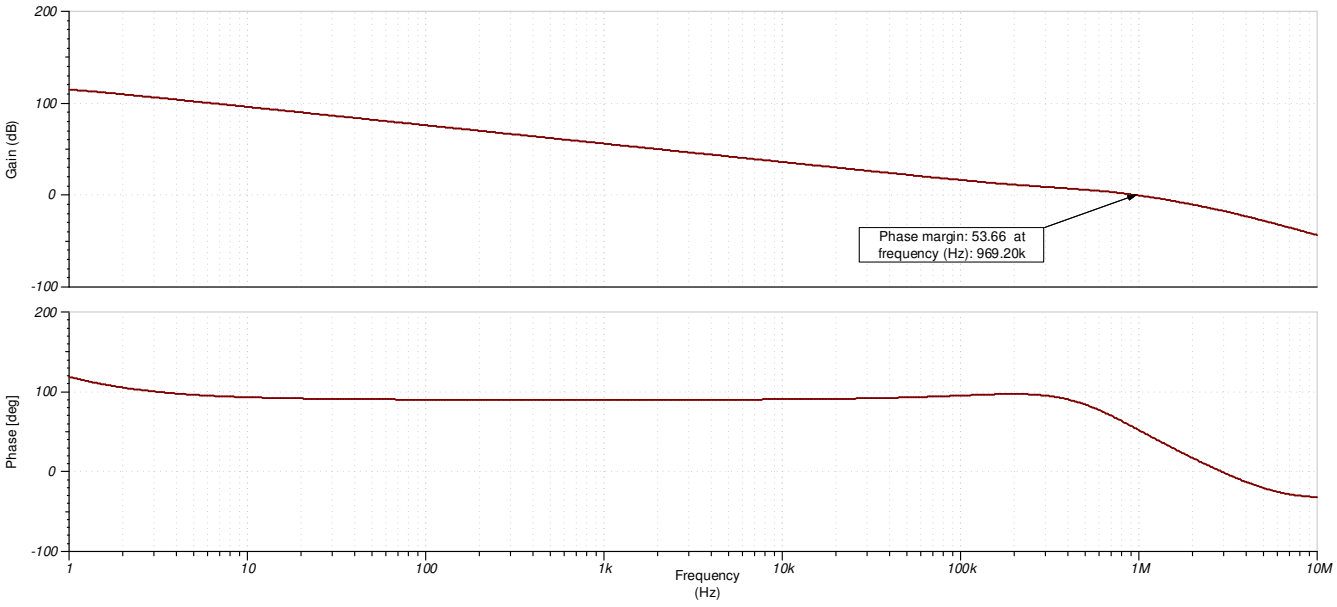
Design Simulations

DC Simulation Results

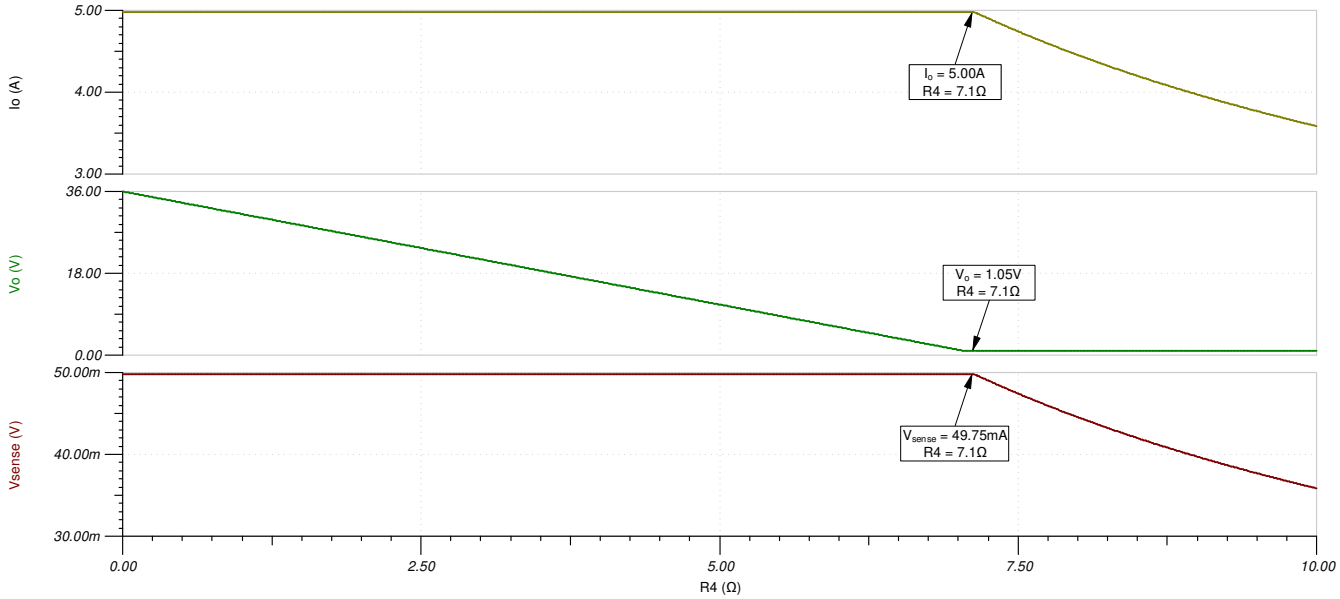


Loop Stability Simulation Results

Loop gain phase is 53 degrees.



Compliance Voltage Simulation Results



Design References

1. See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.
2. TI Precision Labs

Design Featured Op Amp

OPA2991	
V_{ss}	2.7V to 40V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	125µV
I_q	560µA
I_b	10pA
UGBW	4.5MHz
SR	21V/µs
#Channels	1, 2, 4
www.ti.com/product/opa2991	

Design Alternate Op Amp

OPA197	
V_{ss}	4.5V to 36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	25µV
I_q	1mA
I_b	5pA
UGBW	10MHz
SR	20V/µs
#Channels	1, 2, 4
www.ti.com/product/opa197	

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265