Analog Engineer's Circuit

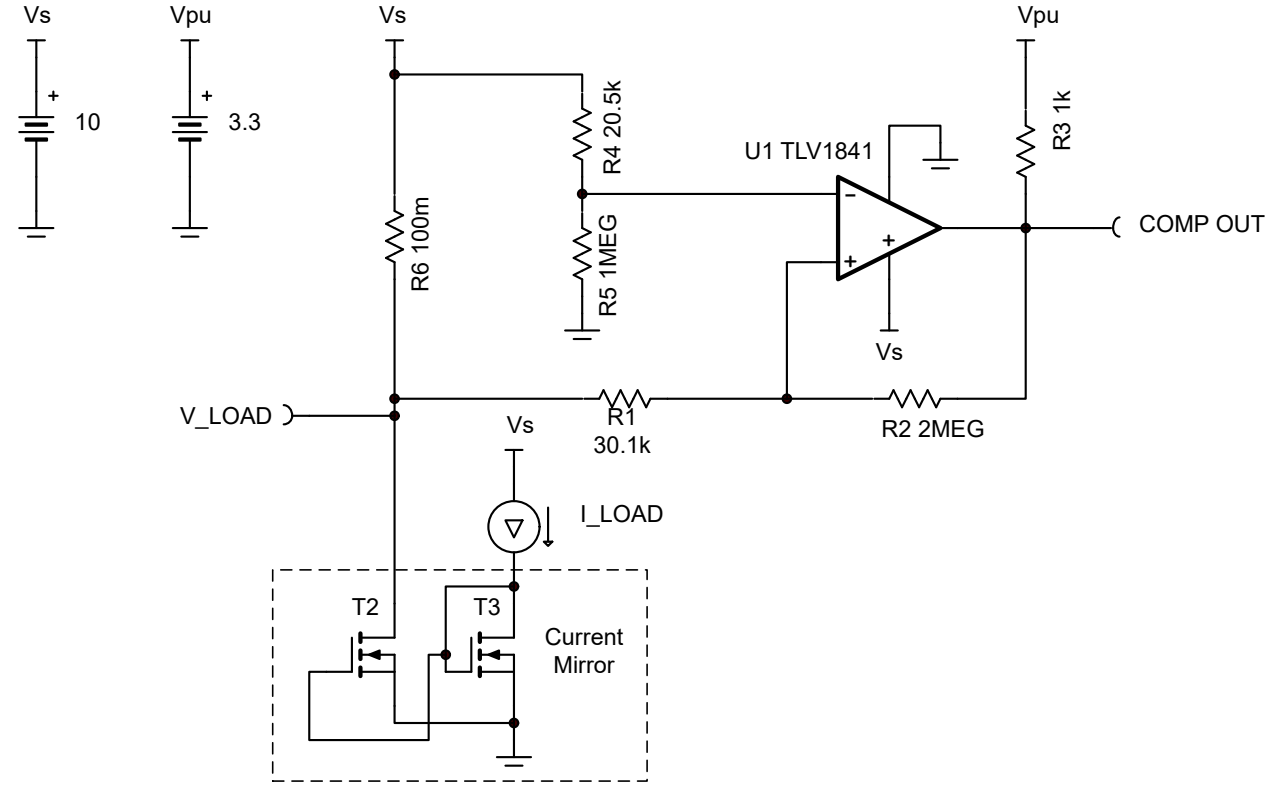
High-Side Current Sensing With Comparator Circuit

Design Goals

Load Current (I_L)		System Supply (V_S)	Comparator Output Status	
Overcurrent (I_{OC})	Recovery Current (I_{RC})	Typical	Overcurrent	Normal Operation
1A	0.5A	10V	V_{OL} < 0.4V	V_{OH} = V_{PU} = 3.3V

Design Description

This high-side, current sensing circuit uses one comparator with a rail-to-rail input common-mode range to create an overcurrent alert (OC-Alert) signal at the comparator output (COMP OUT) if the load current rises above 1A. The OC-Alert signal in this implementation is active low. So when the 1A threshold is exceeded, the comparator output goes low. Hysteresis is implemented such that OC-Alert returns to a logic high state when the load current reduces to 0.5A (a 50% reduction). This circuit utilizes an open-drain output comparator to level shift the output high logic level for controlling a digital logic input pin. For applications needing to drive the gate of a MOSFET switch, a comparator with a push-pull output is preferred.



Design Notes

1. Select a comparator with rail-to-rail input common-mode range to enable high-side current sensing.
2. Select a comparator with an open-drain output stage for level-shifting.
3. Select a comparator with low input offset voltage to optimize accuracy.
4. Calculate the value for the shunt resistor (R_6) so the shunt voltage (V_{SHUNT}) is at least ten times larger than the comparator offset voltage (V_{IO}).

Design Steps

1. Select the value of R_6 so V_{SHUNT} is at least 10 times greater than the comparator input offset voltage (V_{IO}). Making R_6 very large improves OC detection accuracy but reduces supply headroom.

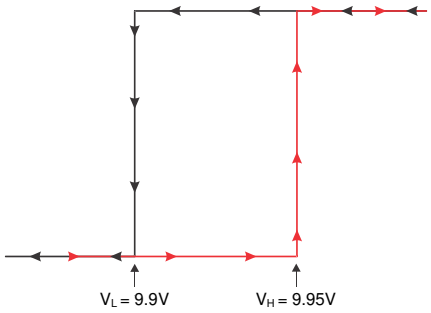
$$V_{SHUNT} = (I_{OC} \times R_6) \geq 10 \times V_{IO} = 55mV$$

$$\text{set } R_6 = 100m\Omega \text{ for } I_{OC} = 1A \text{ and } V_{IO} = 5.5mV$$

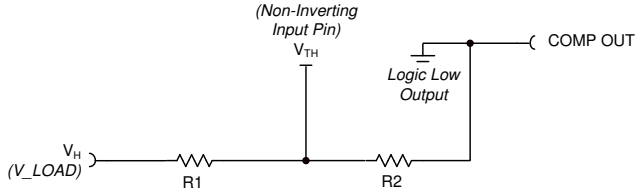
2. Determine the desired switching thresholds for when the comparator output transitions from high-to-low (V_L) and low-to-high (V_H). V_L represents the threshold when the load current crosses the OC level, while V_H represents the threshold when the load current recovers to a normal operating level.

$$V_L = V_S - (I_{OC} \times R_6) = 10 - (1 \times 0.1) = 9.9V$$

$$V_H = V_S - (I_{RC} \times R_6) = 10 - (0.5 \times 0.1) = 9.95V$$

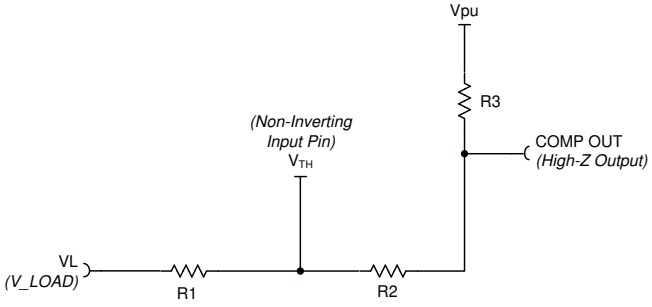


3. With the non-inverting input pin of the comparator labeled as V_{TH} and the comparator output in a logic low state (ground), derive an equation for V_{TH} where V_H represents the load voltage (V_{LOAD}) when the comparator output transitions from low to high. Note that the simplified diagram for deriving the equation shows the comparator output as ground (logic low).



$$V_{TH} = V_H \times \left(\frac{R_2}{R_1 + R_2}\right)$$

4. With the non-inverting input pin of the comparator labeled as V_{TH} and the comparator output in a high-impedance state, derive an equation for V_{TH} where V_L represents the load voltage (V_{LOAD}) when the comparator output transitions from high to low. Applying *superposition* theory to solve for V_{TH} is recommended.



$$V_{TH} = V_L \times \left(\frac{R_2 + R_3}{R_1 + R_2 + R_3}\right) + V_{PU} \times \left(\frac{R_1}{R_1 + R_2 + R_3}\right)$$

5. Eliminate variable V_{TH} by setting the two equations equal to each other and solve for R_1. The result is the following quadratic equation. Solving for R_2 is less desirable since there are more standard values for small resistor values than the larger ones.

$$0 = (V_{PU}) \times {R_1}^2 + \left(V_{PU} \times R_2 + V_L \times \left(R_3 + R_2\right) - V_H \times R_2\right) \times R_1 + \left(V_L - V_H\right) \times \left({R_2}^2 + R_2 \times R_3\right)$$

6. Select values for R3 and R2. R_3 is significantly smaller than R_2 (R_3 << R_2). Avoid increasing R_3 since an increase in R_3 causes the comparator logic high-output level to increase beyond V_{PU}. For example, increasing R_3 to a value of 100kΩ can cause the logic high output to be 3.6V. In this case, select R_2 = 2M and R_3 = 1kΩ.

$$R_2 = 2M\Omega$$

$$R_3 = 1k\Omega$$

7. Calculate R_1 after substituting in numeric values for V_{PU}, R_2, V_L, V_H, and R_3. For this design, set V_{PU} = 3.3, R_2 = 2M, V_L = 9.9, V_H = 9.95, and R_3 = 1kΩ.

$$0 = (3.3) \times {R_1}^2 + \left(6.591M\right) \times R_1 - \left(200.1G\right)$$

$$\text{the positive root for } R_1 = 29.9k\Omega$$

$$\text{using standard } 1\% \text{ resistor values, } R_1 = 30.1k\Omega$$

8. Calculate V_{TH} using the equation derived in *Design Step 3*; use the calculated value for R_1. Note that V_{TH} is less than V_L since V_{PU} is less that V_L.

$$V_{TH} = V_H \times \left(\frac{R_2}{R_1 + R_2}\right) = 9.802V$$

9. With the inverting terminal labeled as V_{TH}, derive an equation for V_{TH} in terms of R_4, R_5, and V_S.

$$V_{TH} = V_S \times \left(\frac{R_5}{R_4 + R_5}\right)$$

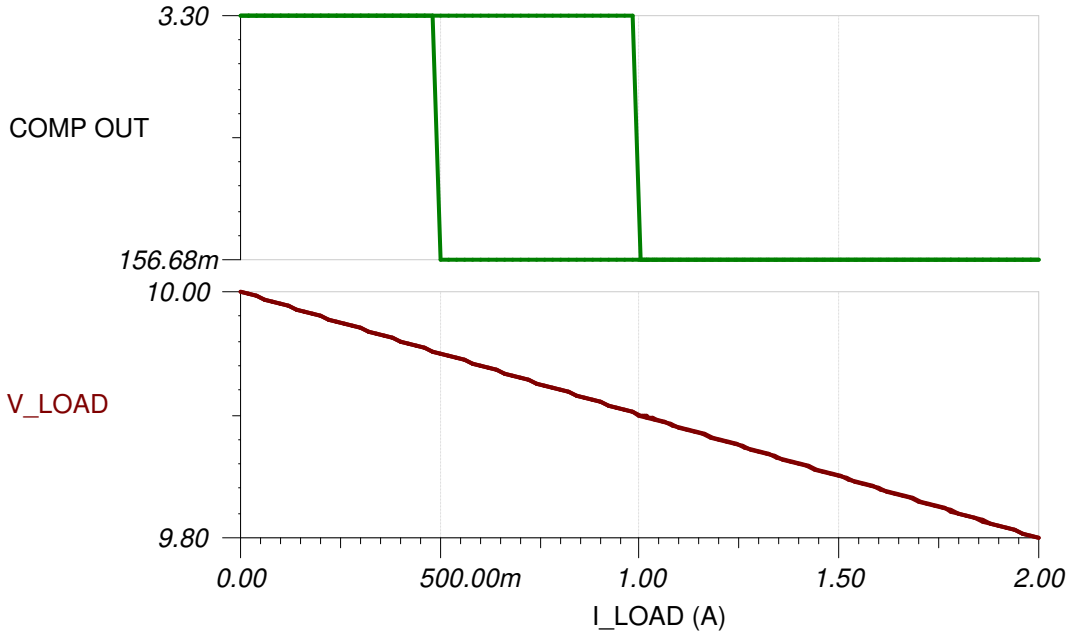
10. Calculate R_4 after substituting in numeric values R_5 = 1M, V_S = 10, and the calculated value for V_{TH}.

$$R_4 = \left(\frac{R_5 \times (V_S - V_{TH})}{V_{TH}}\right) = 20.15k\Omega$$

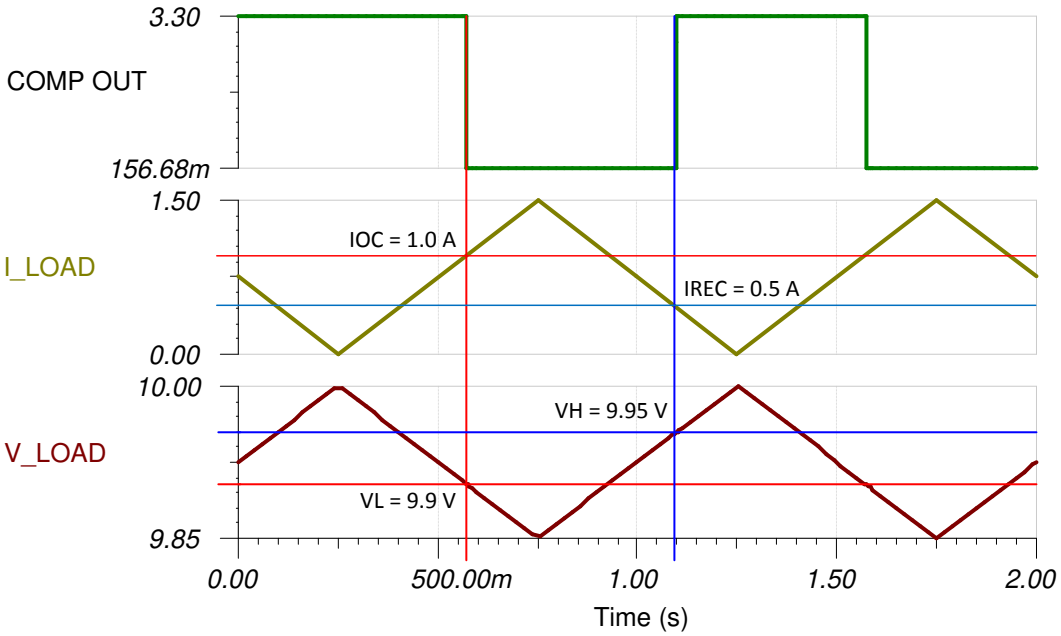
$$\text{using standard } 1\% \text{ resistor values, } R_4 = 20.5k\Omega$$

Design Simulations

DC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See Circuit SPICE Simulation File SLOM456.

Design Featured Comparator

Parameters	TLV184x	TLV183x
V_S	2.7V to 40V	2.7V to 40V
V_{inCM}	2.7V to 40V	2.7V to 40V
V_{OUT}	Open-Drain	Push-Pull
V_{OS}	500µV	500µV
I_Q	70µA/Ch	70µA/Ch
$t_{PD(HL)}$	65ns	65ns
#Channels	1, 2, 4	1, 2, 4
	TLV184x	TLV183x

Design Alternate Comparator

	TLV902x_3x	TLV323x
V_S	1.6V to 5.5V	2.7V to 5.5V
V_{inCM}	Rail-to-rail	Rail-to-rail
V_{OUT}	Open-Drain, Push-Pull	Push-Pull
V_{OS}	300µV	500µV
I_Q	16µA/Ch	200µA/Ch
$t_{PD(HL)}$	100ns	20ns
#Channels	1, 2, 4	1, 2
	TLV902x_3x	TLV3231

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