Analog Engineer's Circuit

Single-Supply, Low-Side, Unidirectional Current-Sensing Circuit

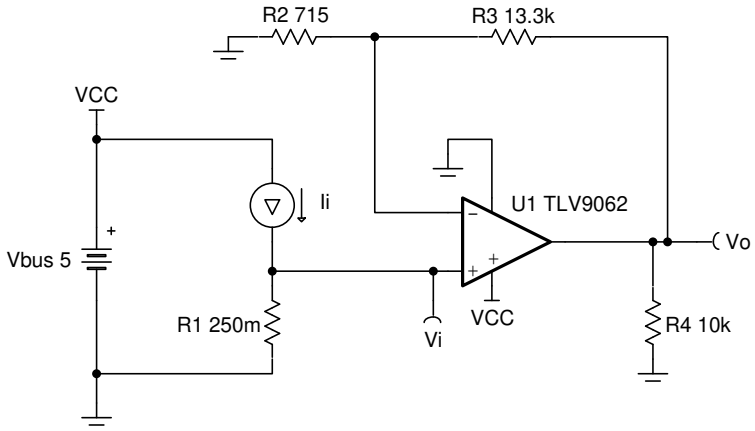
Pete Semig

Design Goals

Input		Output		Supply		Full–Scale Range Error
I_{iMax}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	FSR_{Error}
1A	250mV	50mV	4.9V	5V	0V	0.2%

Design Description

This single–supply, low–side, current sensing method accurately detects load current up to 1A and converts it to a voltage between 50mV and 4.9V. The input current range and output voltage range can be scaled as necessary and larger supplies can be used to accommodate larger swings.



Design Notes

1. Use the op amp linear output operating range, which is usually specified under the test conditions.
2. The common–mode voltage is equal to the input voltage.
3. Tolerance of the shunt resistor and feedback resistors determines the gain error of the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. If trying to detect zero current with output swing to GND, a negative charge pump (such as LM7705) can be used as the negative supply in this design to maintain linearity for output signals near 0V. See *Single-Supply, Low-Side, Unidirectional Current-Sensing Solution With Output Swing to GND Circuit* analog engineer's circuit for more information.
6. Using high–value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
7. The small–signal bandwidth of this circuit depends on the gain of the circuit and gain bandwidth product (GBP) of the amplifier.
8. Filtering can be accomplished by adding a capacitor in parallel with R_3 . Adding a capacitor in parallel with R_3 improves stability of the circuit if high–value resistors are used.
9. For more information on op amp linear operating region, stability, capacitive load drive, driving ADCs, and bandwidth please see the Design References section.

Design Steps

The transfer function for this circuit is given below.

$$V_o = I_i \times R_1 \times \left(1 + \frac{R_3}{R_2}\right)$$

1. Define the full–scale shunt voltage and calculate the maximum shunt resistance.

$$V_{iMax} = 250\ mV \quad at \quad I_{iMax} = 1\ A$$

$$R_1 = \frac{V_{iMax}}{I_{iMax}} = \frac{250\ mV}{1\ A} = 250\ m\ \Omega$$

2. Calculate the gain required for maximum linear output voltage.

$$V_{iMax} = 250\ mV \quad and \quad V_{oMax} = 4.9\ V$$

$$Gain = \frac{V_{oMax}}{V_{iMax}} = \frac{4.9\ V}{250\ mV} = 19.6\ \frac{V}{V}$$

3. Select standard values for R_2 and R_3.

   From Analog Engineer's calculator, use "Find Amplifier Gain" and get resistor values by inputting gain ratio of 19.6.

   R_2 = 715 Ω (0.1% Standard Value)

   R_3 = 13.3 kΩ (0.1% Standard Value)

4. Calculate minimum input current before hitting output swing–to–rail limit. I_{iMin} represents the minimum accurately detectable input current.

$$V_{oMin} = 50\ mV; \quad R_1 = 250\ m\ \Omega$$

$$V_{iMin} = \frac{V_{oMin}}{Gain} = \frac{50\ mV}{19.6\ \frac{V}{V}} = 2.55\ mV$$

$$I_{iMin} = \frac{V_{iMin}}{R_1} = \frac{2.55\ mV}{250\ m\ \Omega} = 10.2\ mA$$

5. Calculate Full scale range error and relative error. V_{os} is the typical offset voltage found in data sheet.

$$FSR_{error} = \left(\frac{V_{os}}{V_{iMax} - V_{iMin}}\right) \times 100 = \left(\frac{0.3\ mV}{247.45\ mV}\right) \times 100 = 0.121\ \%$$

$$Relative\ Error\ at\ I_{iMax} = \left(\frac{V_{os}}{V_{iMax}}\right) \times 100 = \left(\frac{0.3\ mV}{250\ mV}\right) \times 100 = 0.12\ \%$$

$$Relative\ Error\ at\ I_{iMin} = \left(\frac{V_{os}}{V_{iMin}}\right) \times 100 = \left(\frac{0.3\ mV}{2.5\ mV}\right) \times 100 = 12\ \%$$

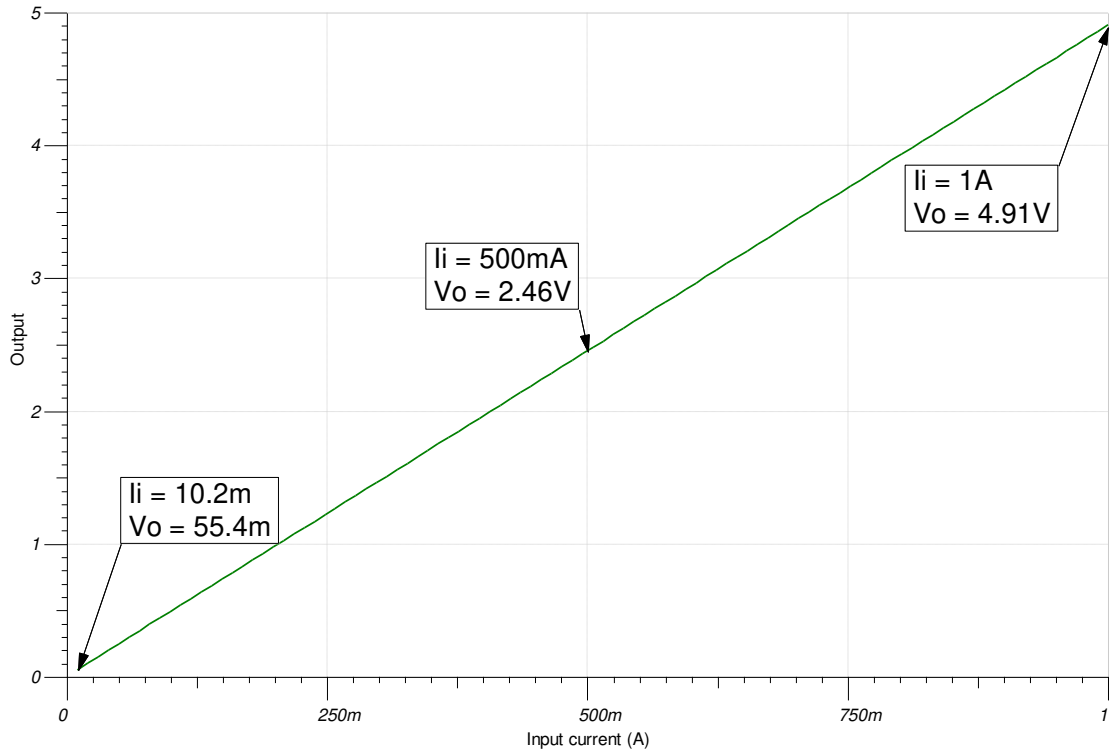
6. To maintain sufficient phase margin, verify that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit

$$\frac{1}{2 \times \pi \times (C_{cm} + C_{diff}) \times (R_2 || R_3)} > \frac{GBP}{G}$$

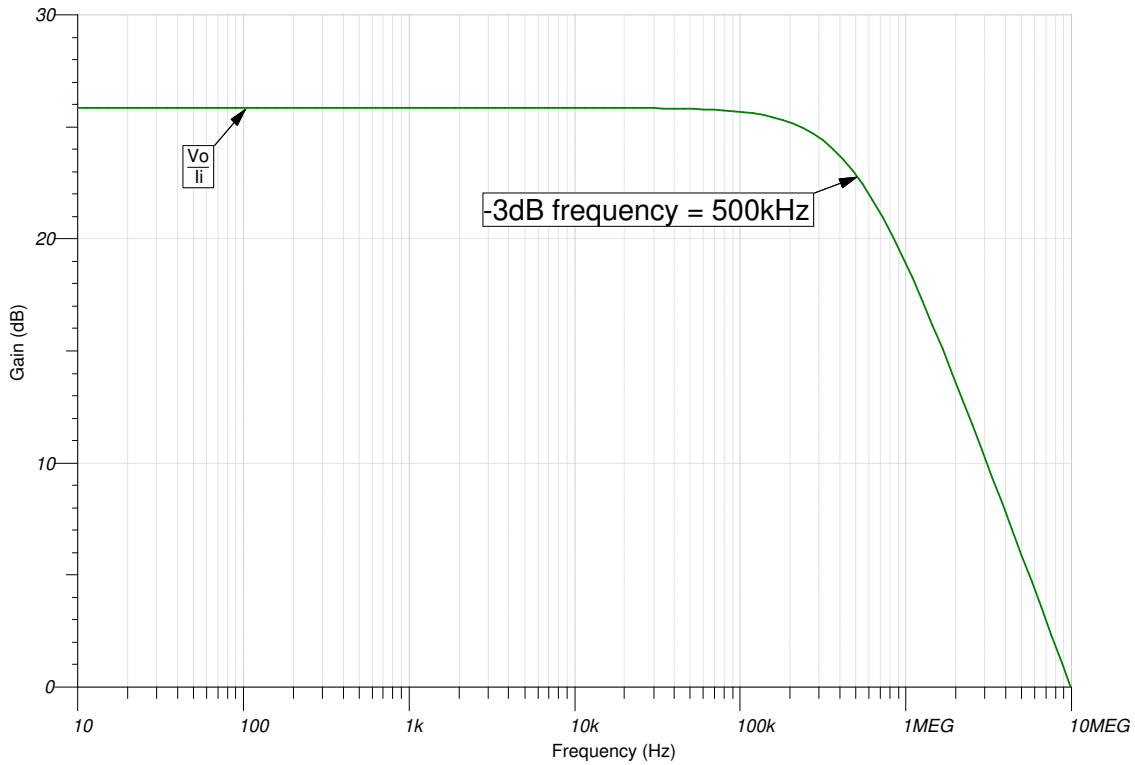
$$\frac{1}{2 \times \pi \times (3pF + 3pF) \times \left(\frac{715\ \Omega \times 13.3\ k\Omega}{715\ \Omega + 13.3\ k\Omega}\right)} > \frac{10\ MHz}{19.6\ \frac{V}{V}} = 39.1\ MHz > 510\ kHz$$

Design Simulations

DC Simulation Results



AC Simulation Results



References

Texas Instruments, *Simulation for Single-Supply Low-Side Unidirectional Current-Sense Circuit*, SBOC523 SPICE simulation file

Texas Instruments, *0-1A, Single-Supply, Low-Side, Current Sensing Solution*, TIPD129 reference design

Texas Instruments, *Current sensing reference design for 10µA to 10mA, low side, single supply*, TIPD104 reference design

Texas Instruments, *Single-Supply, Low-Side, Unidirectional Current-Sensing Solution With Output Swing to GND Circuit*, analog engineer's circuit

Design Featured Op Amp

TLV9061	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	0.3mV
I_q	538µA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1,2,4
TLV9061	

Design Alternate Op Amp

OPA375	
V_{cc}	2.25V to 5.5V
V_{inCM}	(V–) to ((V+)–1.2V)
V_{out}	Rail–to–rail
V_{os}	0.15mV
I_q	890µA
I_b	10pA
UGBW	10MHz
SR	4.75V/µs
#Channels	1
OPA375	

For battery operated or power conscious designs, outside of the original design goals described earlier, where lowering total system power is desired.

LPV821	
V_{cc}	1.7V to 3.6V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	1.5µV
I_q	650nA/Ch
I_b	7pA
UGBW	8kHz
SR	3.3V/ms
#Channels	1
LPV821	

Trademarks

All trademarks are the property of their respective owners.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265