Analog Engineer's Circuit Amplifiers

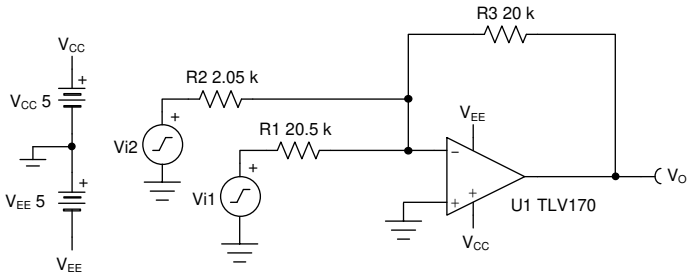
Inverting Summer Circuit

Design Goals

Input 1		Input 2		Output		Freq.	Supply	
V_{i1Min}	V_{i1Max}	V_{i2Min}	V_{i2Max}	V_{oMin}	V_{oMax}	f	V_{cc}	V_{ee}
–2.5V	2.5V	–250mV	250mV	–4.9V	4.9V	10kHz	5V	–5V

Design Description

This design sums (adds) and inverts two input signals, V_{i1} and V_{i2}. The input signals typically come from low-impedance sources because the input impedance of this circuit is determined by the input resistors, R_1 and R_2. The common-mode voltage of an inverting amplifier is equal to the voltage connected to the non-inverting node, which is ground in this design.



Design Notes

1. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions. The common-mode voltage in this circuit does not vary with input voltage.
2. The input impedance is determined by the input resistors. Make sure these values are large when compared to the output impedance of the source.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitor in parallel to R_3. Adding a capacitor in parallel with R_3 will also improve stability of the circuit if high-value resistors are used.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the *Design References* section.

Design Steps

The transfer function for this circuit is given below.

$$V_o = V_{i1} \times \left(-\frac{R_3}{R_1}\right) + V_{i2} \times \left(-\frac{R_3}{R_2}\right)$$

1. Select a reasonable resistance value for R_3.

   $R_3 = 20\ k\Omega$

2. Calculate gain required for V_{i1}. For this design, half of the output swing is devoted to each input.

   $$|G_{Vi1}| = \left|\frac{\frac{V_{oMax} - V_{oMin}}{2}}{V_{i1Max} - V_{i1Min}}\right| = \left|\frac{\frac{4.9\ V - (-4.9\ V)}{2}}{2.5\ V - (-2.5\ V)}\right| = 0.98\frac{V}{V} = -0.175\ dB$$

3. Calculate the value of R_1.

   $$|G_{Vi1}| = \frac{R_3}{R_1} \rightarrow R_1 = \frac{R_3}{|G_{Vi1}|} = \frac{20\ k\Omega}{0.98\ \frac{V}{V}} = 20.4\ k\Omega \approx 20.5\ k\Omega\ (Standard Value)$$

4. Calculate gain required for V_{i2}. For this design, half of the output swing is devoted to each input.

   $$|G_{Vi2}| = \left|\frac{\frac{V_{oMax} - V_{oMin}}{2}}{V_{i2Max} - V_{i2Min}}\right| = \left|\frac{\frac{4.9\ V - (-4.9\ V)}{2}}{250\ mV - (-250\ mV)}\right| = 9.8\ \frac{V}{V} = 19.82\ dB$$

5. Calculate the value of R_2.

   $$|G_{Vi2}| = \frac{R_3}{R_2} \rightarrow R_2 = \frac{R_3}{|G_{Vi2}|} = \frac{20\ k\Omega}{9.8\ \frac{V}{V}} = 2.04\ k\Omega \approx 2.05\ k\Omega\ (Standard Value)$$

6. Calculate the small signal circuit bandwidth to ensure it meets the 10-kHz requirement. Be sure to use the noise gain (NG), or non-inverting gain, of the circuit. When calculating the noise gain note that R_1 and R_2 are in parallel.

   $GBP_{OPA170} = 1.2\ MHz$

   $$NG = 1 + \frac{R_3}{R_1||R_2} = 1 + \frac{20\ k\Omega}{1.86\ k\Omega} = 11.75\frac{V}{V} = 21.4\ dB \tag{8}$$

   $$BW = \frac{GBP}{NG} = \frac{1.2\ MHz}{11.75\ \frac{V}{V}} = 102\ kHz \tag{9}$$

   - This requirement is met because the closed-loop bandwidth is 102kHz and the design goal is 10kHz.

7. Calculate the minimum slew rate to minimize slew-induced distortion.

   $$V_p = \frac{SR}{2 \times \pi \times f} \rightarrow SR > 2 \times \pi \times f \times V_p$$

   $$SR > 2 \times \pi \times 10\ kHz \times 4.9\ V = 307.87\ \frac{kV}{s} = 0.31\ \frac{V}{\mu s} \tag{11}$$

   - SR_{OPA170}=0.4V/µs, therefore it meets this requirement.

8. To avoid stability issues ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

   $$\frac{1}{2 \times \pi \times (C_{cm} + C_{diff}) \times (R_1||R_2||R_3)} > \frac{GBP}{NG}$$

   $$\frac{1}{2 \times \pi \times 3\ pF \times 3\ pF \times 1.7\ k\Omega} > \frac{1.2\ MHz}{11.75\ \frac{V}{V}} \tag{13}$$

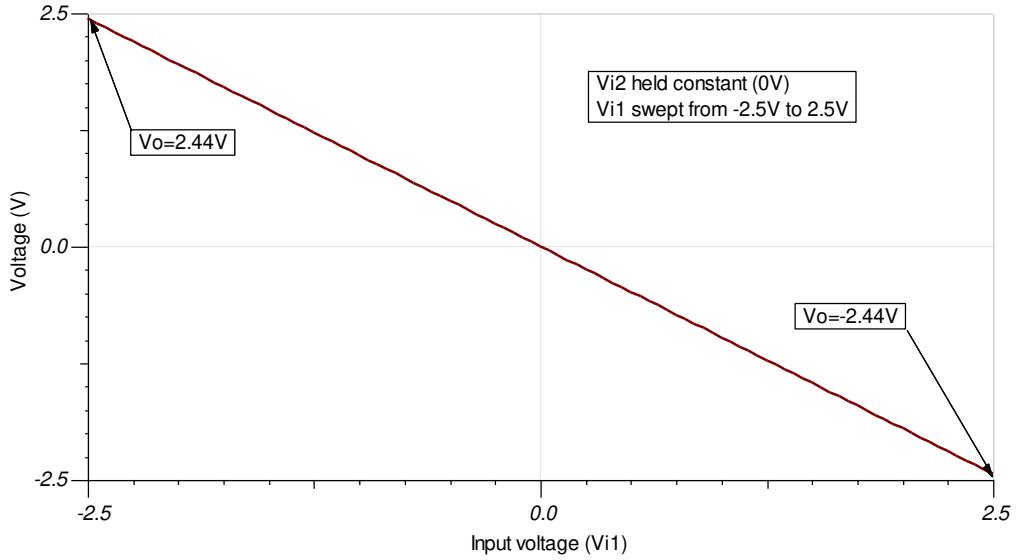
   $$15.6\ MHz > 102\ kHz \tag{14}$$

   - C_{cm} and C_{diff} are the common-mode and differential input capacitances.
   - Since the zero frequency is greater than the bandwidth of the circuit, this requirement is met.

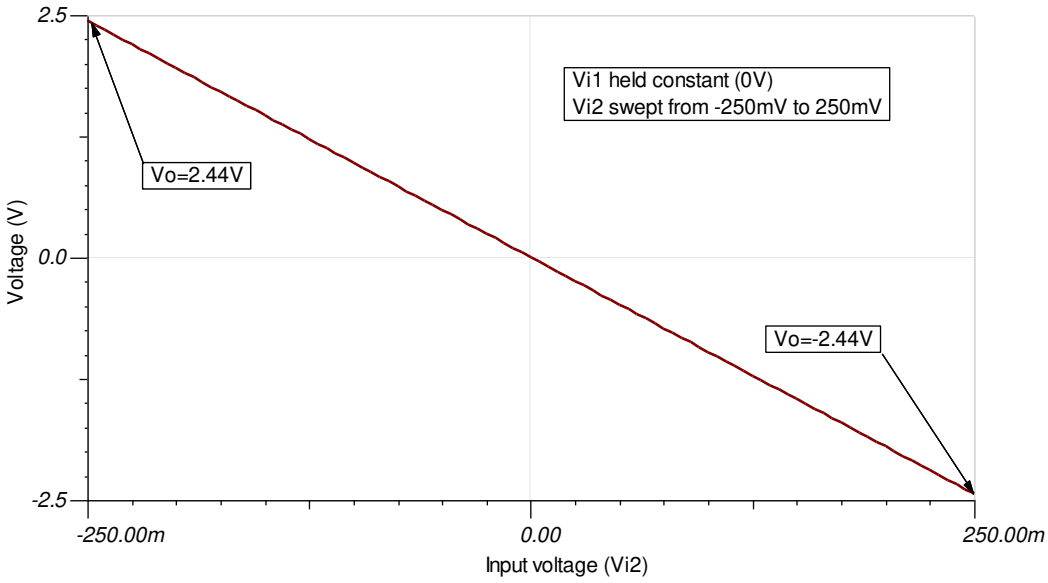
Design Simulations

DC Simulation Results

This simulation sweeps V_{i1} from –2.5V to 2.5V while V_{i2} is held constant at 0V. The output is inverted and ranges from –2.44V to 2.44V.

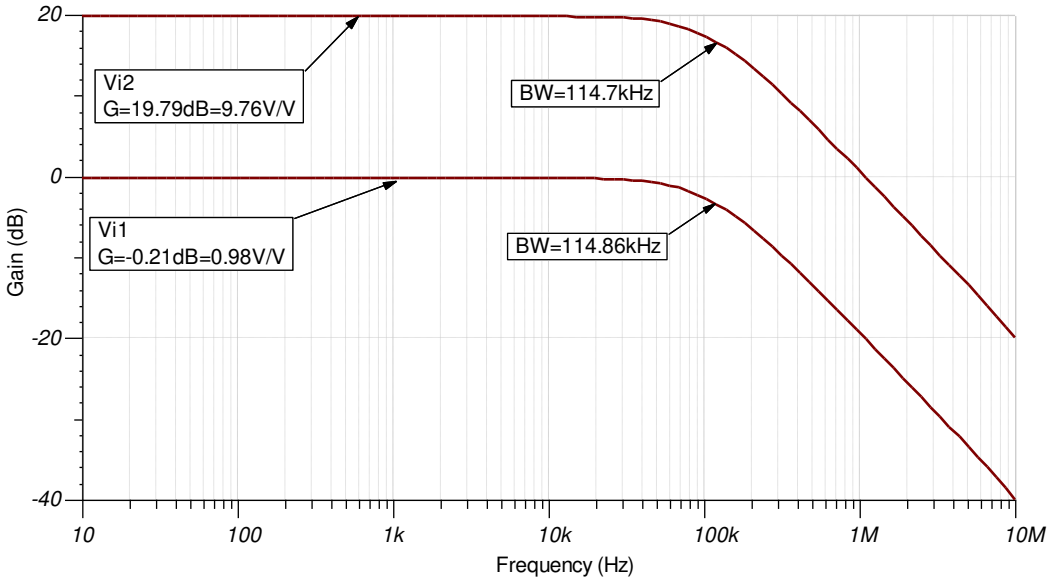


This simulation sweeps V_{i2} from –250mV to 250mV while V_{i1} is held constant at 0V. The output is inverted and ranges from –2.44V to 2.44V.



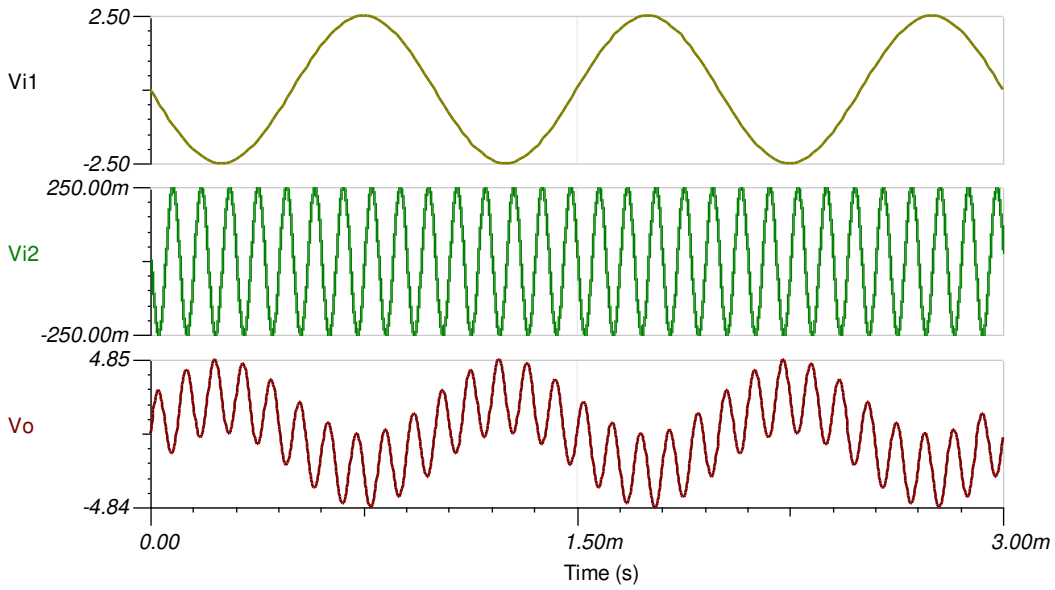
AC Simulation Results

This simulation shows the bandwidth of the circuit. Note that the bandwidth is the same for either input. This is because the bandwidth depends on the noise gain of the circuit, not the signal gain of each input. These results correlate well with the calculations.



Transient Simulation Results

This simulation shows the inversion and summing of the two input signals. V_{i1} is a 1-kHz, 5-V_{pp} sine wave and V_{i2} is a 10-kHz, 500-mV_{pp} sine wave. Since both inputs are properly amplified or attenuated, the output is within specification.



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC494.

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC please visit TI Precision Labs.

Design Featured Op Amp

OPA170	
V_{ss}	2.7V to 36V
V_{inCM}	(Vee-0.1V) to (Vcc-2V)
V_{out}	Rail-to-rail
V_{os}	0.25mV
I_q	110µA
I_b	8pA
UGBW	1.2MHz
SR	0.4V/µs
#Channels	1, 2, 4
www.ti.com/product/opa170	

Design Alternate Op Amp

LMC7101	
V_{ss}	2.7V to 15.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	110µV
I_q	0.8mA
I_b	1pA
UGBW	1.1MHz
SR	1.1V/µs
#Channels	1
www.ti.com/product/lmc7101	

Revision History

Revision	Date	Change
C	January 2021	Updated Formula format
B	December 2020	Updated Design Goals Table
A	January 2019	Down-style title. Updated title role to *Amplifiers*. Added link to circuit cookbook landing page.

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