Analog Engineer's Circuit

Single-Supply Diff-In to Diff-Out AC Amplifier Circuit

Caelan (Zak) Kaye

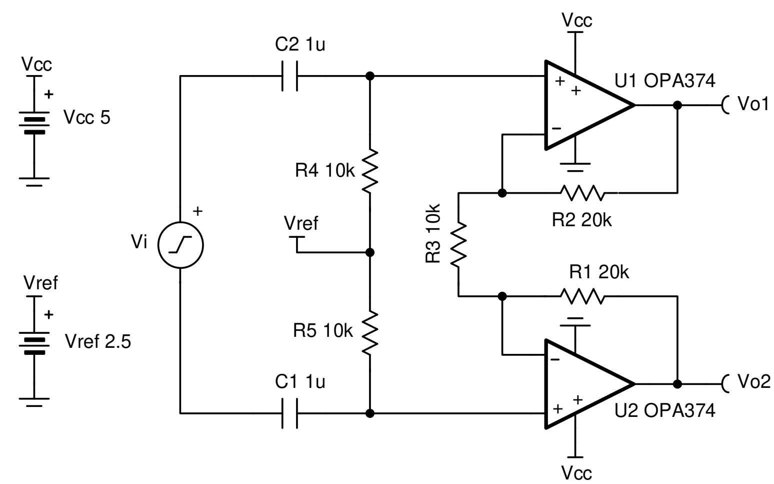
Design Goals

Diff. Input V_i		Diff. Output ($V_{o1} - V_{o2}$)		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
–500mV	+500mV	–2.5V	+2.5V	+5	0V	+2.5V

Lower Cutoff Freq.	Upper Cutoff Freq.
16Hz	> 1MHz

Design Description

This circuit uses two op amps to build a discrete, single-supply diff-in diff-out amplifier. The circuit converts a differential signal to a differential output signal.



Design Notes

1. Verify that R_1 and R_2 are well matched with high accuracy resistors to maintain high DC common-mode rejection performance.
2. Increase R_4 and R_5 to match the necessary input impedance at the expense of thermal noise performance.
3. Bias for single-supply operation can also be created by a voltage divider from V_{cc} to ground.
4. V_{ref} sets the output voltage of the instrumentation amplifier bias at mid-supply to allow the output to swing to both supply rails.
5. Choose C_1 and C_2 to select the lower cutoff frequency.
6. Linear operation is contingent upon the input common-mode and the output swing ranges of the discrete op amps used. The linear output swing ranges are specified under the Aol test conditions in the op amps data sheets

Design Steps

1. The transfer function of the circuit is shown below.

$$V_{oDiff} = V_i \times G + V_{ref}$$
$$\text{where } V_i = \text{the differential input voltage}$$
$$V_{ref} = \text{the reference voltage provided to the amplifier}$$
$$G = 1 + 2 \times \left(\frac{R_1}{R_3}\right)$$

2. Choose resistors R_1 = R_2 to maintain common-mode rejection performance.

$$\text{Choose } R_1 = R_2 = 20\ k\Omega \ \ (\text{Standard value})$$

3. Choose resistors R_4 and R_5 to meet the desired input impedance.

$$\text{Choose } R_4 = R_5 = 10\ k\Omega \ \ (\text{Standard value})$$

4. Calculate R_3 to set the differential gain.

$$\text{Gain} = 1 + \left(\frac{2 \times R_1}{R_3}\right) = 5\ \frac{V}{V}$$
$$R_1 = R_2 = 20\ k\ \Omega$$
$$G = 1 + \frac{2 \times 20\ k\Omega}{R_3} = 5\ \frac{V}{V} \rightarrow 5\ \frac{V}{V} - 1 = \frac{40\ k\Omega}{R_3} = 4 \rightarrow R_3 = \frac{40\ k\Omega}{4} = 10\ k\Omega \ \left(\text{Standard value}\right)$$

5. Set the reference voltage V_{ref} at mid-supply.

$$V_{ref} = \frac{V_{cc}}{2} = \frac{5\ V}{2} \rightarrow V_{ref} = 2.5V$$

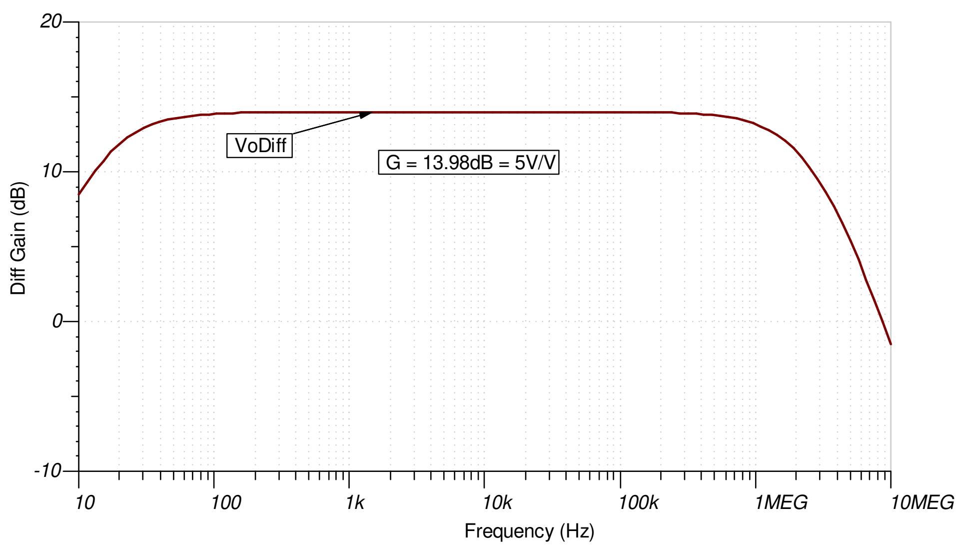
6. Calculate C_1 and C_2 to set the lower cutoff frequency.

$$f_c = \frac{1}{2 \times \pi \times R_4 \times C_1} = 16\ Hz$$
$$R_4 = R_5 = 10\ k\Omega$$
$$f_c = \frac{1}{2 \times \pi \times 10\ k\Omega \times C_1} = 16\ Hz \rightarrow C_1 = \frac{1}{2 \times \pi \times 10\ k\Omega \times 16\ Hz} = 0.99\mu F \rightarrow C_1 = C_2 = 1\mu F \ \left(\text{Standard value}\right)$$

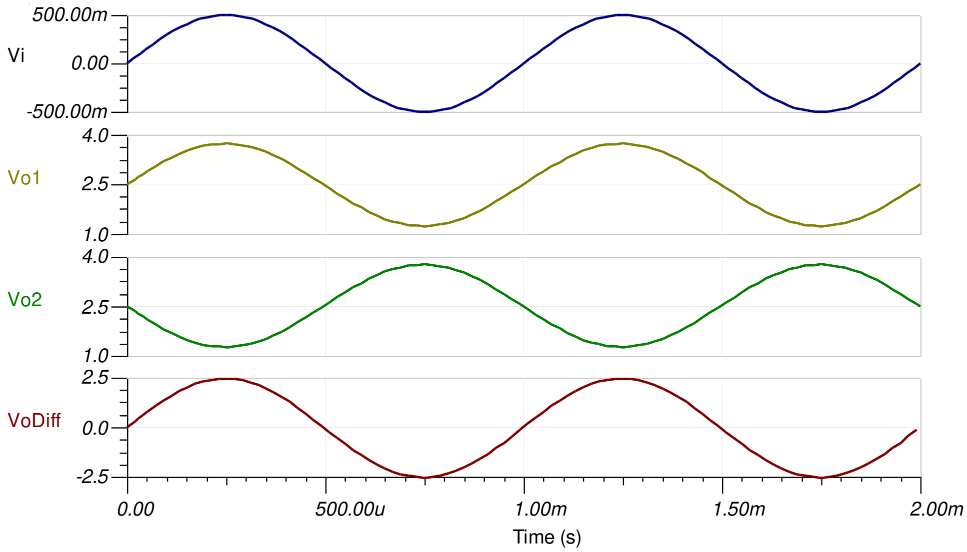
Design Simulations

AC Simulation Results

In the following figure, notice the lower –3-dB cutoff frequency is approximately 16Hz and the upper cutoff frequency is > 1MHz as required for this design.



Transient Simulation Results



References

Texas Instruments, SBOMAU5 SPICE Simulation, file download

Design Featured Op Amp

OPA374	
V_{ss}	2.3V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1mV
I_q	585µA/Ch
I_b	0.5pA
UGBW	6.5MHz
SR	5V/µs
#Channels	1,2,4
OPA374	

Design Alternate Op Amp

TLV9061	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3mV
I_q	0.538mA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1,2,4
TLV9061	

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