

# Analog Engineer's Circuit

## Photodiode Amplifier Circuit



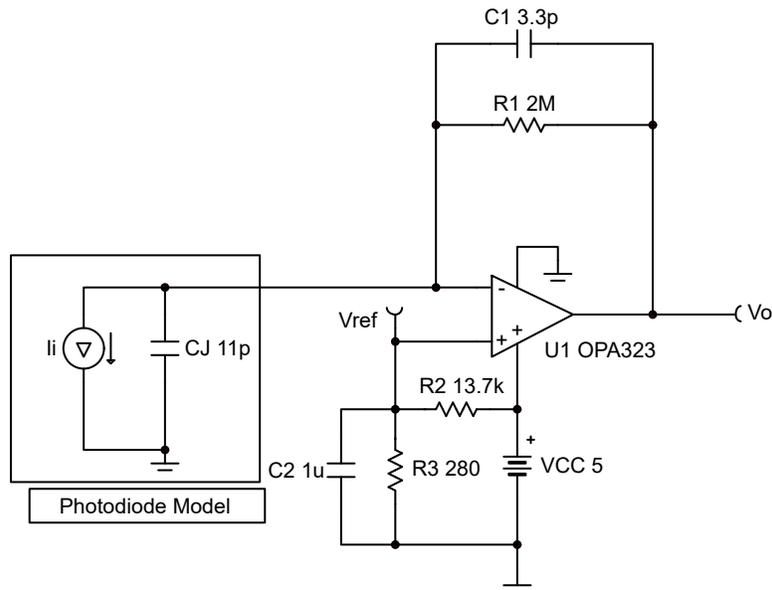
Amplifiers

### Design Goals

Input		Output		BW	Supply		
$I_{iMin}$	$I_{iMax}$	$V_{oMin}$	$V_{oMax}$	$f_p$	$V_{cc}$	$V_{ee}$	$V_{ref}$
0A	2.4 $\mu$ A	100mV	4.9V	20kHz	5V	0V	0.1V

### Design Description

This circuit consists of an op amp configured as a transimpedance amplifier for amplifying the light-dependent current of a photodiode.



### Design Notes

1. A bias voltage ( $V_{ref}$ ) prevents the output from saturating at the negative power supply rail when the input current is 0A.
2. Use a JFET or CMOS input op amp with low bias current to reduce DC errors.
3. Set output range based on linear output swing (see  $A_{ol}$  specification).

## Design Steps

1. Select the gain resistor.

$$R_1 = \frac{V_{oMax} - V_{oMin}}{I_{iMax}} = \frac{4.9V - 0.1V}{2.4\mu A} = 2M\Omega$$

2. Select the feedback capacitor to meet the circuit bandwidth.

$$C_1 \leq \frac{1}{2 \times \pi \times R_1 \times f_p}$$

$$C_1 \leq \frac{1}{2 \times \pi \times 2M\Omega \times 20kHz} \leq 3.97pF \approx 3.3pF \text{ (Standard Value)}$$

3. Calculate the necessary op amp gain bandwidth (GBW) for the circuit to be stable.

$$GBW > \frac{C_i + C_1}{2 \times \pi \times R_1 \times C_1^2} > \frac{13pF + 3.3pF}{2 \times \pi \times 2M\Omega \times (3.3pF)^2} = 119kHz$$

where  $C_i = C_j + C_d + C_{cm} = 11pF + 2pF + 1pF = 13pF$  given

- $C_j$ : Junction capacitance of photodiode
- $C_d$ : Differential input capacitance of the amplifier
- $C_{cm}$ : Common-mode input capacitance of the inverting input

4. Calculate the bias network for a 0.1V bias voltage.

$$R_2 = \frac{V_{cc} - V_{ref}}{V_{ref}} \times R_3$$

$$R_2 = \frac{5V - 0.1V}{0.1V} \times R_3$$

$$R_2 = 49 \times R_3$$

Closest 1% resistor values that yield this relationship are

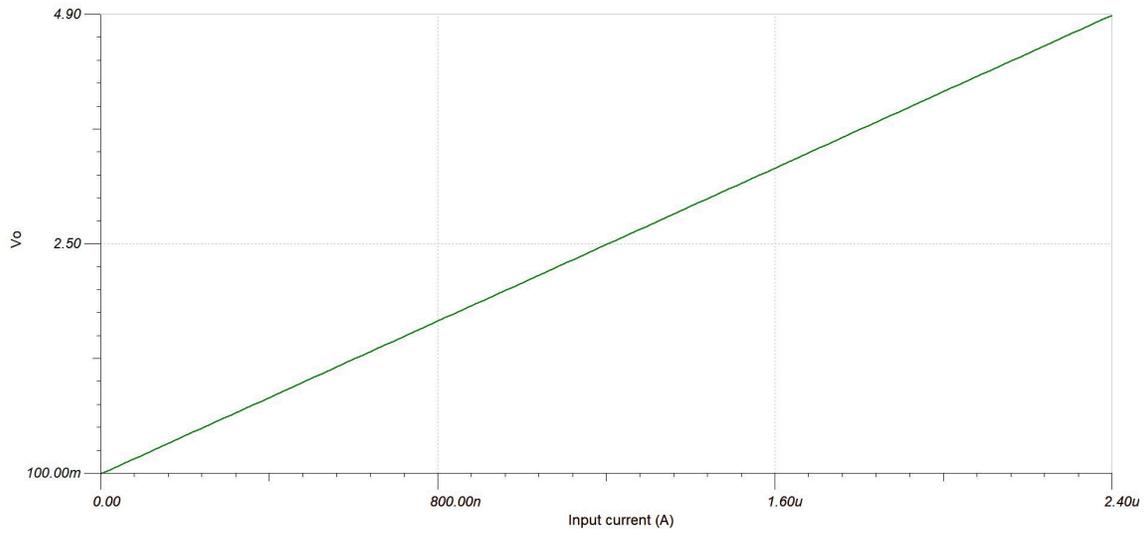
$$R_2 = 13.7k\Omega \text{ and } R_3 = 280\Omega$$

5. Select  $C_2$  to be  $1\mu F$  to filter the  $V_{ref}$  voltage. The resulting cutoff frequency is:

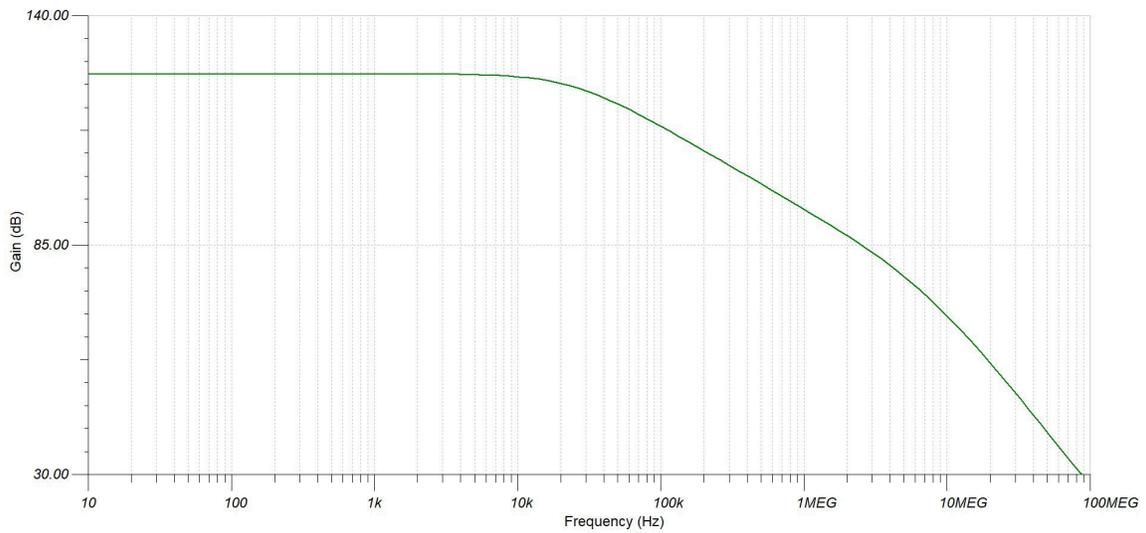
$$f_p = \frac{1}{2 \times \pi \times C_2 \times (R_2 \parallel R_3)} = \frac{1}{2 \times \pi \times 1 \mu F \times (13.7k \parallel 280)} = 580Hz$$

## Design Simulations

### DC Simulation Results



### AC Simulation Results



## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the circuit SPICE simulation file:

- For TINA-TI: [SBOMCH8](#)
- For PSpice for TI: [SBOMCH0](#)

See [TIPD176](#).

## Design Featured Op Amp

OPA323	
$V_{cc}$	1.7V to 5.5V
$V_{inCM}$	Rail-to-rail
$V_{out}$	Rail-to-rail
$V_{os}$	0.15mV
$I_q$	1.6mA/Ch
$I_b$	0.5pA
UGBW	20MHz
SR	33V/ $\mu$ s
#Channels	1, 2, and 4
Link	<a href="#">OPA323</a>

## Design Alternate Op Amp

	OPA328	OPA392	OPA322
$V_{cc}$	2.2V to 5.5V	1.7V to 5.5V	1.8V to 5.5V
$V_{inCM}$	Rail-to-rail	Rail-to-rail	Rail-to-rail
$V_{out}$	Rail-to-rail	Rail-to-rail	Rail-to-rail
$V_{os}$	3 $\mu$ V	1 $\mu$ V	0.5mV
$I_q$	3.8mA/Ch	1.22mA/Ch	1.6mA/Ch
$I_b$	0.2pA	10fA	0.2pA
UGBW	40MHz	13MHz	20MHz
SR	30V/ $\mu$ s	4.5V/ $\mu$ s	10V/ $\mu$ s
#Channels	1 and 2	1, 2, and 4	1, 2, and 4
Link	<a href="#">OPA328</a>	<a href="#">OPA392</a>	<a href="#">OPA322</a>

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