Analog Engineer's Circuit

Slew Rate Limiter Circuit

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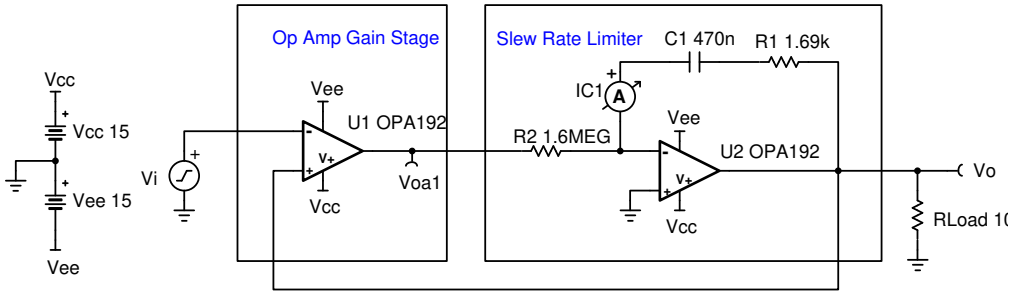
Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
–10V	10V	–10V	10V	15V	–15V	0V

Design Description

This circuit controls the slew rate of an analog gain stage. This circuit is intended for symmetrical slew rate applications. The desired slew rate must be slower than that of the op amp chosen to implement the slew rate limiter.



Design Notes

1. The gain stage op-amp and slew rate limiting op amp should both be checked for stability.
2. Verify that the current demands for charging or discharging C_1 plus any load current out of U_2 will not limit the voltage swing of U_2.

Design Steps

1. Set slew rate and choose a standard value for the feedback capacitor, C_1.

$$C_1 = 470\text{nF}$$

$$\text{SR} = 20\frac{\text{V}}{\text{s}}$$

2. Choose the value of R_2 to set the capacitor current necessary for the desired slew rate.

$$\text{SR} = \frac{I_{C_1}}{C_1}$$

$$20\frac{\text{V}}{\text{s}} = \frac{I_{C_1}}{470\text{nF}} \text{ where } I_{C_1} = 9.4\ \mu\text{A}$$

$$\text{Gain stage op amp } V_{sat} = \pm 14.995 \text{ (typical)}$$

$$I_{C_1} = \frac{V_{sat}}{R_2}$$

$$9.4\ \mu A = \frac{14.995V}{R_2}, \text{so } R_2 = 1.595\ M\Omega \approx 1.6M\Omega \text{ (Standard Value)}$$

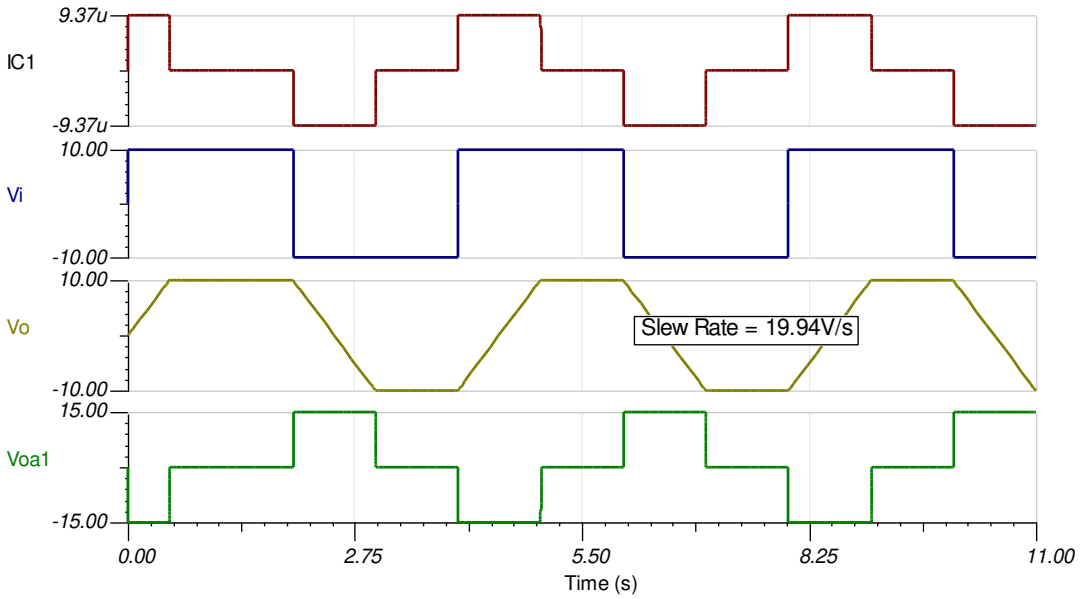
3. Compensate feedback network for stability. R_1 adds a pole to the 1/β network. This pole should be placed so that the 1/β curve levels off a decade before it intersects the open loop gain curve (200 Hz, for this example).

$$f_p = \frac{1}{2\pi \times R_1 \times C_1} = 200Hz$$

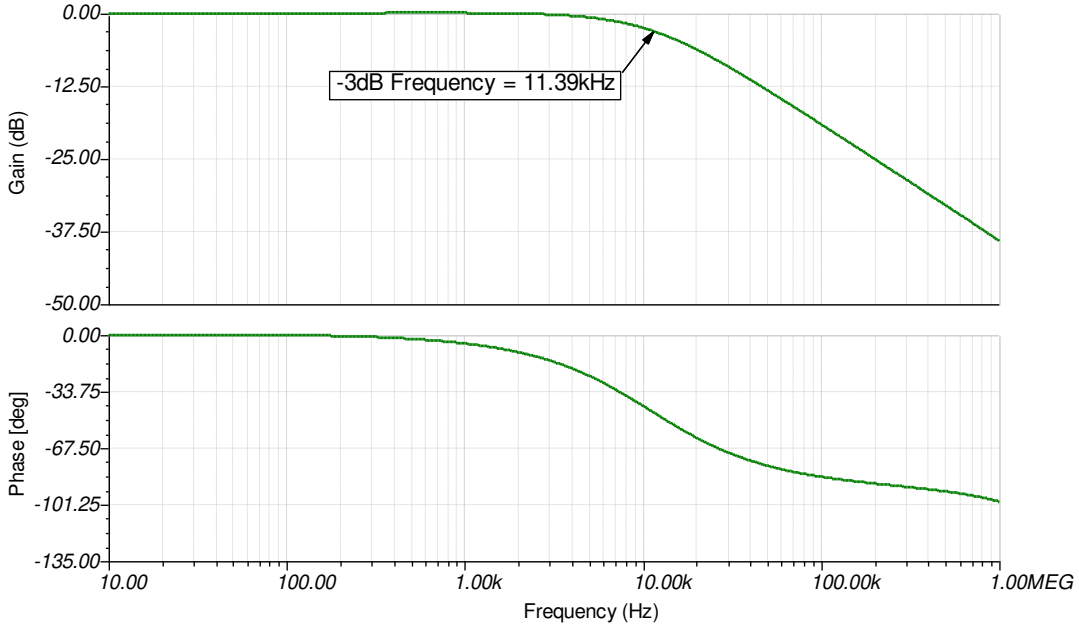
$$200Hz = \frac{1}{2\pi \times R_1 \times 470nF}, \text{so } R_1 = 1.693\ k\Omega \approx 1.69k\Omega \text{ (Standard Value)}$$

Design Simulations

Transient Simulation Results



AC Simulation Results



Design References

Texas Instruments, *Simulation for Slew Rate Limiter*, circuit SPICE simulation file

Texas Instruments, *Single Op-Amp Slew Rate Limiter*, reference design

Design Featured Op Amp

OPA192	
V_{cc}	4.5V to 36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5µV
I_q	1mA/Ch
I_b	5pA
UGBW	10MHz
SR	20V/µs
#Channels	1, 2, and 4
OPA192	

Design Alternate Op Amp

TLV2372	
V_{cc}	2.7V to 16V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	2mV
I_q	750µA/Ch
I_b	1pA
UGBW	3MHz
SR	2.1V/µs
#Channels	1, 2, and 4
TLV2372	

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A* (February 2019) to Revision B (October 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (February 2018) to Revision A (February 2019)	Page
• Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file	1

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