*Analog Engineer's Circuit*

# *Single-Ended Input to Differential Output Circuit*

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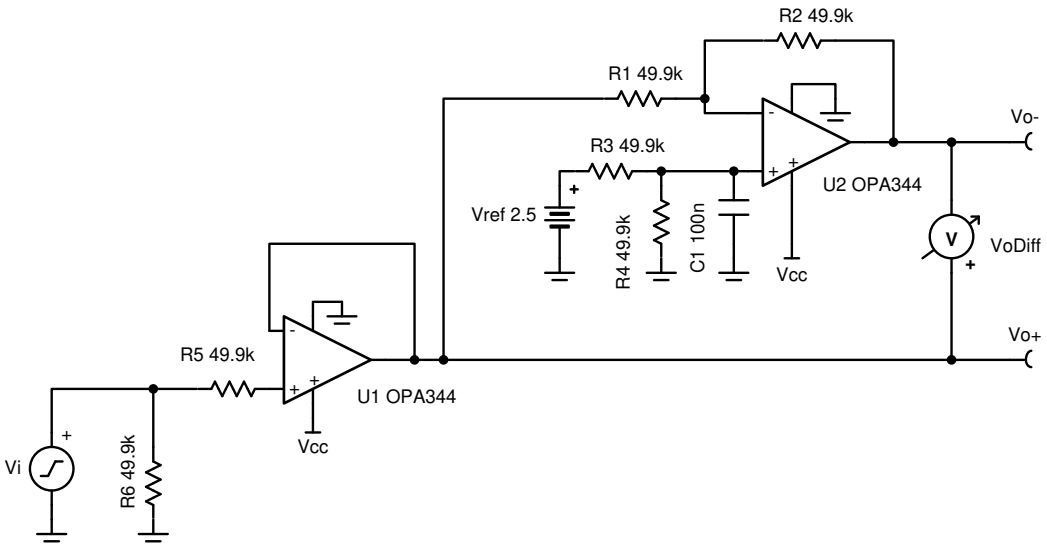
## Design Goals

| Input | | Output | | Supply | | |
|---|---|---|---|---|---|---|
| $V_{iMin}$ | $V_{iMax}$ | $V_{oDiffMin}$ | $V_{oDiffMax}$ | $V_{cc}$ | $V_{ee}$ | $V_{ref}$ |
| 0.1V | 2.4V | –2.3V | 2.3V | 2.7V | 0V | 2.5V |

## Design Description

This circuit converts a single ended input of 0.1V to 2.4V into a differential output of ±2.3V on a single 2.7V supply. The input and output ranges can be scaled as necessary as long as the op amp input common-mode range and output swing limits are met.




## Design Notes

1. Op amps with rail-to-rail input and output maximizes the input and output range of the circuit.
2. Op amps with low $V_{os}$ and offset drift reduces DC errors.
3. Use low tolerance resistors to minimize gain error.
4. Set output range based on linear output swing (see $A_{ol}$ specification).
5. Keep feedback resistors low or add capacitor in parallel with $R_2$ for stability.

## Design Steps

1. Buffer $V_i$ signal to generate $V_{o+}$.

$$V_{O+} = V_i$$

2. Invert and level shift $V_{o+}$ using a difference amplifier to create $V_{o–}$.

$$V_{o-} = (V_{ref} - V_{o+}) \times \left(\frac{R_2}{R_1}\right)$$

3. Select resistances so that the resistor noise is smaller than the amplifier broadband noise.

$$E_{nv} = 30\frac{nV}{\sqrt{Hz}} \text{ (Voltage noise from op amp)}$$

$$\text{If } R_1 = R_2 = R_3 = R_4 = 49.9k\Omega \text{ then}$$

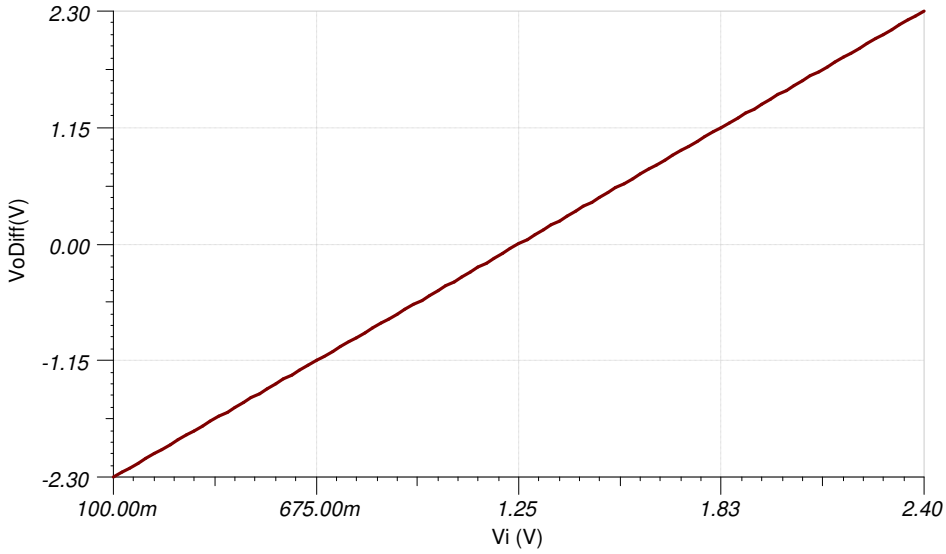
$$E_{nr} = \sqrt{\left(\sqrt{4 \times kB \times T \times [R_1 \,||\, R_2]}\right)^2 + \left(\sqrt{4 \times kB \times T \times [R_3 \,||\, R_4]}\right)^2} = 28.7\frac{nV}{\sqrt{Hz}} \; (<E_{nv})$$

4. Select resistances that protect the input of the amplifier and prevents floating inputs. To simplify the bill of materials (BOM), select $R_5 = R_6$.

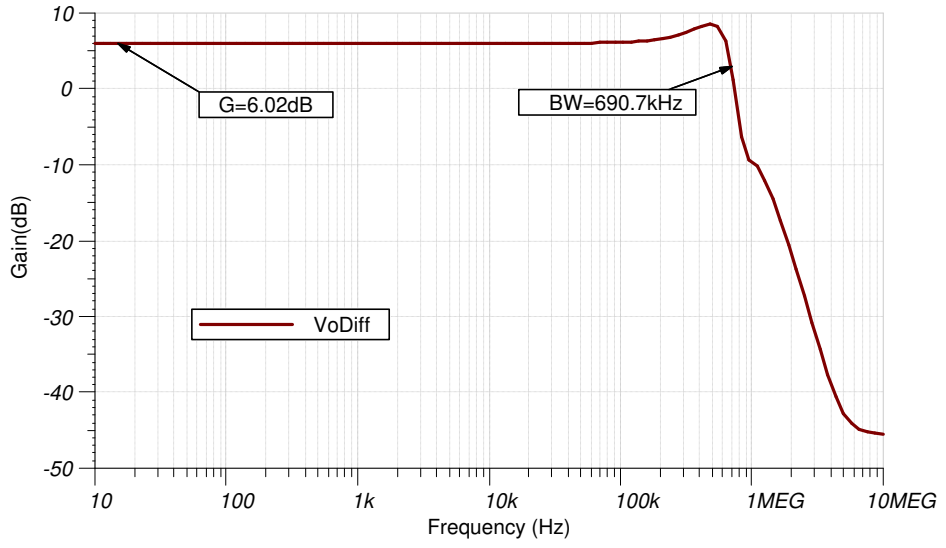
$$R_5 = R_6 = 49.9k\Omega$$

## Design Simulations

### DC Simulation Results




### AC Simulation Results



### Design References

Texas Instruments, *Simulation for Single-Ended Input to Differential Output*, circuit SPICE simulation file

Texas Instruments, *Single-Ended Input to Differential Output Conversion Circuit*, reference design

### Design Featured Op Amp

| OPA344 | |
|---|---|
| $V_{ss}$ | 1.8V to 5.5V |
| $V_{inCM}$ | Rail-to-rail |
| $V_{out}$ | Rail-to-rail |
| $V_{os}$ | 0.2mV |
| $I_q$ | 150µA |
| $I_b$ | 0.2pA |
| UGBW | 1MHz |
| SR | 0.8V/µs |
| #Channels | 1, 2, and 4 |
| OPA344 | |

### Design Alternate Op Amp

| OPA335 | |
|---|---|
| $V_{ss}$ | 2.7V to 5.5V |
| $V_{inCM}$ | $V_{ee}$–0.1V to$V_{cc}$–1.5V |
| $V_{out}$ | Rail-to-rail |
| $V_{os}$ | 1 µV |
| $I_q$ | 285µA/Ch |
| $I_b$ | 70pA |
| UGBW | 2MHz |
| SR | 1.6V/µs |
| #Channels | 1 and 2 |
| OPA335 | |

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## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (February 2019) to Revision B (October 2024)** **Page**

- Updated the format for tables, figures, and cross-references throughout the document..... 1

**Changes from Revision * (February 2018) to Revision A (February 2019)** **Page**

- Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file..... 1

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