Application Report
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Interfacing High-Speed LVDS Outputs of the ADS527x/ADS524x

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ABSTRACT

The ADS527x/ADS524x families of devices are high-performance octal/quad channel analog-to-digital converters (ADCs), ideal for the highest system density. Serial low voltage differential signaling (LVDS) outputs reduce the number of I/O interfaces required, power and overall package size. These device families are rated to work from sampling rates of 20–70MSPS. This corresponds to data rates of 240–840Mbps. This application report illustrates the design of a simple deserializer that can be used for capture rates up to 360Mbps. We then discuss the design of a receiver that can reliably deserialize LVDS outputs all the way up to 840Mbps. This high-speed deserializer has been implemented on the Altera EP2A15, part of the APEX™II family of FPGAs.

1 ADS527x/ADS524x System Overview

Table 1 lists the devices available for each speed node.

Table 1. ADS527x/ADS524x Part Numbers with Speed Nodes

SPEED NODE	OCTAL VERSIONS	QUAD VERSIONS
40MSPS	ADS5270	ADS5240
50MSPS	ADS5271	–
65MSPS	ADS5272	ADS5242
65MSPS	ADS5277	–
70MSPS	ADS5273	–

The ADS527x/ADS524x family integrates a phase lock loop (PLL) that multiplies the incoming conversion clock by a factor of 12. The PLL output is used to generate clocks with multiplication factor of 6x and 1x. Data is output in DDR format where both edges of the 6x clock (LCLK) are used for capturing 12 bits of data. The 1x clock (ADCLK) is aligned to one data frame and can be used as a frame synchronizer during deserialization. Figure 1 illustrates the timing of the data channel with respect to LCLK (6x-CLK) and ADCLK (1x-CLK).

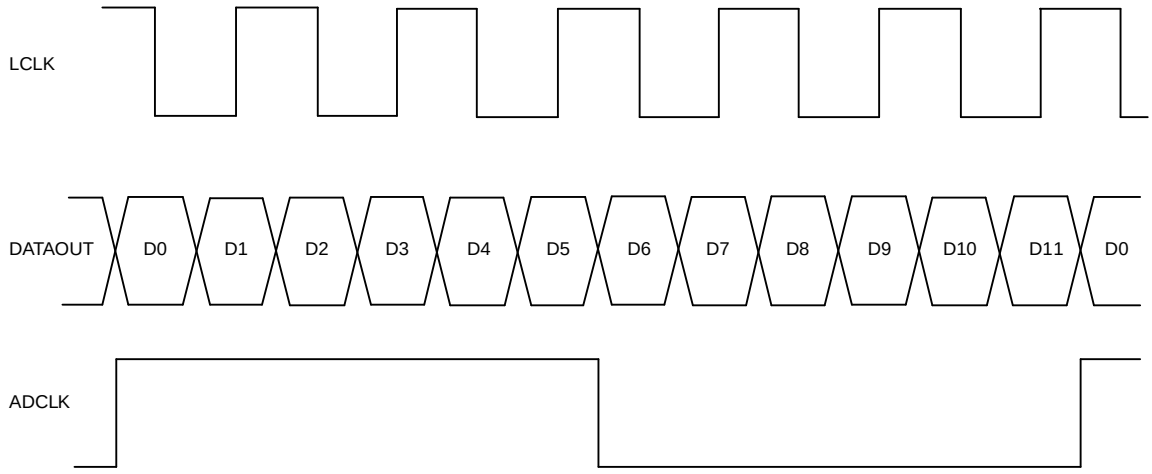

Figure 1. Timing and Alignment of ADS527x Data with LCLK and ADCLK

The ADS527x/ADS524x families of devices are specified for operation at speeds over 20MSPS. The PLL bandwidth restricts the sampling frequency from going below this threshold. The theoretical setup and hold times of these families are less than half the clock width of the 12x clock. The effects of finite rise-and-fall times and PLL jitter further reduce the time margin in which the data can be captured. Table 2 illustrates the typical setup and hold times for different sampling speeds.

Table 2. Typical Timing Margins Available for the Receiver at Different Speed Nodes of the ADS527x Family

SPEED (MSPS)	$T_I/2$ (1)	TYPICAL SETUP/HOLD TIMES (ps)
20	2083	1860
30	1389	1150
40	1042	855
50	833	570
65	641	400
70	595	335

(1) T_I is the time period of the internal 12x CLOCK

2 Capturing LVDS Outputs

While the LVDS interface provides all the features of higher system density, low power and low electromagnetic interference (EMI), the challenge is to capture LVDS serial outputs, especially at higher speed nodes. ADS527x/ADS524x outputs are meant to be deserialized using conventional deserialization techniques, as shown in Figure 2. However, this scheme calls for extremely good matching across channels and between differential pairs at high speeds. Any amount of skew across channels (arising from board trace mismatch, or mismatch within the receiver chip, as well as timing mismatches arising from process variations) can potentially reduce the timing margins for the receiver and fail the simple deserialization scheme.

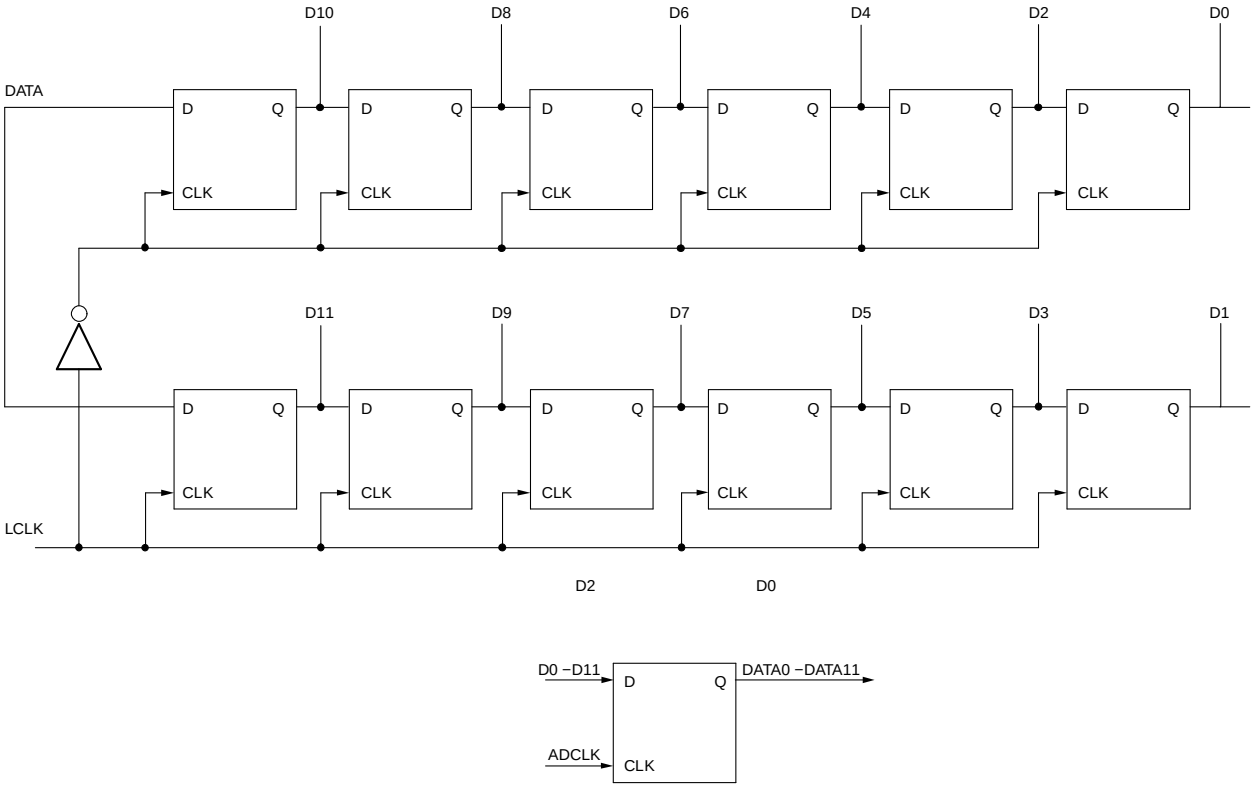

Figure 2. Conventional Deserializer for Capturing Serial Data from ADS527x

While this scheme is simple to implement and can be used for low speeds (less than 30MSPS of ADC operation), it is not suitable for higher speed nodes. For speed nodes that can offer only sub-nanosecond timing margins, this scheme may not be robust in practical situations primarily because it does not have the capability to compensate for data skew.

In the presence of skew, the available setup and hold times get crunched considerably, leading to potential false captures. Figure 3 demonstrates a superior scheme for deserialization primarily aimed at high speed deserialization. The deserializer is based on a PLL or a delay locked loop (DLL) that generates eight different equivalently-spaced phases of the same clock. Each channel is deserialized using high-speed deserializers; the deserialization clock pairs are obtained from one of the eight sets of the PLL/DLL, the pair being out of phase.

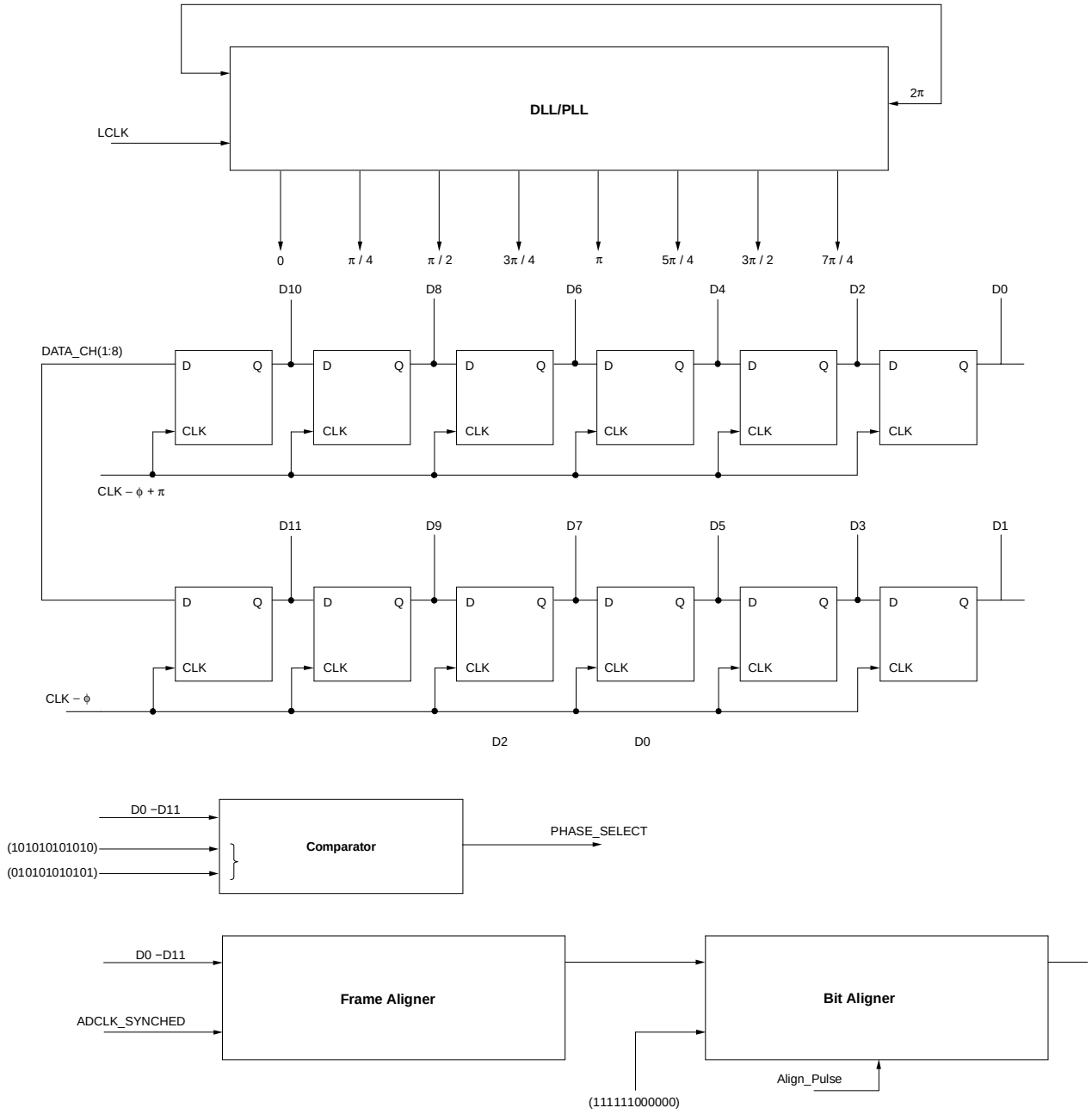

Figure 3. Deserializer Architecture for Extending Receiver Capture Rate

Each data channel is fed to two parallel sets of 6-bit deserializer inputs clocked with these two out-of-phase clocks. The ADS527x/ADS54x provides useful user modes for high-speed serial interface. One such mode is the deskew mode, wherein the device gives out an alternate sequence of '101010…' Each data channel is deserialized and the outputs are compared against **101010101010** and **010101010101**. A phase sweep of the DLL/PLL outputs for each data channel leads to one or more phases for which the capture point is stable for that channel. A simple algorithm can then fix up the required phase of the DLL/PLL that is needed to efficiently capture the given channel.

The 1x clock is also synchronized with respect to LCLK. The synchronized clock is used to latch to parallel outputs of the deserializer. One other mode offered by this family of devices is the synchronization mode, wherein each data line gives an output equivalent to the 1x clock. By programming the device in this mode, the user can expect an output of **111111000000**. The user might observe a bit shift in this process that results from a bit length mismatch during deskewing. This shift is static and can be calibrated out while in synchronization mode.

Once the capture solution is calibrated out using deskew and synchronization, it can be efficiently used for data capture, even at high speeds.

3 General Design Guidelines

When designing the interface between the ADS527x/ADS524x and the receiver, follow these general guidelines:

- The delays of the data and clock outputs should remain well-matched within the device. Ideally, the bit clock is expected to transition in the middle of the valid data window. Depending on the data setup and hold time specifications of the receiver, a constant delay could be added in the bit clock path in order to increase the data setup time at the expense of the data hold time.
- Match the traces from the output pins of the ADS527x/ADS524x to the receiver input pins for all data and clock channels. In general, keep trace lengths as short as possible to get the best eye patterns from the LVDS data. Also, consider effects such as crosstalk that could potentially reduce the data valid time.
- Match the loading on all channels.
- Jitter performance of the DLL/PLL is critical, especially at speed nodes of 300Mbps and greater. To obtain the best jitter performance, use a separate power supply for the DLL/PLL.
- Ensure that the LVDS termination resistors are laid out close to the LVDS receiver pins (or, if possible, internal to the receiver chip). If using internal termination on the receiver, note that the waveforms seen on the receiver pins may not be accurate representations of the actual waveforms seen inside the receiver. This difference is because of the effects of package parasitics that exist between the receiver pins and the internal termination.
- LVDS lines should be routed differentially with minimum loop area.
- The LVDS pair should be routed on a single layer without inserting vias. If vias are required, there should also be ground vias in the vicinity to ensure proper return paths.
- Use the ADS527x/ADS524x LVDS IBIS models (available for download at www.ti.com) to perform signal integrity checks on the board. One of the four LVDS current modes can be chosen at this stage to provide the required output swing and best signal integrity. Table 3 lists the respective IBIS models for these devices.

Table 3. Available IBIS Models for ADS527x/ADS524x

DEVICE NAME	LITERATURE NUMBER
ADS527x	SBAM004
ADS524x	SBAM003

4 Conclusion

The ADS527x/ADS524x families of devices offer high performance and system density. These devices are ideal for applications such as ultrasound and medical imaging that require very high system density. The serial data interface minimizes I/O and package size, but creates a challenge with the capture mechanism. This application note illustrates a simple deserialization technique and outlines the reasons why it does not work reliably for higher data rates. It then shows a more robust deserialization technique that makes use of the test patterns given out by the ADS527x family of devices. This technique compensates for the skews between the data channels and clock. This technique also effectively positions the clock and data optimally for each channel, in order to maximize the setup and hold times for capture.

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