

High-Voltage Signal Conditioning for Differential ADCs

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ABSTRACT

Analog designers are frequently required to convert high-voltage signals to levels acceptable to low-voltage data converters with differential inputs. This paper describes solutions for this common task using modern amplifiers and typical power supplies. Three examples of conditioning $\pm 10\text{V}$ bipolar signals for low-voltage analog-to-digital converters (ADCs) are shown; a single-supply design, a modular design, and a fully-differential design.

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Introduction

Analog front-end designers are often confronted with the challenge of coupling high-voltage bipolar signals to differential ADCs operating on low-voltage single rail power supplies. Many applications continue to use high-voltage bipolar analog signals. Differential inputs are becoming more common on high-resolution data converters because of improved signal quality, noise cancellation and ground-loop isolation. As a result, traditional single-part high-voltage converters are becoming obsolete. Modern ADCs are designed on small geometry processes because of advanced digital capabilities, higher yields, and lower costs. Op amps, on the other hand, are designed on large geometry processes to withstand higher internal voltages and allow precise control of internal elements. Modern op amps offer a number of outstanding features, such as rail-to-rail I/O, wide common-mode range, linear transfer functions, low power consumption and low-voltage operation. Another solution, the fully-differential op amp, is an emerging topology ideal for differential converters. By using discrete op amps and ADCs, designers can optimize circuit performance by using the proper part and avoiding expensive, compromised, single-part solutions.

1 Circuit 1: The Single-Supply Approach

The circuit shown in Figure 1 uses two precision op amps with a single 3V supply. The first stage attenuates the incoming $\pm 10V$ signal. The second stage provides a complementary output. Level-shift can be adjusted by changing the reference voltage at the noninverting input to U_3 .

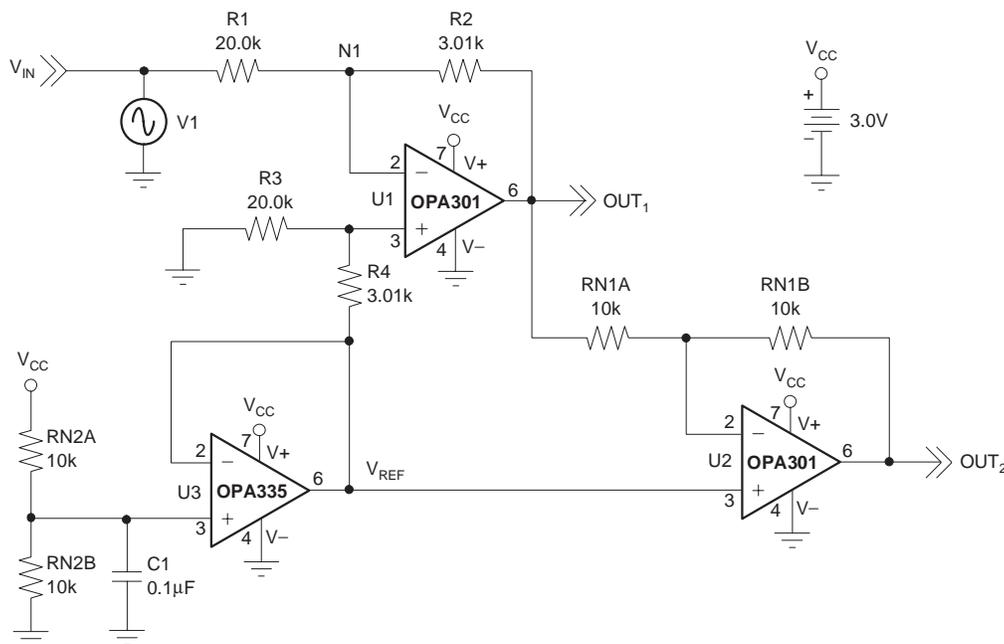


Figure 1. Circuit 1: Single-Supply

The bias components are related by the following formula:

$$R1 = R3$$

$$R2 = R4$$

$$\frac{R1}{R2} = \frac{V_{IN}}{V_{OUT}}$$

The circuit in Figure 1 uses the following values:

$$V_{OUT} = 3V$$

$$V_{IN} = 20(\pm 10)V$$

$$R1 = R3 = 20.0k \ 1\%$$

$$R2 = R4 = 3.01k \ 1\%$$

$$V_{REF} = \text{midpoint of ADC full-scale input range}$$

This design is relatively straightforward. Gain errors are reduced by the use of resistor networks in the second stage and the reference divider. Two inverting stages are used to keep the input common-mode voltage constant. This configuration allows the use of amps with non-rail-to-rail input such as the OPA301, which is optimized for driving 16-bit data converters. The DC sweep of Circuit 1 is shown in Figure 2. This design can be used with input voltages far outside the power-supply rails; however, designers need to pay attention to the power dissipated in R_1 and as well as component matching. Additionally, note the use of the OPA356 as a reference buffer. High-speed reference buffers are essential for optimal circuit performance.

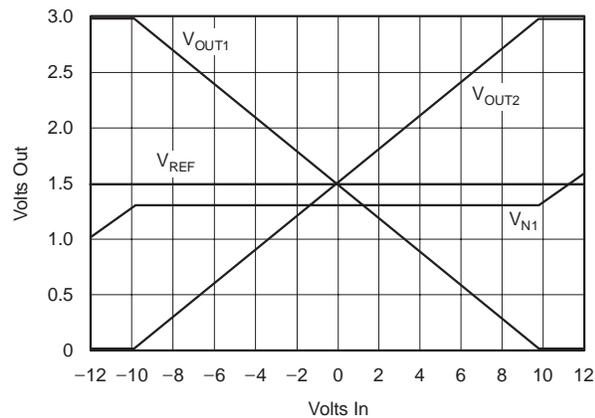


Figure 2. DC Sweep of Circuit 1

2 Circuit 2: A Modular Approach

The circuit shown in Figure 3 is modular for an absolute range. The first stage is attenuation of the bipolar input. The second stages are level-shifting and phase inversion. This style is convenient because designers can compartmentalize adjustments. The overall input range can be adjusted by changing R1, while the output range can be changed by adjusting the REF4V096. For example, the REF4V096 could be connected to V_{CC} . The mid-point can be adjusted at the noninverting input to U3. Thus, for example, this could be connected to a CM output from a data converter. (Conversely, the output of U3 could be connected to a CM input of a data converter.) These parameters are independent and can be tuned with a minimum of interaction. Furthermore, designers may want to include filtering for anti-aliasing or other analog functions; these blocks can be neatly inserted at node N2.

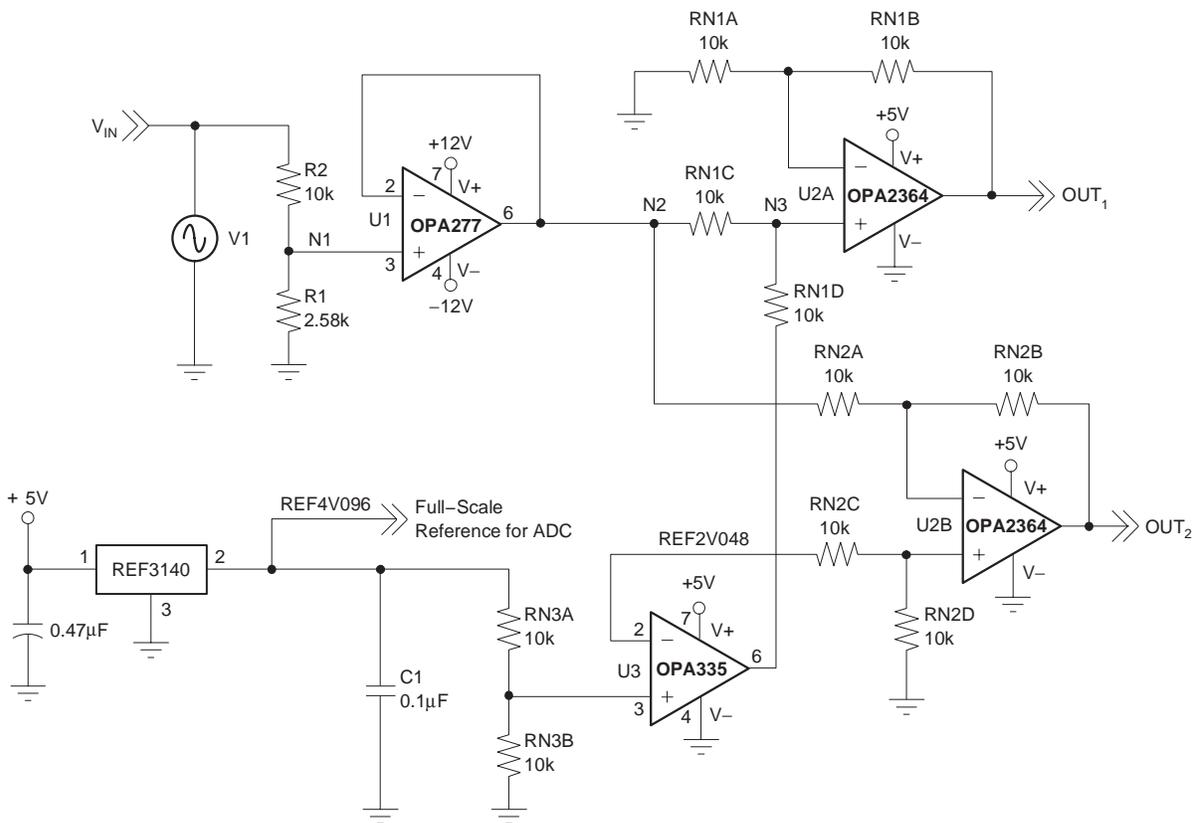


Figure 3. Circuit 2: Modular

On the front-end voltage divider, the equation for R1 is:

$$R1 = \frac{(V_{OUT} \cdot R2)}{(V_{IN} - V_{OUT})} \quad (1)$$

In Circuit 2, the following values are used:

$$V_{OUT} = 4.096V = OUT_1 - OUT_2$$

$$V_{IN} = 20(\pm 10)V = V_1$$

$$R1 = 2.56k \text{ (2.58k is closest standard value)}$$

$$R2 = 10k$$

$$V_{REF} = 4.096V$$

These component values can be altered to account for different input ranges or input impedance requirements. In this example, the value of R₂ is held constant to simplify calculations and reduce trimming to one element.

The first stage op amp is an OPA277. The OPA277 was chosen for its low V_{IO}, low drift, and bipolar swing. This stage needs to have bipolar swing about ground because the input signal is bipolar. The OPA277 is also a great candidate for active-filter stages. TI's free FilterPro design tool (available for download at www.ti.com) can be used to design and model active filters. FilterPro presumes that the amplifiers under consideration are operating in a bipolar mode, making node N1 the appropriate place for filters. Another option for the first stage is the OPA725, which is suitable for bipolar stages with ±5V rails.

The second stage op amp is the OPA2364. This outstanding, low-voltage op amp offers many assets which are ideal for this stage: it is low-voltage and low-power, in addition to having a large input common-mode voltage range. It also has zero input crossover distortion for linear, monotonic, large-signal output.

Resistor networks are used to bias the OPA2364 and the reference because they are matched. This ratiometric design takes advantage of this property. Gain errors from mismatched components cannot be distinguished from genuine signals. For example, the gain error from discrete 1% components is equivalent to -40dB of erroneous signal. This is inadequate for 12-bit, or higher, conversions, where the minimum detectable signal is below -70dB. Resistor networks with ratio 0.01% tolerances (-80dB) are readily available. High-quality metal foil networks with 0.005% tolerances (-106dB) may be necessary for extreme cases.

Figure 3 shows Circuit 2 with the REF3140, a 4.096V reference. The 4.096V range of the REF3140 makes 1LSB = 1mv on a 12-bit ADC. This design would be ideal for the ADS7817, ADS8325 or similar ADC. Moreover, this design can be easily converted to low-voltage rails in the second stage. The OPA2364 can operate down to 1.8V_{DC}, and this design allows V_{CC} to be used as the reference. Conversion to low-voltage rails is straightforward; the ADC reference and the reference shown in Circuit 2 should be identical, the reference must be buffered, and R1 must be rescaled using the formula above (Equation 1).

Figure 4 shows the DC sweep plot of Circuit 2. Node N3 shows the input common-mode voltage of the second stage. A non-RRI amp, such as the OPA301, could be used here, if the input common-mode voltage falls within the device limits.

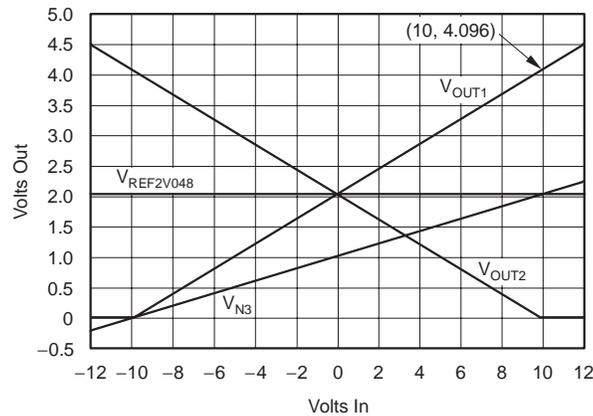


Figure 4. DC Sweep of Circuit 2

Designers may want to consider the INA2132 for the second stage. These amps are considerably slower than the OPA2364, but they come with precision-matched internal resistors to reduce gain errors. In general, DC precision is desirable for open-loop applications such as temperature sensors or calibrated transducers, where absolute accuracy, offset and drift are critical. This precision makes the INA132 a good choice for absolute measurements. In closed-loop applications such as servos loops or PID controllers, high-speed and monotonicity are desirable. In closed-loop systems, DC offsets and gain errors will be canceled by feedback and calibration. This makes the OPA2364, or the OPA301, both good choices for servos and feedback signals.

3 Circuit 3: A Fully-Differential Approach

Circuit 3 shows the THS4121. (See Figure 5.) Newer fully-differential amplifiers, such as the THS4121, make single-ended to differential conversion a simple process. The THS4121 is designed for high-speed applications that use transformer-coupling and differential converters. The THS4121 offers suitable performance down to DC for low-resolution applications. The output range has been decreased to avoid clipping because the outputs are not rail-to-rail. In spite of these restrictions, designers will be attracted to the uncomplicated configuration as well as the low-voltage requirements, single-supply and small size of the device. This design is intended for use with the ADS8324 or ADS7817 converters. Both these converters are offered in very small MSOP-8 packages.

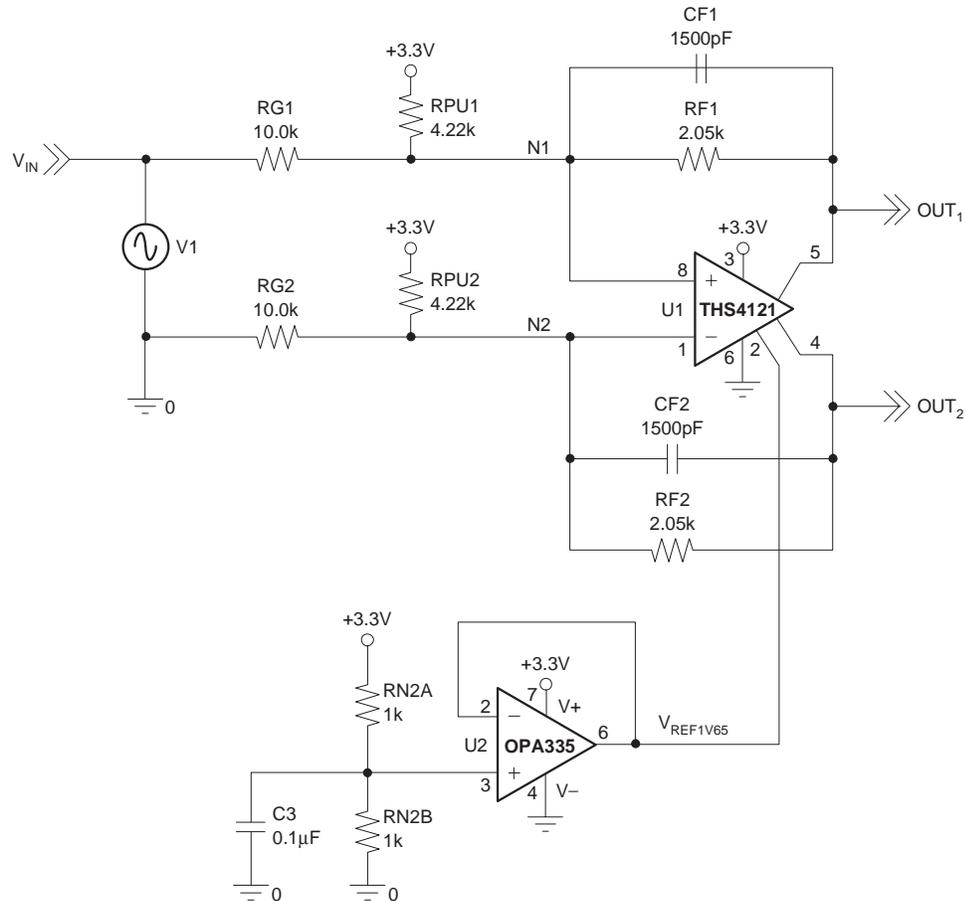


Figure 5. Circuit 3: Fully-Differential

The bias components are related by the following formula:

$$RG_1 = RG_2$$

$$RF_1 = RF_2$$

$$\frac{RF_1}{RG_1} = 1/2 \cdot \frac{V_{IN}}{V_{OUT}}$$

In Circuit 3, the following values are used:

$$V_{OUT} = 2V = (OUT_1) - (OUT_2)$$

$$V_{IN} = 20V(\pm 10V) = V_1$$

$$R1 = R3 = 10.0k$$

$$R2 = R4 = 2.050k \ 1\%$$

The THS4121 also needs pull-up resistors to keep the input common-mode voltage within limits. The equation given for R_{PU} in the THS4121 product data sheet is:

$$R_{PU} = \frac{(V_P - V_{DD})}{\left[\frac{(V_{IN} - V_P)}{RG} + \frac{(V_{OUT} - V_P)}{RF} \right]} \quad (2)$$

For this application, we targeted the input common-mode voltage to be in the middle of the common-mode input voltage range for the THS4121 when V_{IN} is zero.

$$V_{DD} = V_{CC} = 3.3V$$

$$V_P = 1.925V = \frac{[0.65 + (V_{DD} - 0.35)]}{2}$$

$$V_{IN} = 0V$$

$$V_{OUT} = 1.65V$$

$$R_G = 10.0k$$

$$R_F = 2.05k$$

$$R_{PU} = 4.22k$$

Feedback capacitors have also been added to reduce wideband noise and help stabilize the amp. In general, $\pm 10V$ signals are not high-frequency because of slew-rate limitations, so narrow-banding only affects unwanted signal components.

Figure 6 shows a DC sweep of Circuit 3.

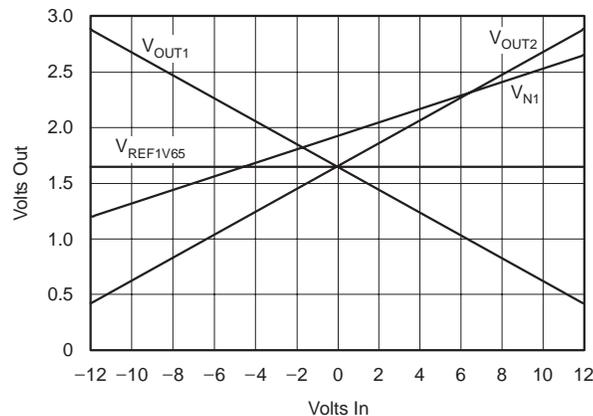


Figure 6. DC Sweep of Circuit 3

For more information on fully-differential amplifiers and active filtering, please review TI Application Note SLOA054D (available for download at www.ti.com).

4 Voltage References and Ranges

The references shown in these examples are simple. They are for ratiometric applications where the ADC range is the rail. The references shown are $V_{CC}/2$, or at the mid-scale of the ADC range. This proportion is required for these circuits. 3.3V or 5V can be used in any of these designs; the references would be 1.65V or 2.5V, respectively. These designs will work with absolute references as well, as long as the V_{REF} is one-half of the ADC full-scale range.

The other requirement is a good buffer driving the reference signal. These designs put a wide range of loads on the reference, and a buffer is essential. For in-depth information on buffering references for precision and high-resolution designs, please see Application Note SBVA002, *Voltage Reference Filters*.

References

Karki, J. Fully-Differential Amplifiers. Application note. (SLOA054x)

Stitt, R.M. Voltage Reference Filters. Application note. (SBVA002)

FilterPro™ MFB and Sallen-Key Design Program. Executable program. (SLVC003.zip)

THS4121 Product data sheet. (SLOS319x)

To obtain a copy of the referenced documents, visit the Texas Instruments web site at www.ti.com. x indicates the current revision letter for each document.

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