*EVM User's Guide: ADS8681WEVM-PDK*

# *ADS8681WEVM-PDK Evaluation Module*

## Description

The ADS8681WEVM-PDK is a platform for evaluating the performance of the ADS8681W, an integrated data acquisition system based on a successive approximation register (SAR) analog-to-digital converter (ADC). This device features a high-speed, high-precision SAR ADC, integrated differential analog front-end (AFE) input driver circuit, over-voltage protection circuit up to ±20V, and an on-chip 4.096V reference with extremely low temperature drift. The evaluation kit includes the ADS8681WEVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over Universal Serial Bus (USB) for data capture, configuration, and analysis.

## Get Started

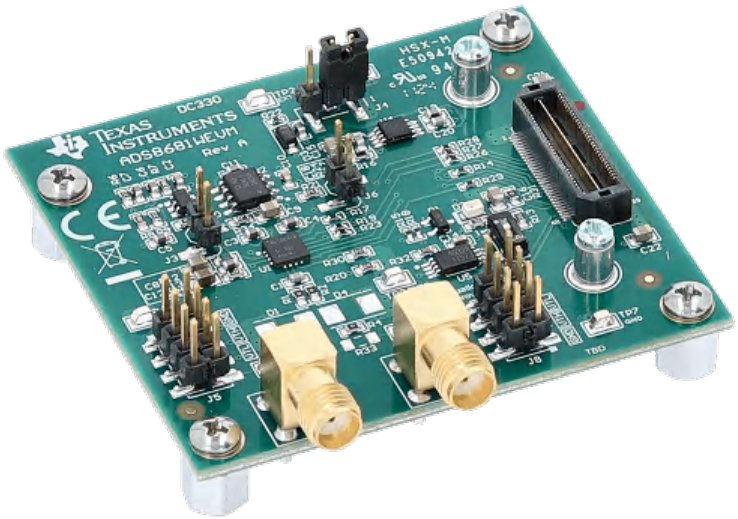
1. Order the ADS8681WEVM-PDK from ti.com
2. Download and install the ADS8681WEVM GUI Software
3. Connect the ADS8681WEVM to the computer with the included USB cable
4. Launch the ADS8681WEVM GUI from the start menu
5. For IC details, refer to the ADS8681W data sheet
6. Visit the E2E forums for support and questions

## Features

- 16-bit ADC with integrated analog front-end
- High speed: 1MSPS
- Software programmable input ranges
  - Bipolar differential ranges: ±12.288V, ±10.24V, ±6.144V, ±5.12V, and ±2.56V
  - Unipolar differential ranges: 0V–12.288V, 0V–10.24V, 0V–6.144V, and 0V–5.12V
- Analog supply (5V): 1.65V to 5V I/O supply
- Constant resistive input impedance ≥ 1MΩ
- Input bandwidth: 450kHz
- Input overvoltage protection: up to ±20V
- On-chip, 4.096V reference with low drift
- Excellent performance:
  - DNL: ±0.6LSB; INL: ±0.6LSB
  - SNR: 80dB; THD: –95.5dB
- ALARM feature with high, low threshold

## Applications

- Analog input modules
- Semiconductor tests
- Servo drive control modules



# 1 Evaluation Module Overview

## 1.1 Introduction

The ADS8681W features a high-speed, high-precision SAR ADC, integrated differential AFE input driver, an on-chip 4.096V reference with extremely low temperature drift, and supports input ranges up to ±12.288V. The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS8681W
- Supplies power to all active circuitry on the ADS8681WEVM board

This user's guide describes the characteristics, operation, and use of the ADS8681W evaluation module (EVM). The ADS8681WEVM enables the evaluation of the device through a USB interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS8681WEVM.

## 1.2 Performance Development Kit Contents

The ADS8681WEVM Performance Development Kit (PDK) includes the following:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS8681W.
- The PHI controller, which provides a convenient communication interface to the ADS8681W over USB 2.0 (or higher).
- Easy-to-use evaluation software for 64-bit Microsoft® Windows® 10 or 11 operating systems.
- The software suite includes graphical tools for data capture, histogram analysis, spectral analysis, linearity analysis,and custom configuration of the ADS8681W. This suite also has a provision for exporting data for post-processing.

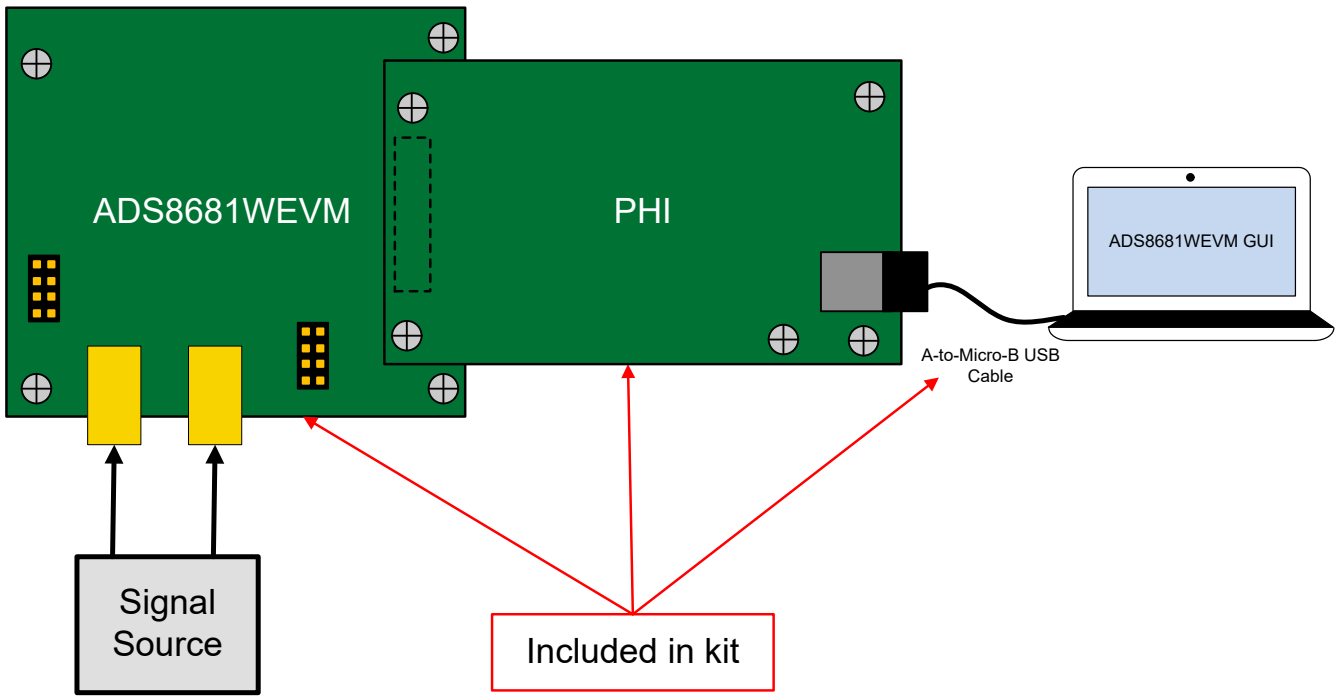



**Figure 1-1. System Connection for Evaluation**

## 1.3 Specification

The following specifications are applicable to the ADS8681WEVM board and the PHI.

**Table 1-1. ADS8681WEVM-PDK Specifications**

| Parameter | Conditions | | Value |
|---|---|---|---|
| Temperature | Recommended operating free-air temperature range, $T_A$ | | 15°C ≤ $T_A$ ≤ 35°C |
| External power supply voltage | Recommended voltage range for TP2 to GND | | 6V ≤ $V_{EXT}$ ≤ 9V |
| Analog input range | AIN_P − AIN_M | Input range = ±3 × $V_{REF}$ | -12.288V ≤ AIN_x ≤ 12.288V |
| | | Input range = ±2.5 × $V_{REF}$ | -10.24V ≤ AIN_x ≤ 10.24V |
| | | Input range = ±1.5 × $V_{REF}$ | -6.144V ≤ AIN_x ≤ 6.144V |
| | | Input range = ±1.25 × $V_{REF}$ | -5.12V ≤ AIN_x ≤ 5.12V |
| | | Input range = ±0.625 × $V_{REF}$ | -2.56V ≤ AIN_x ≤ 2.56V |
| | | Input range = 3 × $V_{REF}$ | 0V ≤ AIN_x ≤ 12.288V |
| | | Input range = 2.5 × $V_{REF}$ | 0V ≤ AIN_x ≤ 10.24V |
| | | Input range = 1.5 × $V_{REF}$ | 0V ≤ AIN_x ≤ 6.144V |
| | | Input range = 1.25 × $V_{REF}$ | 0V ≤ AIN_x ≤ 5.12V |

## 1.4 Device Information

The ADS8681W is a high-speed, high-performance, easy-to-use integrated data acquisition system device. This single-channel device supports true bipolar differential and single-ended input voltage swings up to ±12.288V and operates on a single 5V analog supply

The ADS8681W consists of a high-precision successive approximation register (SAR) analog-to-digital converter (ADC) and a power-optimized analog front-end (AFE) circuit for signal conditioning. The ADS8681W includes:

- A high-resistive input impedance (≥ 1MΩ) that is independent of the sampling rate
- A programmable gain amplifier (PGA) with a differential and single-ended input configuration supporting nine software-programmable unipolar and bipolar input ranges
- A second-order, low-pass anti-aliasing filter
- An ADC driver amplifier that provides quick settling of the SAR ADC input for high accuracy
- An input over-voltage protection circuit up to ±20V

The integrated precision AFE circuit includes high input impedance and a precision ADC operating from a single 5V supply. This AFE circuit offers a simplified end design without requiring external high-voltage bipolar supplies and complicated driver circuits.

# 2 Hardware

## 2.1 EVM Analog Interface

The ADS8681W features integrated analog front-end circuitry with a constant resistive input impedance, relieving the requirement of external buffer amplifier circuit. The ADS8681WEVM is designed for easy interfacing with analog sources. This section covers the details of the front-end circuit including jumper configuration for different input test signals and board connectors for single-ended and differential sources.

### *2.1.1 ADC Analog Input Signal Path*

The ADS8681WEVM is designed for easy interfacing to analog sources via SMA connector. J1 and J7 of the ADS8681WEVM are SMA connectors that allow single-ended and differential analog source connectivity to the input signal path of the ADS8681W through a coaxial cable. The schematic for the analog input signal path is shown in Figure 2-1.

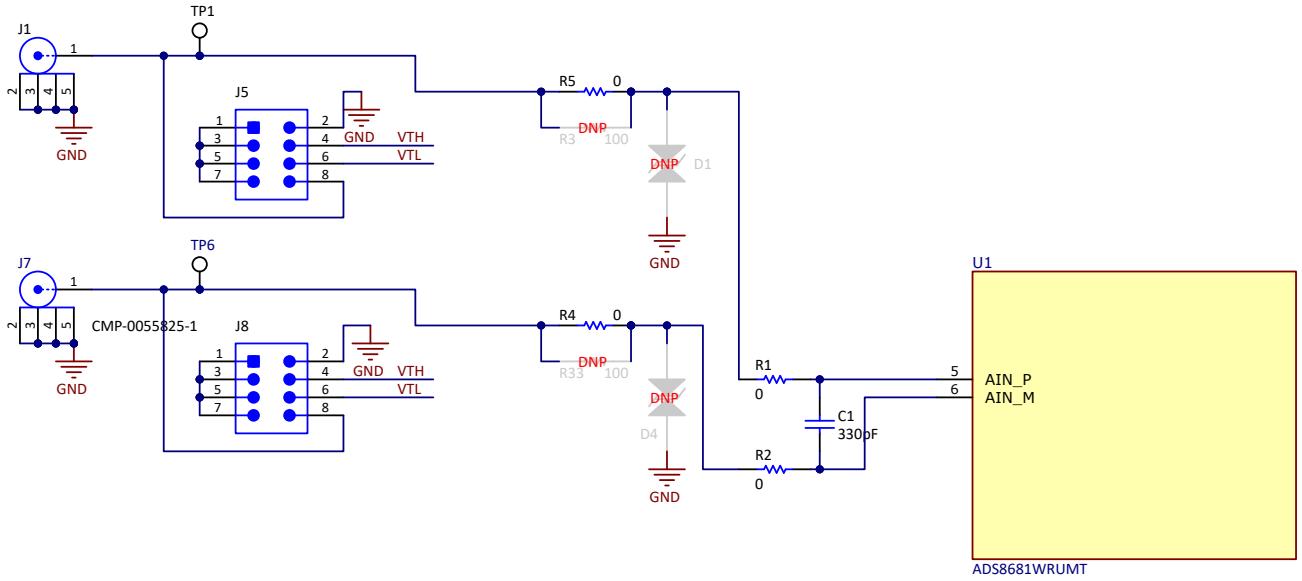



**Figure 2-1. Schematic of Input Signal Path**

When evaluating the ADS8681W performance on the EVM board, the proper resistor values can be used together with a 330pF capacitor (C0G type) to compose a low-pass filter on the input path.

The internal over-voltage protection circuit of the ADS8681W withstands up to ±20 V on the analog input pin. However, external protection circuitry is utilized to provide additional over-voltage protection with transient voltage suppressors (TVS) D1 and D4, and high-power resistors (MMA0204 footprint) R3 and R33 on the input signal path to the ADS8681W.

AIN_P and AIN_M are also accessible through pin 8 of header J5 and pin 8 of header J8 respectively. The odd-numbered pins of J5 and J8 are shorted together on the board and can be jumpered to any one of the even numbered pins which are marked as “GND”, “VTH”, or “VTL”.

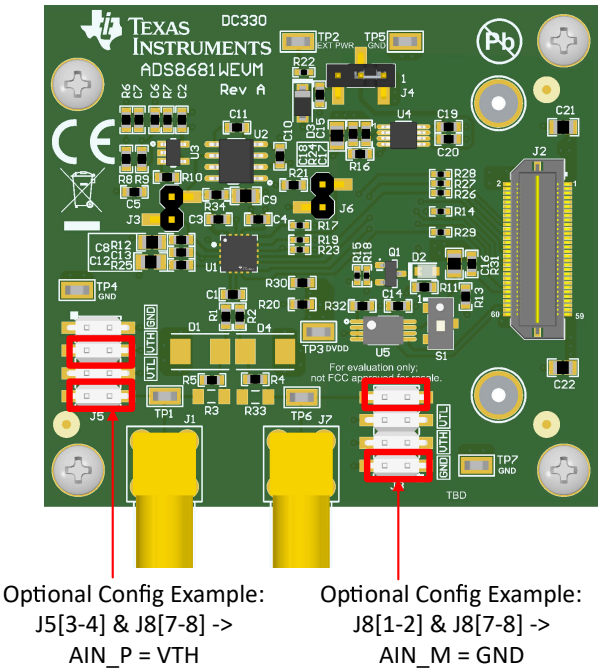



**Figure 2-2. Connectors and Jumpers for Input**

The EVM board provides buffered DC voltage sources that have nominal values of about 4V and 100mV. Header pins J5.Pin4 and J8.Pin4 provide a 4V output (VTH). Header pins J5.Pin6 and J8.Pin6 provide a 100mV output (VTL). These DC voltage pins are useful for debugging any potential problems with the front-end circuit or the ADC. The jumper settings for using VTL and VTH on-board voltage signal and external input signal on J1 and J7 are summarized in Table 2-1 and Table 2-2, respectively.

**Table 2-1. Jumper Settings on J5 for AIN_P**

| Input | Value | J5.Pin1 < > J5.Pin2 | J5.Pin3 < > J5.Pin4 | J5.Pin5 < > J5.Pin6 | J5.Pin7 < > J5.Pin8 |
|---|---|---|---|---|---|
| VTL | 100mV | Open | Open | Close | Close |
| VTH | 4V | Open | Close | Open | Close |
| GND | Ground | Close | Open | Open | Close |
| External Signal on J1 | | Open | Open | Open | Open |

**Table 2-2. Jumper Settings on J8 for AIN_N**

| Input | Value | J8.Pin1 < > J8.Pin2 | J8.Pin3 < > J8.Pin4 | J8.Pin5 < > J8.Pin6 | J8.Pin7 < > J8.Pin8 |
|---|---|---|---|---|---|
| VTL | 100mV | Open | Open | Close | Close |
| VTH | 4V | Open | Close | Open | Close |
| GND | Ground | Close | Open | Open | Close |
| External Signal on J7 | | Open | Open | Open | Open |

**Note**

In single-ended operation, connect AIN_M to ground by installing jumpers across J8[1,2] and J8[7,8] (see Table 2-2).

### 2.1.2 Onboard ADC Reference

The ADS8681W incorporates a high precision 4.096V internal voltage reference. Alternatively, the REF5040 (U2), an onboard external 4.096V precision voltage reference, is selectable for evaluation purposes if the external voltage reference is necessary for a system application. The reference voltage source is determined by bit 6 of the RANGE_SEL_REG register of the ADS8681W. Configure the reference settings on the ADS8681WEVM-PDK by navigating to the *Register Map Config* page on the GUI as described in Section 4.1.2. By default, the internal reference is enabled after the ADC is powered up, so the jumper on J3 must not be connected when powering up. If the ADS8681W must be configured with the external reference, make sure to disable the internal voltage reference by setting bit 6 of the RANGE_SEL_REG register before using a jumper on J3 to connect the external reference. The schematic for the reference path is shown in Figure 2-3.

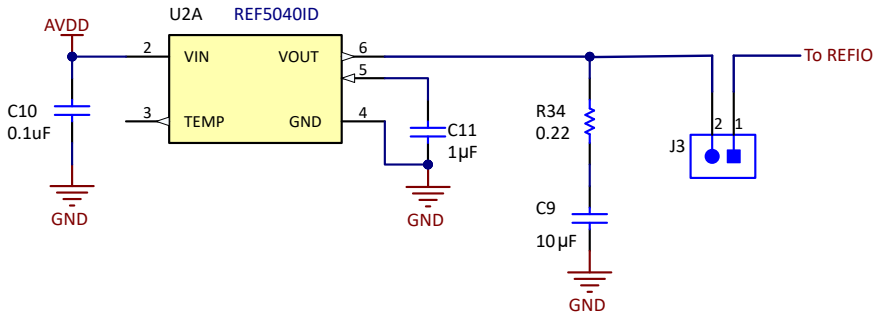



**Figure 2-3. Onboard Reference Signal Path**

## 2.2 Power Supplies

The PHI provides multiple power supply options for the ADS8681WEVM, derived from the USB supply of the computer. The EEPROM on the ADS8681WEVM uses a common 3.3V power supply (EVM_ID_PWR) generated directly by the PHI. The ADC and analog input drive circuits are powered by the TPS7A4901 onboard the EVM. The TPS7A4901 is a low-noise linear regulator that uses the 5.5V supply out of a switching regulator on the PHI to generate a much cleaner 5V output (AVDD) for all analog circuits on the EVM board. The LDO circuit that generates AVDD is shown in Figure 2-4.

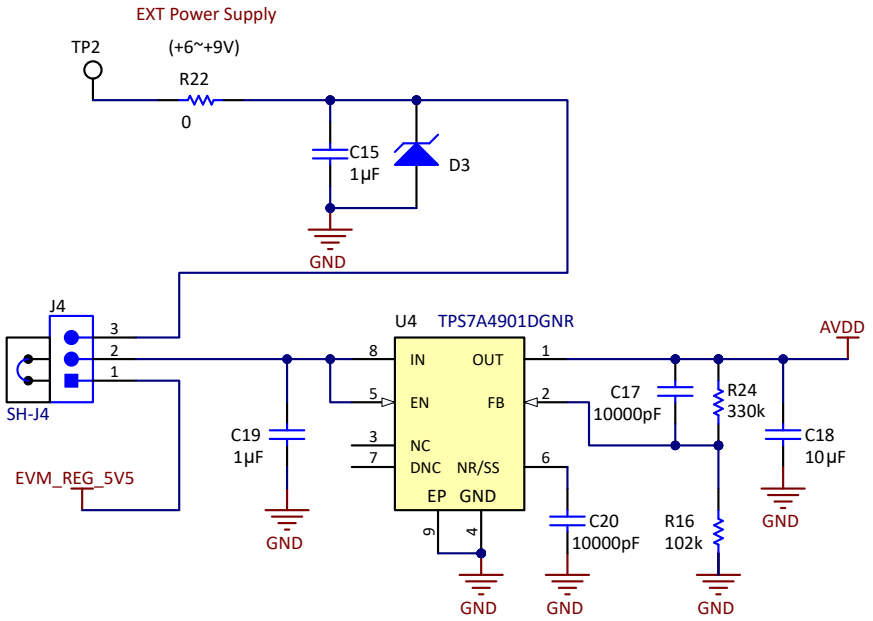



**Figure 2-4. Analog Supply Circuit**

The analog supply can be also provided by an external power supply when a jumper is installed on pin 2-3 position of J4. The 3.3V power supply to the digital section of the ADC is provided directly by an LDO on the PHI (EVM_DVDD).

# 3 Software

## 3.1 Digital Interfaces

As noted in Section 1.1, the EVM interfaces with the PHI controller board which, in turn, communicates with the computer over USB. There are two devices on the EVM with which the PHI communicates – the ADC (over SPI™, U1) and the EEPROM (over $I^2C$, U5). The EEPROM comes pre-programmed with the information required to configure and initialize the ADS8681WEVM-PDK platform. Once the hardware on the EVM board has been initialized, the EEPROM is no longer used and is disabled on the EVM board (refer to Section 3.2.1.)

### *3.1.1 multiSPI™ SPI for ADC Digital IO*

The ADS8681WEVM-PDK supports all the interface modes as detailed in the SBASAY5ADS868x 16-Bit, High-Speed, Single-Supply, SAR ADC DAQ System With Programmable, Bipolar Input Ranges data sheet. In addition to the standard SPI modes (with single-, dual-, and quad-SDO lanes) the multiSPI™ modes support single- and dual-data output rates and the four possible clock source settings as well. The PHI is capable of operating at a 1.8V logic level and is directly connected to the digital I/O lines of the ADC.

The ADS8681WEVM offers 49.9Ω resistors between the SPI signals and J2 to aid with signal integrity. Typically, in high-speed SPI communication, fast signal edges can cause overshoot; these 49.9Ω resistors slow down the signal edges to minimize signal overshoot.

## 3.2 ADS8681WEVM-PDK Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for properly operating the ADS8681WEVM-PDK.

### *3.2.1 Default Jumper and Switch Settings*

Upon unpacking, the EVM is already configured with the default jumper settings, as shown in Figure 3-1.

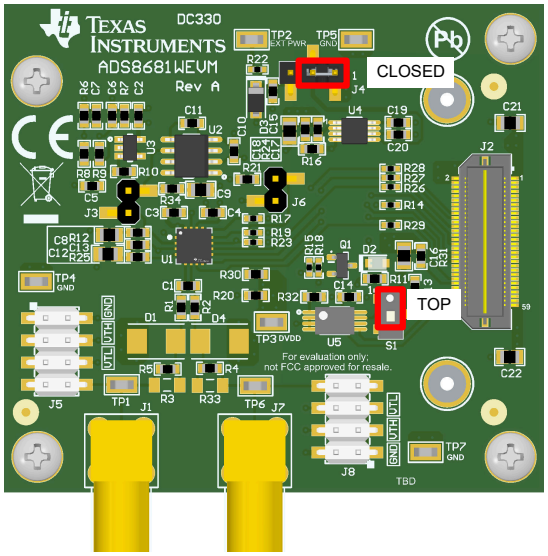



**Figure 3-1. Default Settings for Jumper and Switch**

The default setting includes no jumpers installed on J5 or J8, making J1 and J7 the AIN_P and AIN_M input signal sources respectively. The default position of J4 is position 1-2 so that the linear regulator is powering the system using 5.5V from the PHI controller. Place switch S1 at position 1-2 (to the top) to enable EEPROM write protection. Leave J3 open so the ADC's internal voltage reference is used when powering up. J6 is open to disconnect ALARM output connection to the PHI controller. The locations for the default jumpers and switch are shown in Figure 3-1.

### 3.2.2 EVM Graphical User Interface (GUI) Software Installation

Download the latest version of the EVM GUI installer from the *Order and start development* folder of the ADS8681WEVM-PDKproduct page and run the GUI installer. Accept the license agreements and follow the on-screen instructions to complete the installation as shown in Figure 3-2.

**Note**

The GUI for the ADS8681WEVM-PDK is the ADS8681EVM GUI. The GUI is compatible for both the ADS8681WEVM-PDK and ADS8681EVM-PDK.

As a part of the ADS8681EVM GUI installation, a prompt with a Device Driver Installation appears on the screen as shown in Figure 3-2.

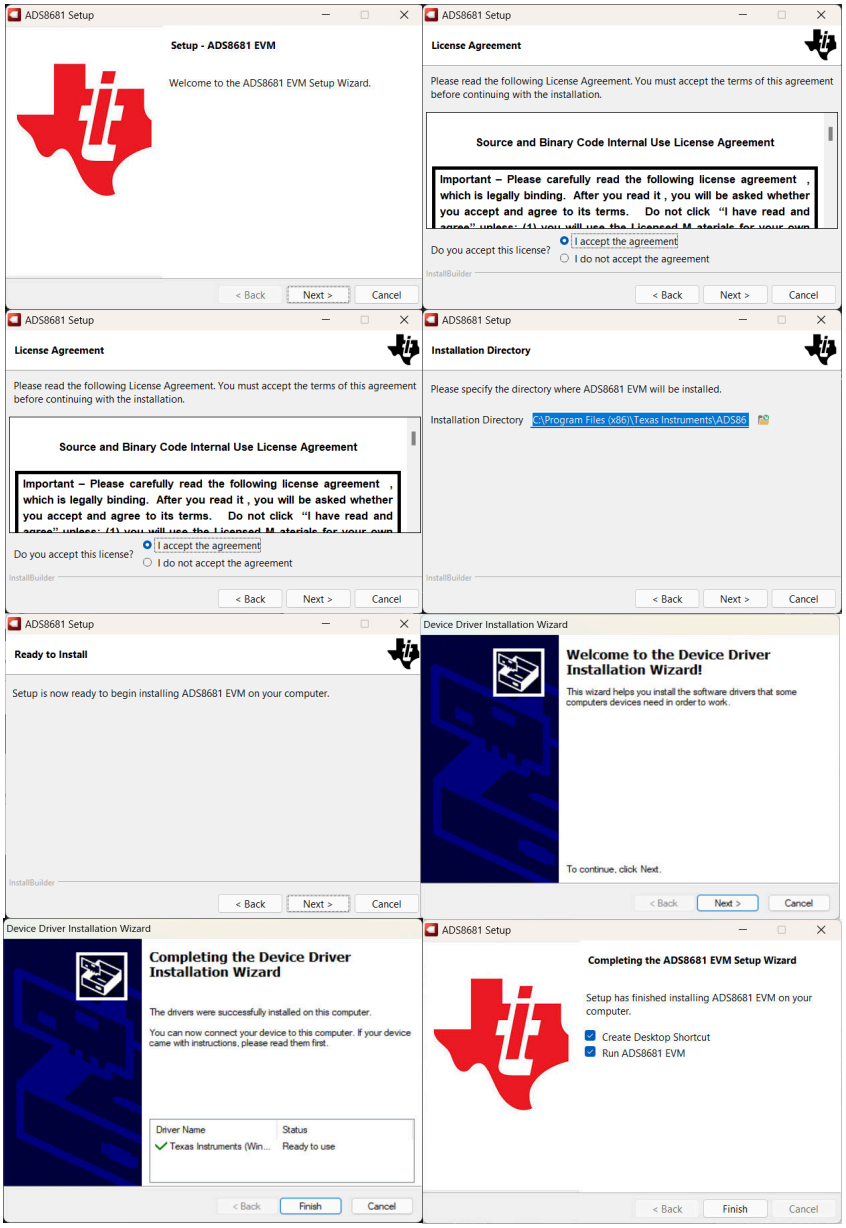



**Figure 3-2. ADS8681W Software Installation Prompts**

After these installations, verify that *C:\Program Files (x86)\Texas Instruments\ADS8681 EVM* installation path is shown in Figure 3-3.

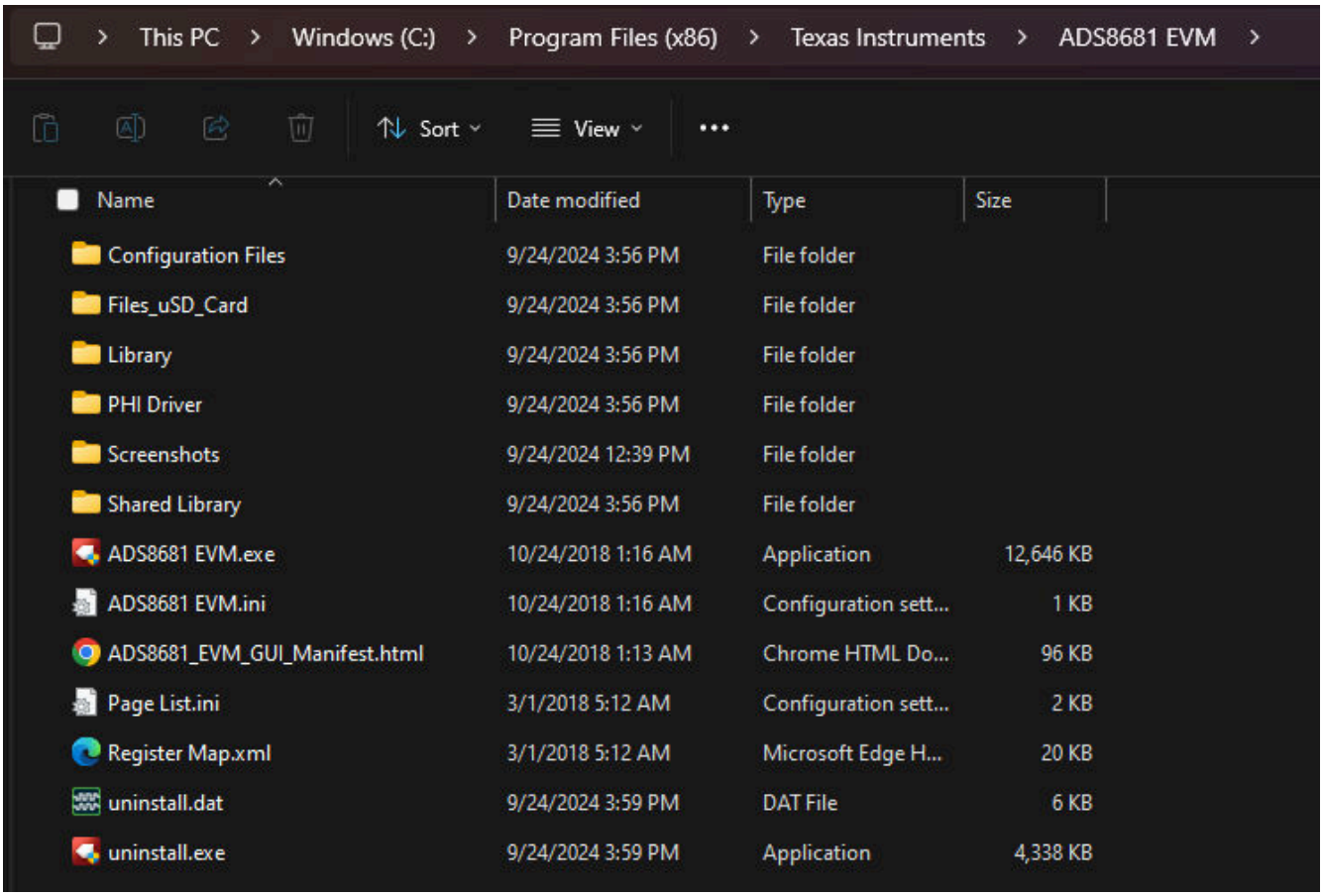



**Figure 3-3. ADS8681EVM GUI Folder Post-Installation**

# 4 Implementation Results

## 4.1 ADS8681WEVM-PDK Operation

The following instructions are a step-by-step guide for connecting the ADS8681WEVM-PDK to the computer and evaluating the performance of the ADS8681W:

1. Connect the ADS8681WEVM to the PHI. Install the two screws as indicated in Figure 4-1.
2. Use the provided USB cable to connect the PHI to the computer
   - LED D5 on the PHI lights up indicating that the PHI has powered up
   - LEDs D1 and D2 on the PHI start blinking, indicating the PHI is booted up and communicating with the EVM

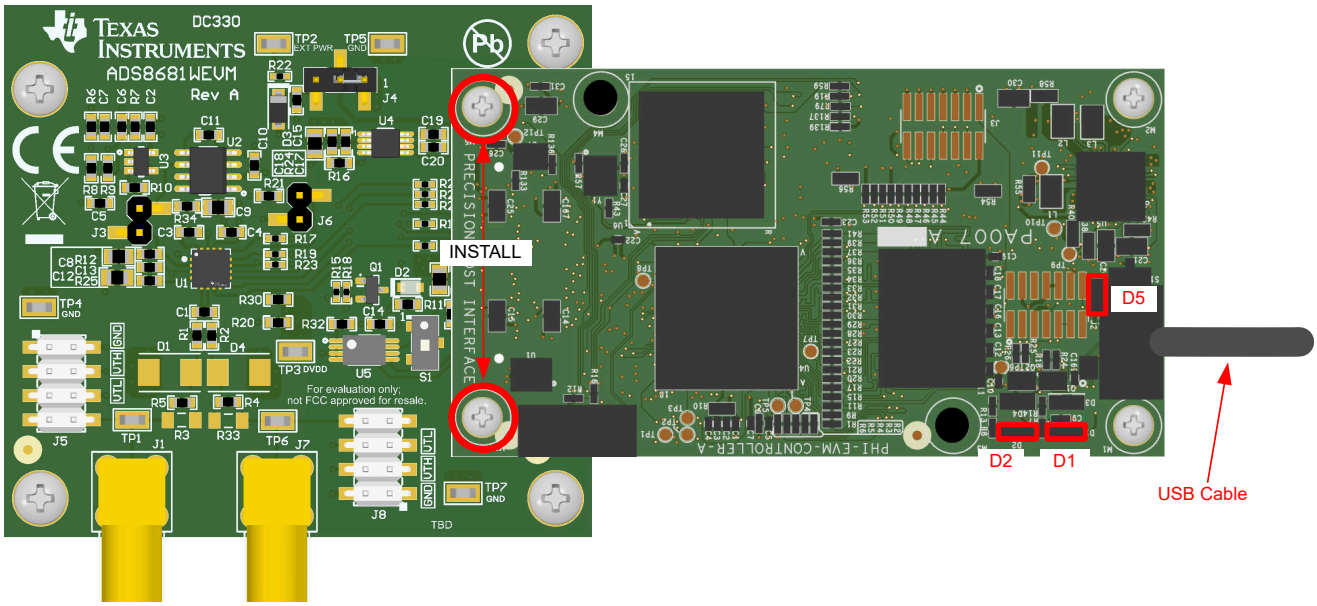



**Figure 4-1. EVM-PDK Hardware Setup and LED Indicators**

3. Launch the ADS8681EVM GUI software from the *Start Menu* of computer, *Desktop Shortcut*, or *Installation* folder (Figure 4-2).

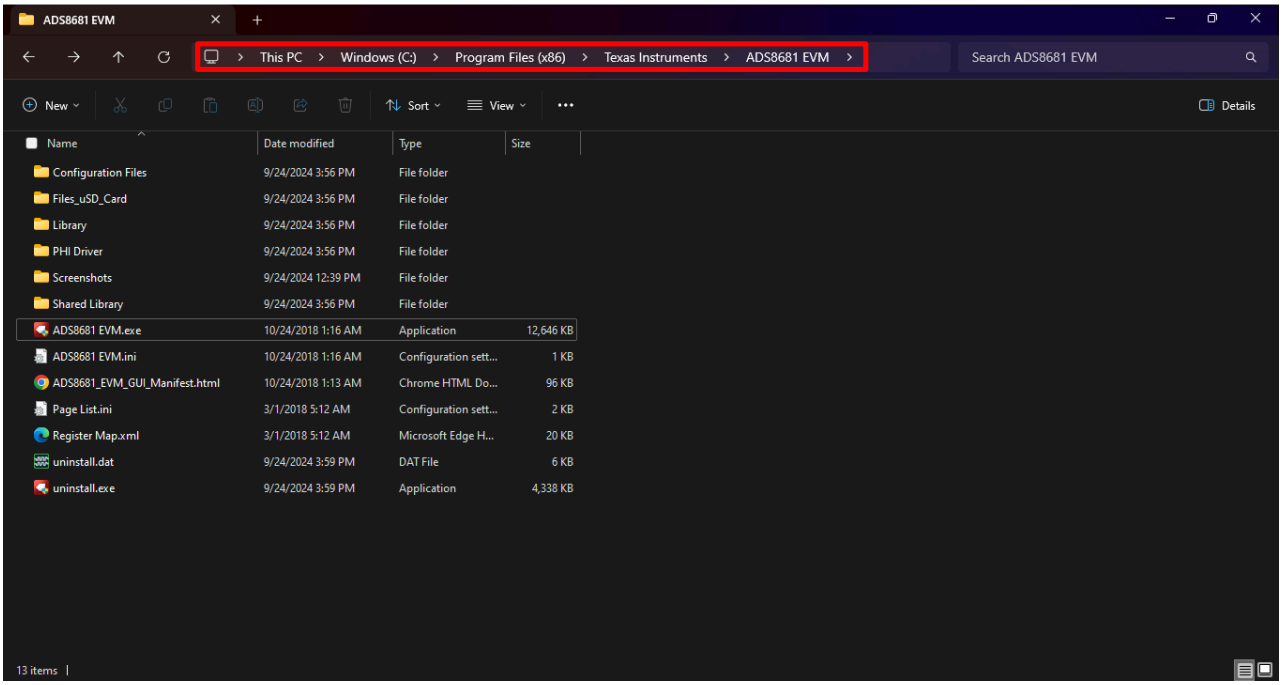



**Figure 4-2. Launch ADS8681EVM GUI Software**

### 4.1.1 EVM GUI Global Settings for ADC control

Although the EVM GUI does not allow direct access to the levels and timing configuration of the ADC digital interface, the EVM GUI does give users high-level control over virtually all functions of the ADS8681W, including interface modes, sampling rate, and number of samples captured.

The various functions of the ADS8681W are exercised through the input parameters of the GUI (as well as the default values), as illustrated in Figure 4-3. These are global settings because the settings persist across the GUI tools listed in the top left pane as *Pages*, which include *Register Map Configuration*, *Time Domain Display*, *Spectral Analysis*, *Histogram Analysis*, and *Linearity Analysis* tools.

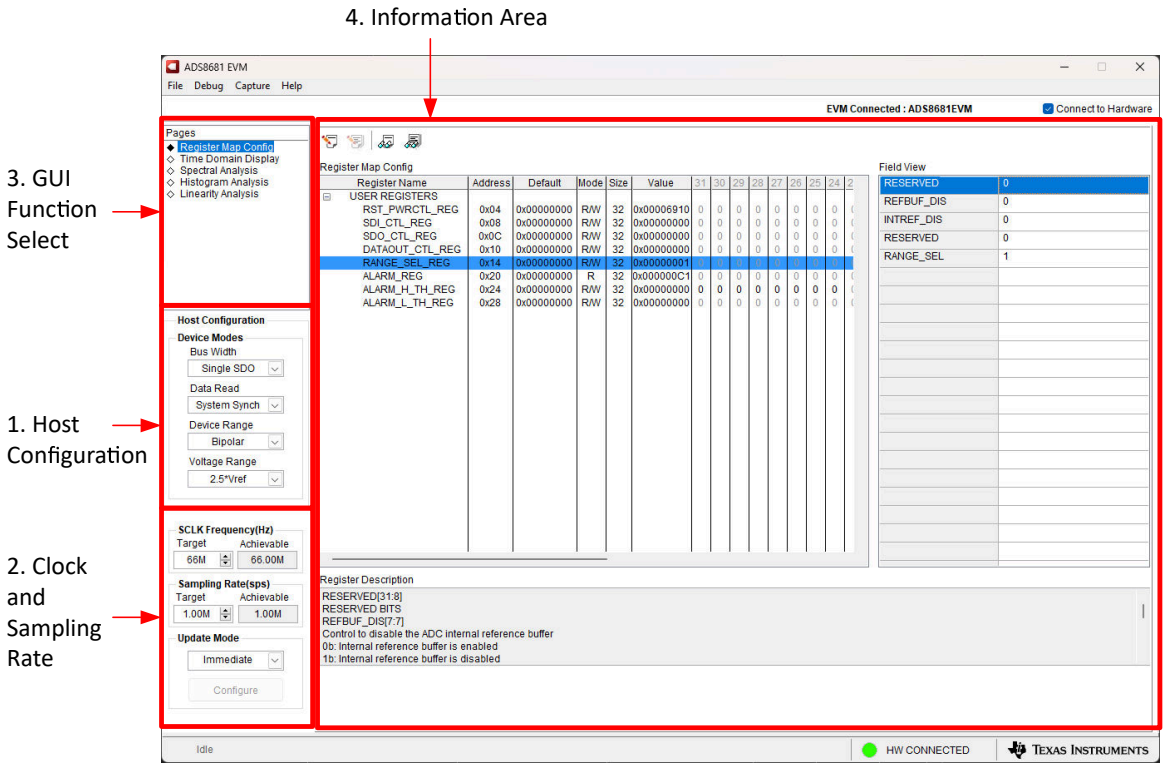



**Figure 4-3. EVM GUI Global Input Parameters**

The host configuration options in this pane allow the choice of various SPI and multiSPI host interface options available on the ADS8681W. The host always communicates with the ADS8681W using the standard SPI protocol over the single SDI lane, irrespective of the mode selected for *Data Capture*.

The drop-down boxes under the *Device Modes* sub-menu allows selection of the data capture mode. The *Bus Width* drop-down allows selection between *Single-*, and *Dual-SDO* lanes; *Data Read* between *Source* and *System Synchronous* modes; *Device Range* between *Bipolar* and *Unipolar* modes, and *Voltage Range* between 3 × Vref, 2.5 × Vref, 1.5 × Vref, 1.25 × Vref, and 0.625 × Vref options. Detailed descriptions of each of these modes are available in the ADS868x 16-Bit, High-Speed, Single-Supply, SAR ADC DAQ System With Programmable, Bipolar Input Ranges data sheet.

Selection of *SCLK Frequency* and *Sampling Rate* is allowed on this pane and is dependent of the *Device Modes* selected. Select or specify a target SCLK frequency (in Hz) and the GUI tries to match this as closely as possible by changing the PHI PLL settings and the achievable frequency that can differ from the target value displayed. Similarly, the sampling rate of the ADC can be adjusted by modifying the *Target Sampling Rate* argument (also in Hz). The achievable ADC sampling rate can differ from the target value, depending on the applied SCLK frequency and selected *Device Mode* and the closest match achievable is displayed. This pane allows the choice of various settings available on the ADS8681W in an iterative fashion until the best settings for the corresponding test scenario are discovered.

The final option in this pane is the selection for the *Update Mode*. The default value is *Immediate*, which indicates that the interface settings selection is applied to configure both the host and the ADS8681W instantly. The *Manual* option indicates that the selection is made only when the final choices are decided upon and the user is ready to configure the device. This is described in more detail in the following section.

The GUI is switched between hardware mode and simulation mode by checking and unchecking the *Connected to Hardware* box in the top right area at any time.

### *4.1.2 Register Map Configuration Tool*

The register map configuration tool allows viewing and modification all of the registers of the ADS8681W. This is selected by clicking on the *Register Map Config* radio button at the *Pages* section of the left pane as indicated in Figure 4-4.

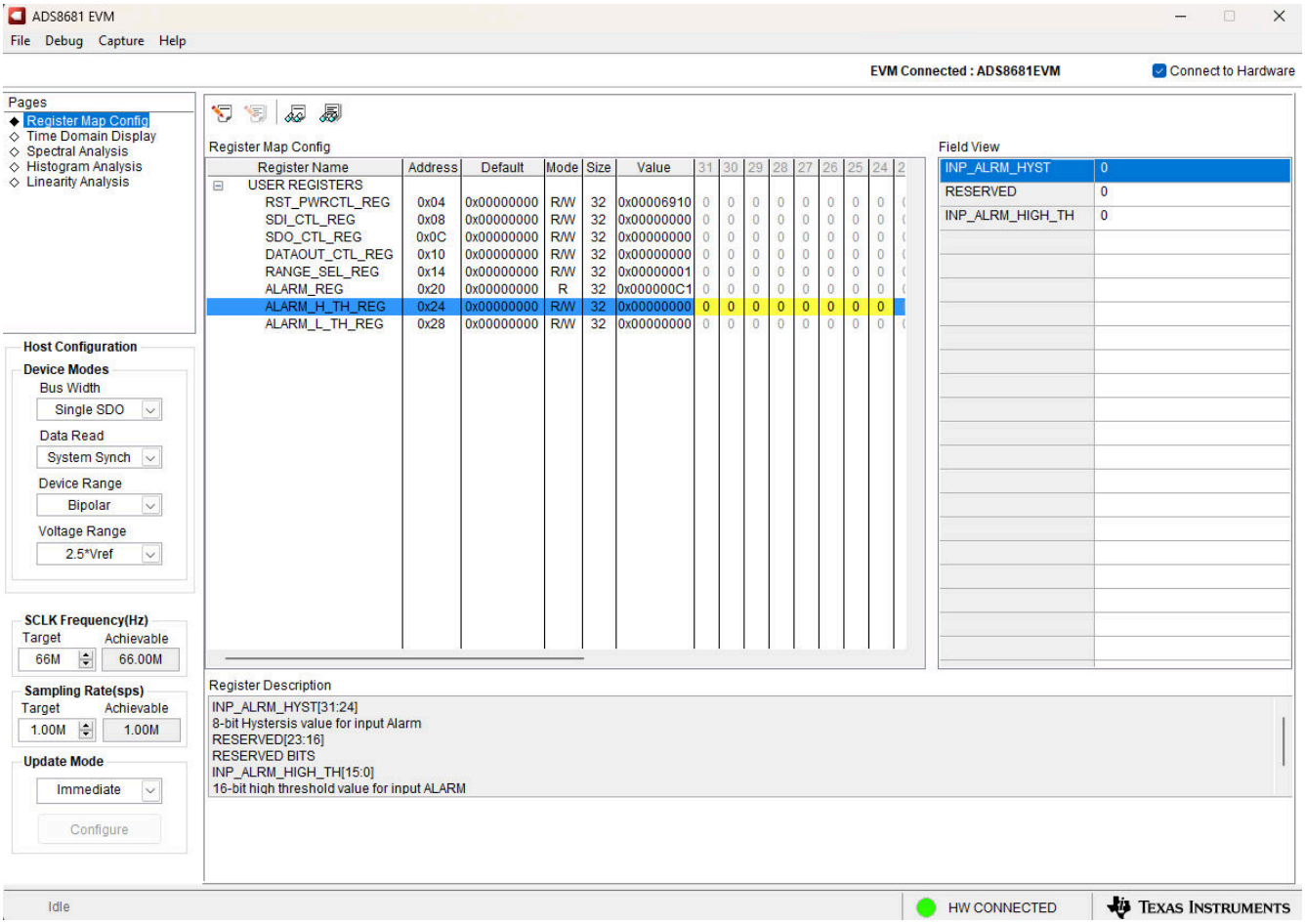



**Figure 4-4. Register Map Configuration**

On power up and initialization, the values on this page correspond to the reset values of the device registers. The register values are changed by single-clicking the corresponding bit field of the registers. If interface mode settings are affected by the change in register values, this change reflects on the left pane immediately. The impact of changes in the register value reflects on the ADS8681W device on the ADS8681WEVM-PDK based on the *Update Mode* selection as described in Section 4.1.1.

### *4.1.3 Time Domain Display Tool*

The *Time Domain Display* tool allows visualization of the ADS8681W's response to a given input signal. This tool is useful for both studying the behavior and debugging any problems with the ADC or drive circuits.

The user can trigger a capture of the data of the selected number of samples from the ADS8681W, as per the current interface mode settings using the capture button as indicated on Figure 4-5. The sample indices are on the X-axis and there are two Y-axes showing the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage, the selected *Device Range* and *Voltage Range*. The measured maximum and minimum code and equivalent voltage are also shown in the bottom right pane.

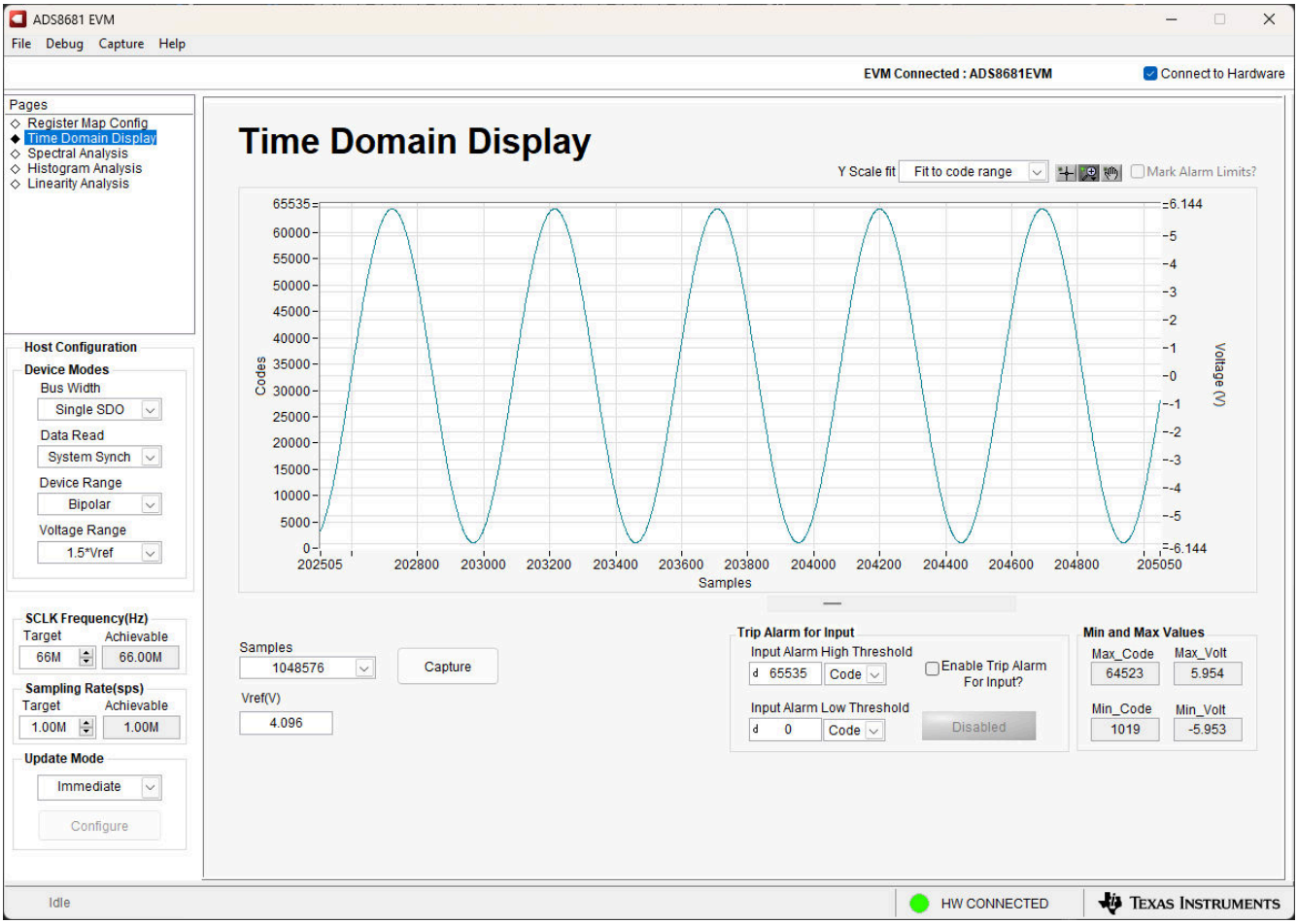



**Figure 4-5. Time Domain Display Tool**

### 4.1.4 Histogram Tool

Noise degrades ADC resolution and the histogram tool is used to estimate *Effective Resolution*, which is an indicator of the number of bits of ADC resolution lost due to noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC is reflected in the standard deviation of the ADC's output code histogram, obtained by performing multiple conversions of a DC input applied to a given channel.

The histogram analysis corresponding to a DC input is displayed by selecting *Histogram Analysis* on *Pages* and clicking on the *Capture* button as shown in Figure 4-6. The *Analysis* results include *Mean*, *Sigma*, *Min Code*, *Max Code*, and *Code* spread.

The X Scale of *Histogram Analysis* results are changed by selecting *Auto mode* or the default *Fit to code* range in the top right area, which is similar as the Y scale fit in the *Time Domain Display* tool.

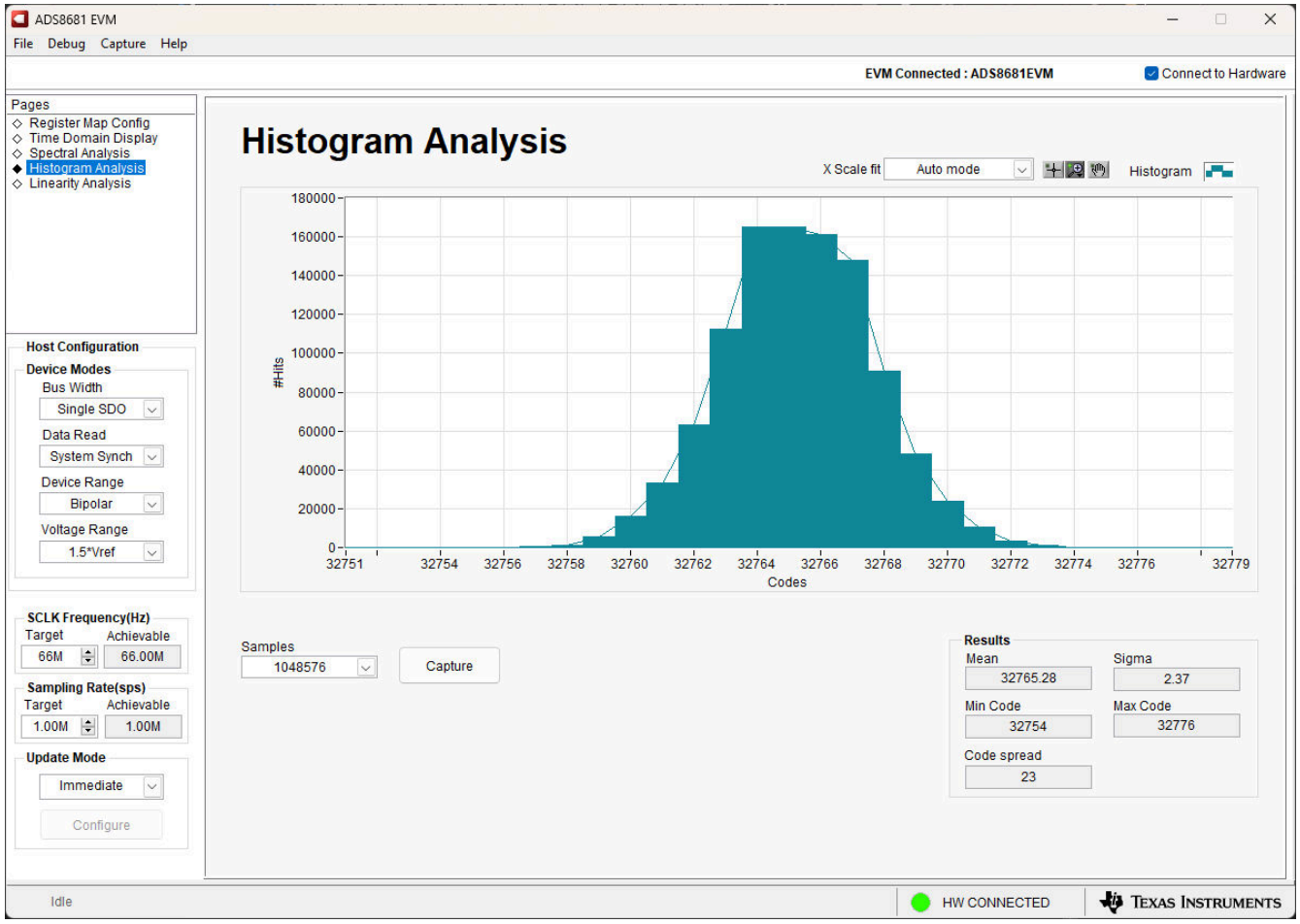



**Figure 4-6. Histogram Analysis Tool**

### 4.1.5 Spectral Analysis Tool

The spectral analysis tool is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS8681W SAR ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting.

The spectral analysis corresponding to a 1kHz sinusoidal signal and 1Msps sampling rate is displayed on clicking the *Capture* button as shown in Figure 4-7.

The expected ADC input is a sinusoidal signal of peak-to-peak amplitude close to the ADC's full-scale input range (FSR). The RMS power of the input signal normalized to FSR is shown in the *Signal Power (dBFS)* field and is about –0.5 dBFS (or about 95% × FSR) to avoid the input clipping.

The sampling rate of the ADC is adjusted by modifying the target sampling rate (sps) argument which is a global setting (it affects all tools). The achievable ADC sampling rate can differ from the target value depending on the applied SCLK frequency and PHI PLL settings. Note that the user is also required to specify a target SCLK frequency which the tool tries to match as exactly as possible by iteratively changing the PHI PLL settings until convergence.

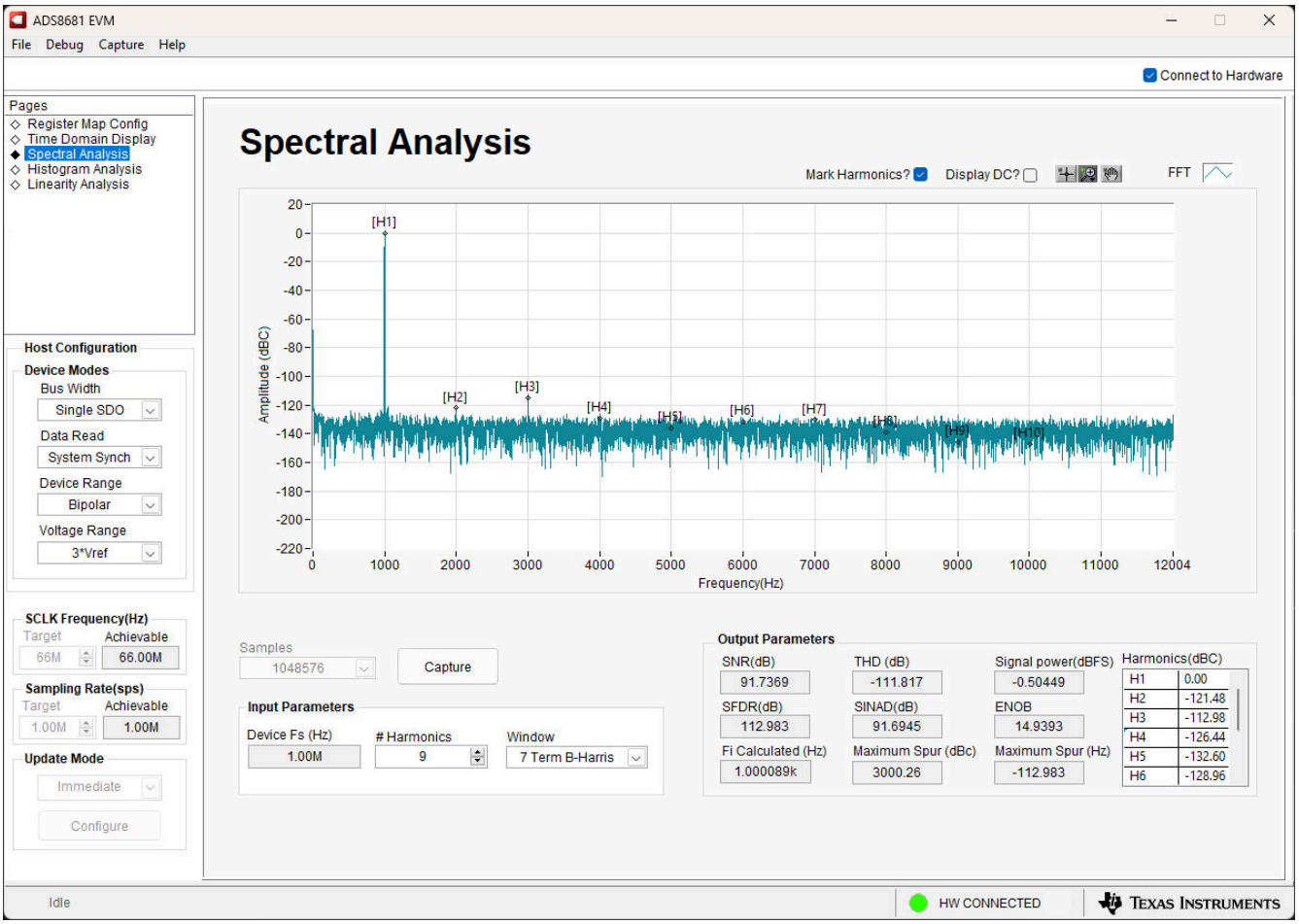



**Figure 4-7. Spectral Analysis Tool**

Finally, the *FFT* tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The *7-Term Blackman Harris* window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. Note that the *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

### 4.1.6 Linearity Analysis Tool

The linearity analysis tool measures and generates the DNL and INL plots over code for the specific ADS8681W installed in the evaluation board. A 1kHz sinusoidal input signal with very low distortion is applied for linearity analysis, which is slightly saturated and verifies there is no damage to the ADC, as shown in shown in Figure 4-8. The external source linearity to be better than the ADC linearity is critical. This is important to make sure that the measured system performance reflects the linearity errors of the ADC and is not limited by the performance of the signal source.

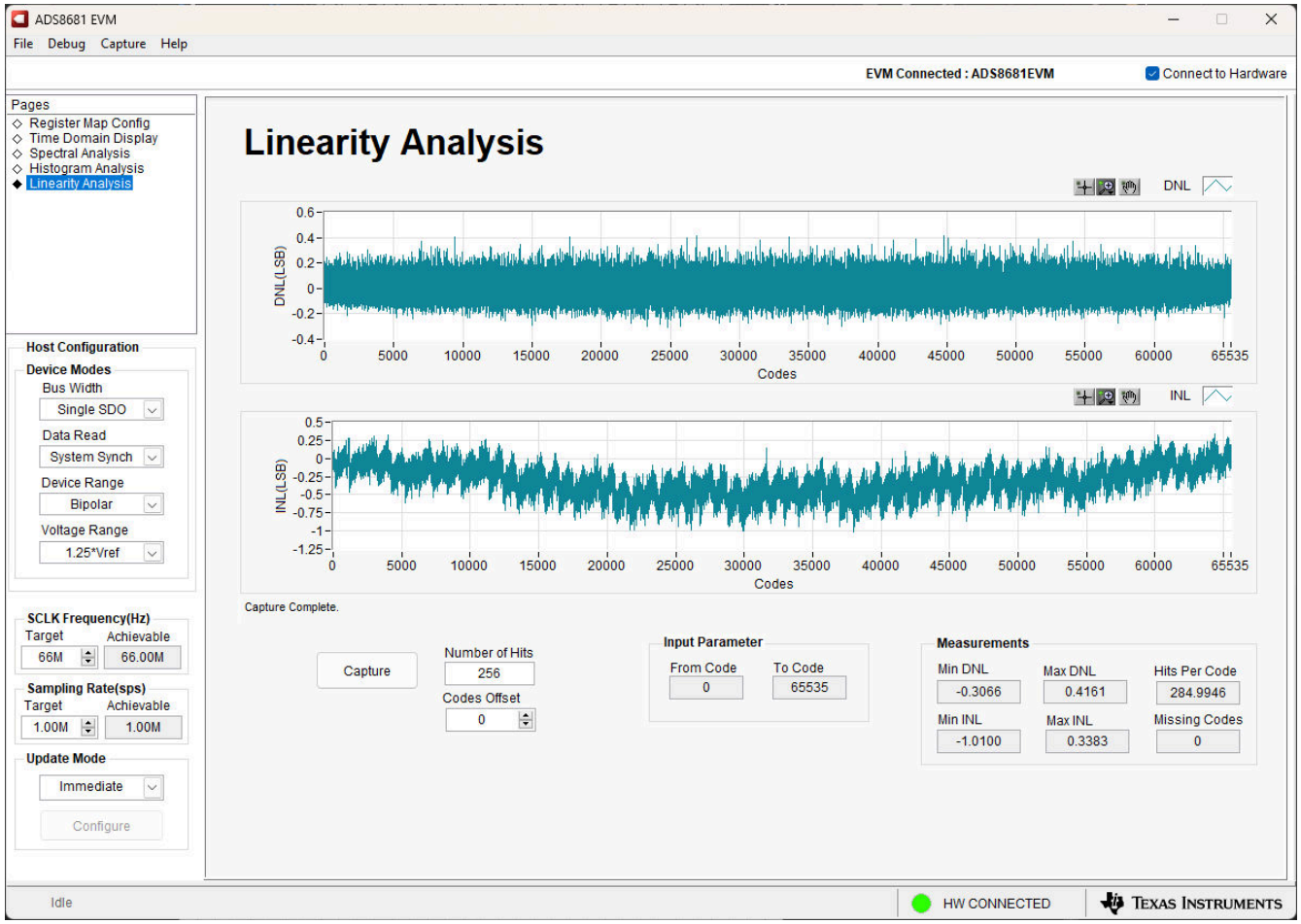



**Figure 4-8. Linearity Analysis Tool**

# 5 Hardware Design Files

## 5.1 ADS8681WEVM-PDK Schematic

The EVM schematic is shown in Figure 5-1.

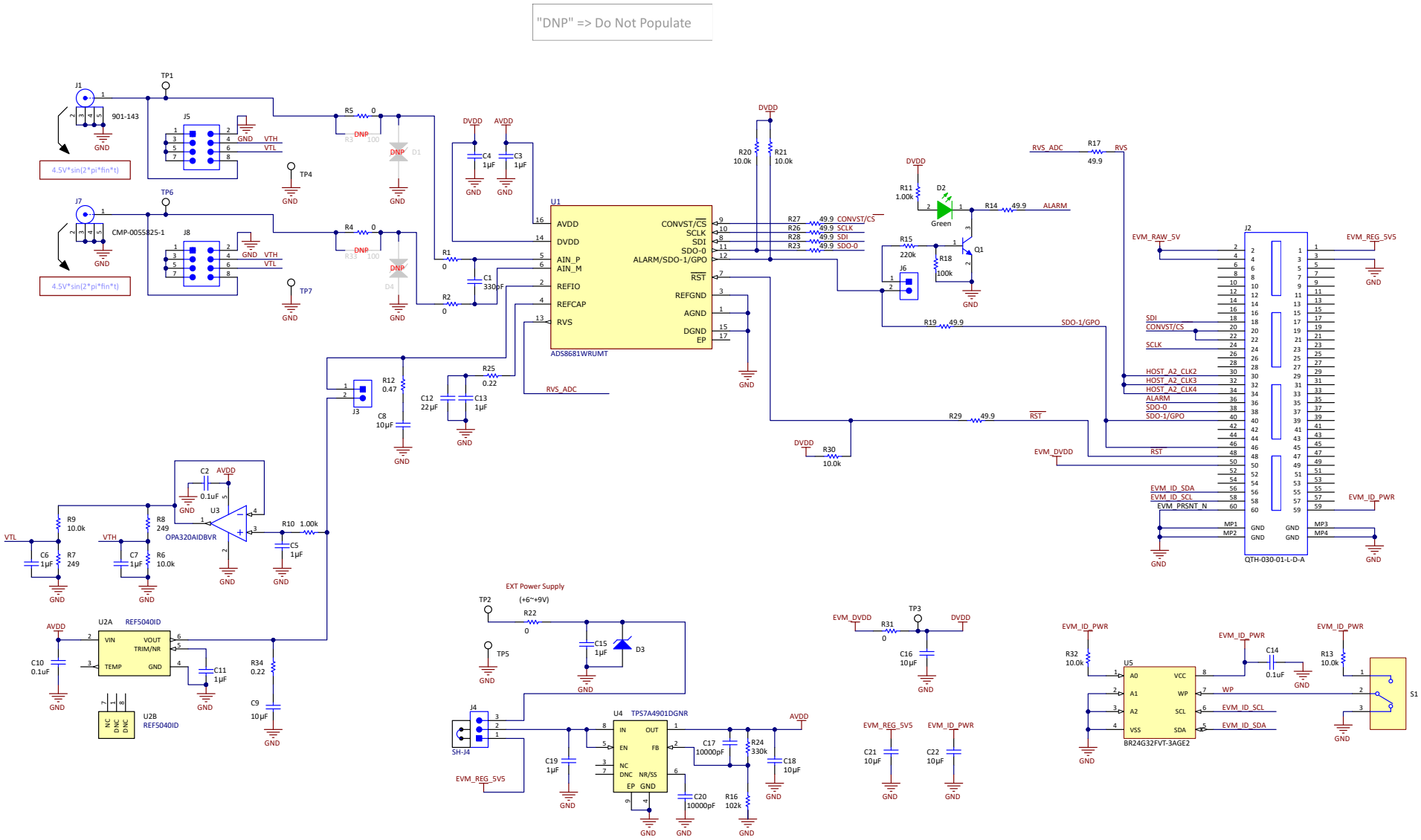



**Figure 5-1. Schematic Diagram of ADS8681WEVM**

## 5.2 PCB Layout

The EVM PCB layouts are illustrated in Figure 5-2 through Figure 5-5.

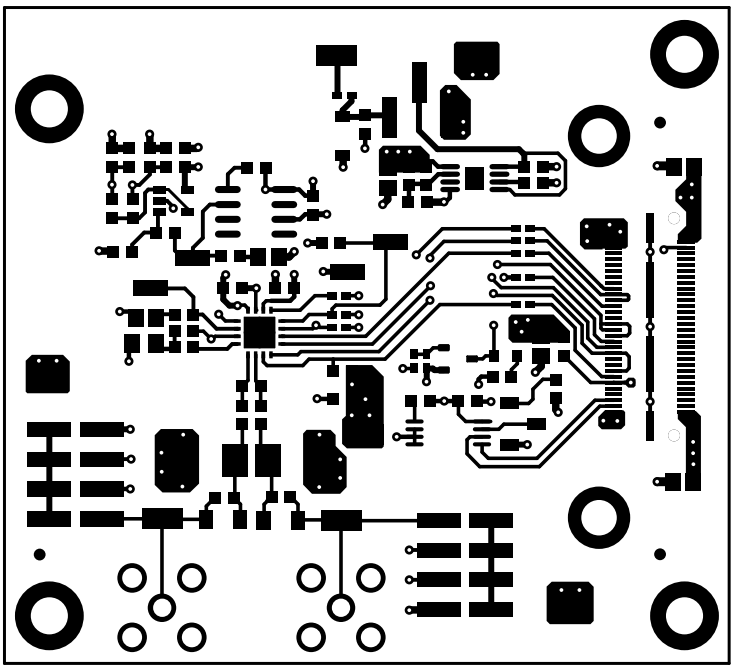


**Figure 5-2. ADS8681WEVM PCB Layer 1 – Top Layer**

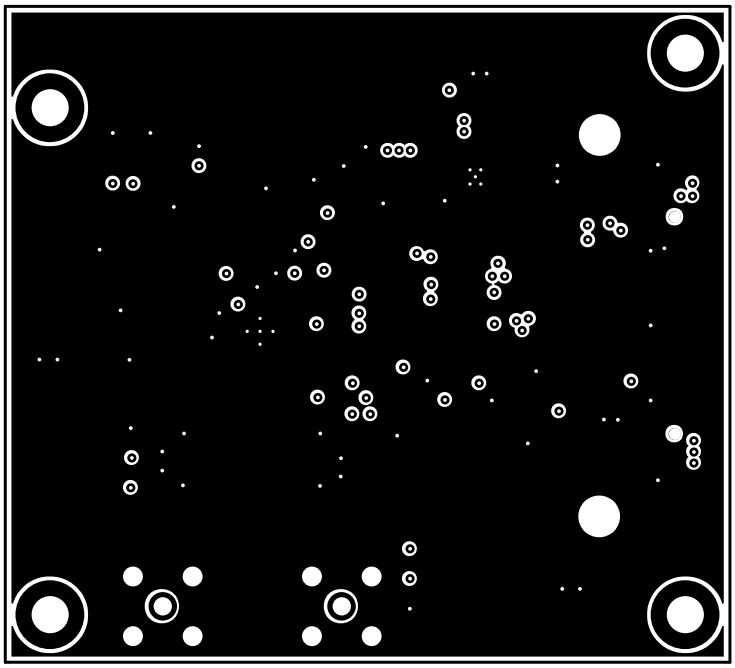


**Figure 5-3. ADS8681WEVM PCB Layer 2 – GND Plane**

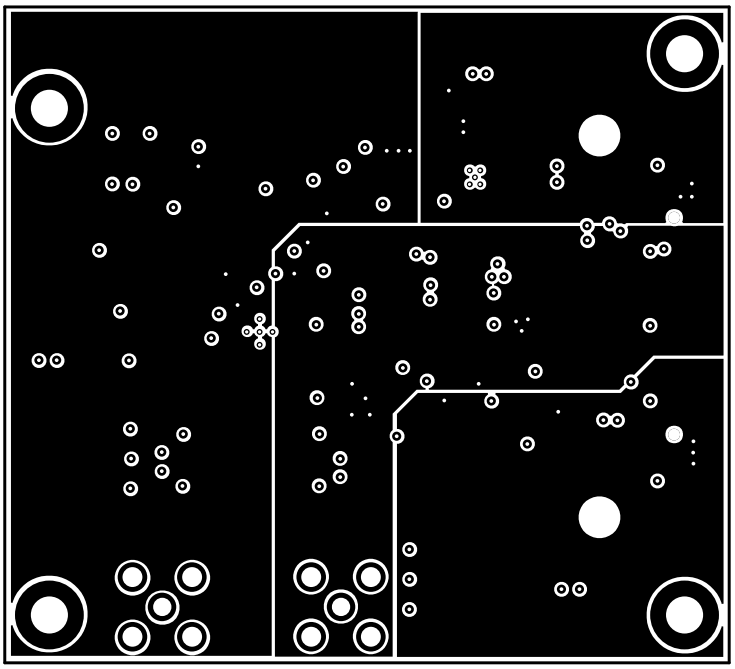


**Figure 5-4. ADS8681WEVM PCB Layer 3 – Power Planes**

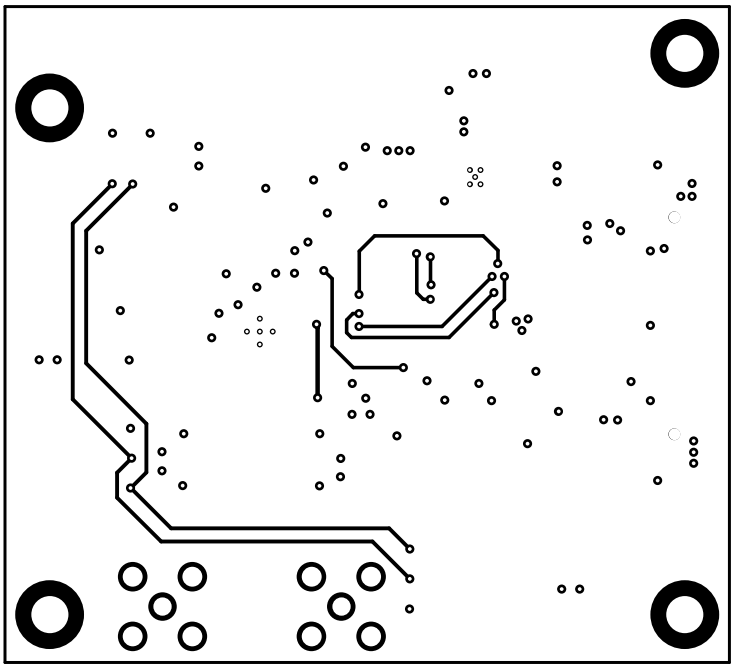


**Figure 5-5. ADS8681WEVM PCB Layer 4 – Bottom Layer**

## 5.3 Bill of Materials

The EVM BOM is listed in Table 5-1.

**Table 5-1. ADS8681WEVM Bill of Materials**

| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
|---|---|---|---|---|---|---|
| @H1, @H2, @H3, @H4 | 4 | | Hex Standoff, #4-40, Aluminum, 1/4" | 1/4" Aluminum Hex Standoff | 1891 | Keystone |
| @H5, @H6 | 2 | | MACHINE SCREW PAN PHILLIPS M2 | | MPMS 002 0005 PH | B&F Fastener Supply |
| C1 | 1 | 330pF | CAP, CERM, 330pF, 100V, +/- 5%, C0G/NP0, 0603 | 0603 | C1608C0G2A331J | TDK |
| C2, C10, C14 | 3 | 0.1uF | CAP, CERM, 0.1µF, 50V, +/- 10%, X7R, 0603 | 0603 | C0603C104K5RACTU | Kemet |
| C3, C4, C5, C6, C7, C11, C13, C15, C19 | 9 | 1uF | CAP, CERM, 1µF, 16V, +/- 10%, X7R, 0603 | 0603 | C1608X7R1C105K | TDK |
| C8, C9, C16, C18, C21, C22 | 6 | 10uF | CAP, CERM, 10µF, 25V, +/- 10%, X5R, 0805 | 0805 | CL21A106KAFN3NE | Samsung Electro-Mechanics |
| C12 | 1 | 22uF | CAP, CERM, 22µF, 16V, +/- 20%, X5R, 0805 | 0805 | GRM21BR61C226ME44 | MuRata |
| C17, C20 | 2 | 10000pF | CAP, 10000pF, 0603, 5%, 50V, C0G | 0603 | C1608C0G1H103J080AA | TDK |
| D2 | 1 | Green | LED, Green, SMD | 2x1.4mm | LG M67K-G1J2-24-Z | OSRAM |
| D3 | 1 | 9.1V | Diode, Zener, 9.1V, 500mW, SOD-123 | SOD-123 | MMSZ4696T1G | ON Semiconductor |
| FID1, FID2, FID3 | 3 | | Fiducial mark. There is nothing to buy or mount. | N/A | N/A | N/A |
| H1, H2, H3, H4 | 4 | | MACHINE SCREW PAN PHILLIPS 4-40 | Machine Screw, 4-40, 1/4" | PMSSS 440 0025 PH | B&F Fastener Supply |
| H5, H6 | 2 | | ROUND STANDOFF M2 STEEL 5MM | ROUND STANDOFF M2 STEEL 5MM | 9774050243R | Wurth Elektronik |
| H7 | 1 | | CABLE USB A MALE-B MICRO MALE 1M (Kit Item) | USB Cable | 102-1092-BL-00100 | CNC Tech |
| J1 | 1 | | Connector, TH, Right Angle SMA 50 ohm | SMA | 901-143 | Amphenol RF |
| J2 | 1 | | Header(Shrouded), 19.7mil, 30x2, Gold, SMT | Header (Shrouded), 19.7mil, 30x2, SMT | QTH-030-01-L-D-A | Samtec |
| J3, J6 | 2 | | Header, 2.54mm, 2x1, Gold, R/A, SMT | Header, 2.54mm, 2x1, R/A, SMT | 87898-0204 | Molex |
| J4 | 1 | | Header, 100mil, 3x1, Gold, SMT | Samtec_TSM-103-01-X-SV | TSM-103-01-L-SV | Samtec |

**Table 5-1. ADS8681WEVM Bill of Materials (continued)**

| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
|---|---|---|---|---|---|---|
| J5 | 1 | | Header, 100mil, 4x2, Gold, SMT | Header, 100mil, 4x2, SMT | 15910080 | Molex |
| J7 | 1 | | Connector, Right Angle SMA 50 ohm, TH | SMA | 901-143 | Amphenol RF |
| J8 | 1 | | Header, 100mil, 4x2, Gold, SMT | Header, 100mil, 4x2, SMT | 15910080 | Molex |
| Q1 | 1 | 45V | Transistor, NPN, 45V, 0.1A, SOT-23 | SOT-23 | BC847CLT1G | ON Semiconductor |
| R1, R2, R4, R5, R31 | 5 | 0 | RES, 0, 5%, 0.1 W, 0603 | 0603 | CRCW06030000Z0EA | Vishay-Dale |
| R6, R9, R13, R20, R21, R30, R32 | 7 | 10.0k | RES, 10.0 k, 1%, 0.1 W, 0603 | 0603 | RC0603FR-0710KL | Yageo America |
| R7, R8 | 2 | 249 | RES, 249, 1%, 0.1 W, 0603 | 0603 | RC0603FR-07249RL | Yageo America |
| R10, R11 | 2 | 1.00k | RES, 1.00 k, 0.1%, 0.1 W, 0603 | 0603 | RT0603BRD071KL | Yageo America |
| R12 | 1 | 0.47 | RES, 0.47, 1%, 0.1 W, 0603 | 0603 | ERJ-3RQFR47V | Panasonic |
| R14, R17, R19, R23, R26, R27, R28, R29 | 8 | 49.9 | RES, 49.9, 1%, 0.063 W, 0402 | 0402 | CRCW040249R9FKED | Vishay-Dale |
| R15 | 1 | 220k | RES, 220 k, 5%, 0.063 W, 0402 | 0402 | CRCW0402220KJNED | Vishay-Dale |
| R16 | 1 | 102k | RES, 102 k, 0.1%, 0.1 W, 0603 | 0603 | RG1608P-1023-B-T5 | Susumu Co Ltd |
| R18 | 1 | 100k | RES, 100 k, 1%, 0.063 W, 0402 | 0402 | CRCW0402100KFKED | Vishay-Dale |
| R22 | 1 | 0 | RES, 0, 5%, 0.063 W, 0402 | 0402 | RC0402JR-070RL | Yageo America |
| R24 | 1 | 330k | RES, 330 k, 0.1%, 0.1 W, 0603 | 0603 | RG1608P-334-B-T5 | Susumu Co Ltd |
| R25, R34 | 2 | 0.22 | RES, 0.22, 1%, 0.1 W, 0603 | 0603 | ERJ-3RQFR22V | Panasonic |
| S1 | 1 | | Switch, Slide, SPDT 100mA, SMT | Switch, 5.4x2.5x2.5mm | CAS-120TA | Copal Electronics |
| SH-J4 | 1 | | Shunt, 2.54mm, Gold, Black | Shunt, 2.54mm, Black | 60900213421 | Wurth Elektronik |
| TP1, TP2, TP3, TP4, TP5 | 5 | SMT | Test Point, Miniature, SMT | Testpoint_Keystone_Miniature | 5015 | Keystone |
| TP6, TP7 | 2 | | Test Point, Miniature, SMT | Testpoint_Keystone_Miniature | 5015 | Keystone Electronics |
| U1 | 1 | | 16-Bit, High-Speed, Single-Supply, SAR ADC Data Acquisition System With Programmable, Bipolar Input Ranges | WQFN16 | ADS8681WRUMT | Texas Instruments |

**Table 5-1. ADS8681WEVM Bill of Materials (continued)**

| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
|---|---|---|---|---|---|---|
| U2 | 1 | | Low Noise, Very Low Drift, Precision Voltage Reference, -40 to 125 degC, 8-pin SOIC (D), Green (RoHS & no Sb/Br) | D0008A | REF5040ID | Texas Instruments |
| U3 | 1 | | Precision, 20MHz, 0.9pA Ib, RRIO, CMOS Operational Amplifier, 1.8 to 5.5V, -40 to 125 degC, 5-pin SOT23 (DBV0005A), Green (RoHS and no Sb/Br) | DBV0005A | OPA320AIDBVR | Texas Instruments |
| U4 | 1 | | Single Output High PSRR LDO, 150mA, Adjustable 1.2 to 33V Output, 3 to 36V Input, with Ultra-Low Noise, 8-pin MSOP (DGN), -40 to 125 degC, Green (RoHS & no Sb/Br) | DGN0008D | TPS7A4901DGNR | Texas Instruments |
| U5 | 1 | | I2C BUS EEPROM (2-Wire), TSSOP-B8 | TSSOP-8 | BR24G32FVT-3AGE2 | Rohm |
| D1, D4 | 0 | 36V | Diode, TVS, Bi, 36V, 64.3Vc, SMB | SMB | SM6T36CA | STMicroelectronics |
| R3, R33 | 0 | 100 | RES, 100, 1%, 0.4 W, AEC-Q200 Grade 0, 1.4x3.6mm | 1.4x3.6mm | MMA02040C1000FB300 | Vishay/Beyschlag |

# 6 Additional Information

## 6.1 Trademarks

SPI™ is a trademark of Motorola Mobility LLC.
multiSPI™ is a trademark of Texas Instruments.
Microsoft® and Windows® are registered trademarks of Microsoft Corporation.
All trademarks are the property of their respective owners.

# 7 Related Documentation

The following related documents are available through the Texas Instruments website at www.ti.com.

**Related Documentation**

| Device | Literature Number |
|---|---|
| ADS8681W | SBASAY5 |
| OPA320 | SBOS513 |
| REF5040 | SBOS410 |
| TPS7A4901 | SBVS121 |

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265