

1 Evaluation Module Overview

1.1 Introduction

The ADC3910D125EVM allows for evaluation of all ADC39XX versions as the versions are all P2P compatible. By default, the ADC3910D125EVM, has the ADC3910D125 (10-bit, 125MSPS). The EVM is configured to receive external single-ended analog inputs as the EVM includes baluns for single-ended to differential conversion. The sample clock is also sourced externally and is single-ended LVCMOS.

To capture data from the ADC3910D125EVM, the EVM is connected to a TSW1418EVM through an FMC connector. The TSW1418EVM has an AMD Atrix-7 FPGA to capture the ADC3910D125EVM output. The ADC data, captured by the FPGA, is then transferred to the PC and displayed in HSDC Pro.

1.2 Kit Contents

Table 1-1. ADC3910D125EVM Kit Contents

Item	Description	Quantity
ADC3910D125EVM	PCB	1
FTDI board	PCB	1
Mini USB cable		1
EVM barrel power cable		1

1.3 Specification

The specifications for ADC3910D125 are available in the data sheet ([SBASAD1](#)).

1.4 Device Information

The detailed device information is available in the data sheet ([SBASAD1](#)).

2 Hardware

2.1 Board Overview

This section details the required tools, both hardware and software, needed to effectively use the ADC3910D125EVM.

- The following image highlights the key aspects of the ADC3910D125EVM.

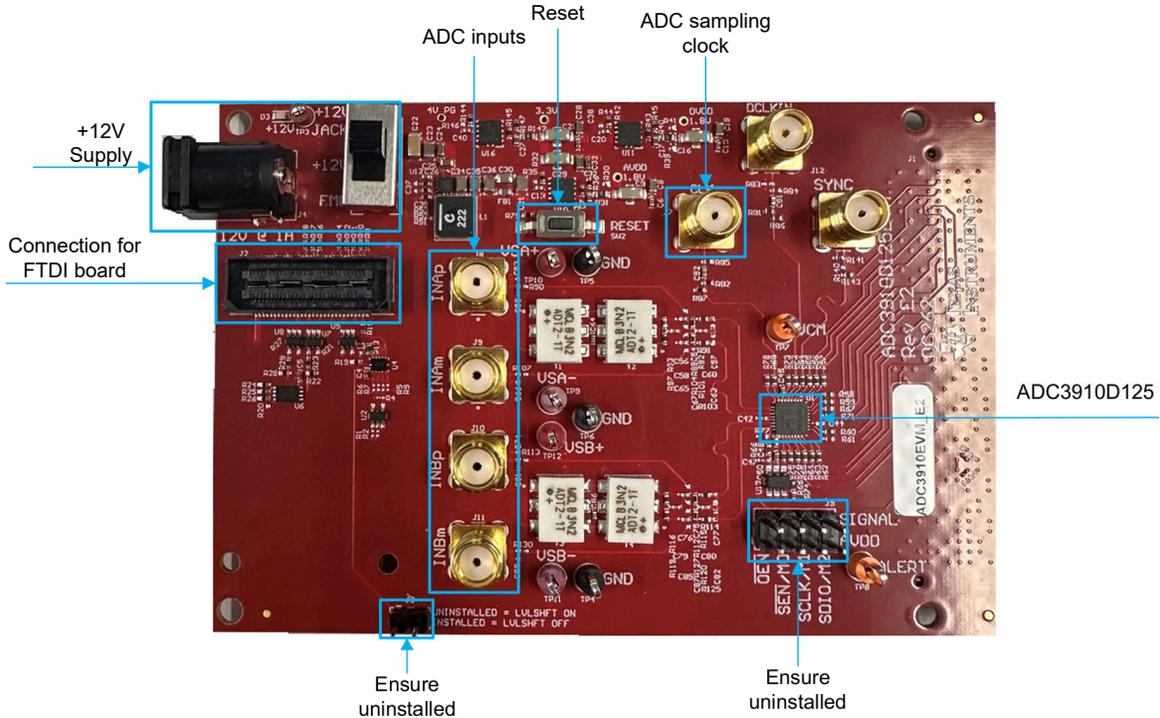


Figure 2-1. ADC3910D125EVM Feature Identification

- Make sure that SW1 is set to take power from the +12V jack, the included FTDI board is connected to J2, and jumpers J3 & J5 remain uninstalled.

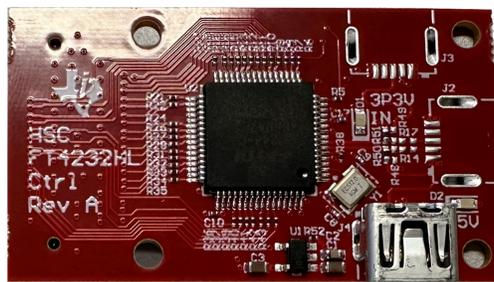


Figure 2-2. FTDI board Included with ADC3910D125EVM That Connects to J2

2.2 Required Equipment

- The following equipment is included in the EVM kit:
 - ADC3910D125EVM
 - FTDI board
 - Mini USB cable
 - Barrel power cable
- The following equipment is not included with the EVM kit, but is required for proper evaluation.
 - TSW1418EVM for capturing the data from the ADC3910D125
 - [HSDC Pro](#)
 - [Python \(3.10.9\)](#)
 - [Vivado Lab Solutions \(2023.2\)](#)
 - Visual Studio Code (VS Code) or preferred IDE
 - At least two, low-noise, signal generators for to provide the ADC sampling clock and an analog input. TI recommends either of the following signal generators:
 - Rohde & Schwarz SMA100A
 - Rohde & Schwarz SMA100B
 - Bandpass filters for the sample clock and the analog inputs. The filters has a narrow passband within 5%-15% of the desired bandwidth and minimal insertion loss.
 - SMA cables for signal connections.

2.3 Hardware Setup

1. Connect the ADC3910D125EVM to the TSW1418EVM through the FMC connector.
2. Connect the FTDI board to the ADC3910D125EVM onto J2 of the ADC3910D125EVM.
3. Install the JTAG dongle provided with the TSW1418EVM onto J3 of the TSW1418EVM.
4. Make sure J13 on TSW1418EVM is between pin two and three.
5. Connect a +12V power supply to the barrel connector (power supply cable included with EVM) of the ADC3910D125EVM.
6. Connect a mini USB cable from the PC to the FTDI board installed on the ADC3910D125EVM.
7. Connect a mini USB cable from the PC to J2 on the TSW1418EVM.
8. Connect a micro USB cable from the PC to the JTAG dongle (on the TSW1418EVM) that was installed in step three.
9. Connect a bandpass filtered clock signal source to J7 labeled CLK of the ADC3910D125EVM.
10. Connect a bandpass filtered analog input source to J8 and/or J10 of the ADC3910D125EVM labeled INAp and INBp, respectively.

If all the steps above were followed correctly, then the final setup looks like the following:



Figure 2-3. Final Setup of ADC3910D125EVM

3 Software

3.1 Software Setup

1. Download and install the latest version of [HSDC Pro](#).
2. Download and install [Python \(3.10.9\)](#).
3. Install [Vivado Lab Solutions \(2023.2\)](#).
4. Download and install [VS Code](#) and install the [Python extension](#) by Microsoft®.
5. Download the ADC3910D125EVM_API_Rev0.1 supplemental software folder found in the ADC3910D125EVM product folder or provided by TI.

4 Implementation Results

4.1 Evaluation Setup

Once the software setup and hardware setups are completed. Follow these steps to get a capture on the ADC3910D125EVM:

1. Connect a bandpass filtered 125 MHz clock signal to the ADC.
2. Connected a bandpass filtered 10.097503662MHz input signal to either ADC input.
3. Launch a PowerShell terminal and change current directory to the location of the ADC3910D125EVM_API_Rev0.1. From within the ADC3910D125EVM_API_Rev0.1 folder, run the following command: `pip install -r requirements.txt`.
 - a. This installs the required python packages to run the provided software files.
4. Launch the `tcl_client.tcl` file, found in the ADC3910D125EVM_API_Rev0.1 folder, in a text editor and update the path in line six to your path.

```
write_hw_ila_data -csv_file -force {YOUR PATH HERE/ADC3910D125EVM_API_Rev0.1/OutputCaptures/iladata.csv} $ila_data_buffer
```

Figure 4-1. Path that needs to be edited in "tcl_client.tcl"

5. Launch and run ADC3910D125EVM_API_Rev0.1.py file provided in the software suite.
 - a. By default, this file is setup to provide a hardware and software reset to the ADC.
 - b. The ADC is placed in the default dual-channel, 10-bit, low latency, DDR interface mode.
 - c. R67 can be probed to confirm that DCLK is active.
6. Launch Vivado Lab 2023.2:
 - a. Click on *Open Hardware Manager*.
 - b. Click on *Open target* at the top with the green background.
 - c. Click on *Auto Connect* from the pop up menu.
 - i. This connects to the xc7a100t_0 FPGA.
 - d. Right-click xc7a100t_0, then select *Program Device* in the pop-up menu.

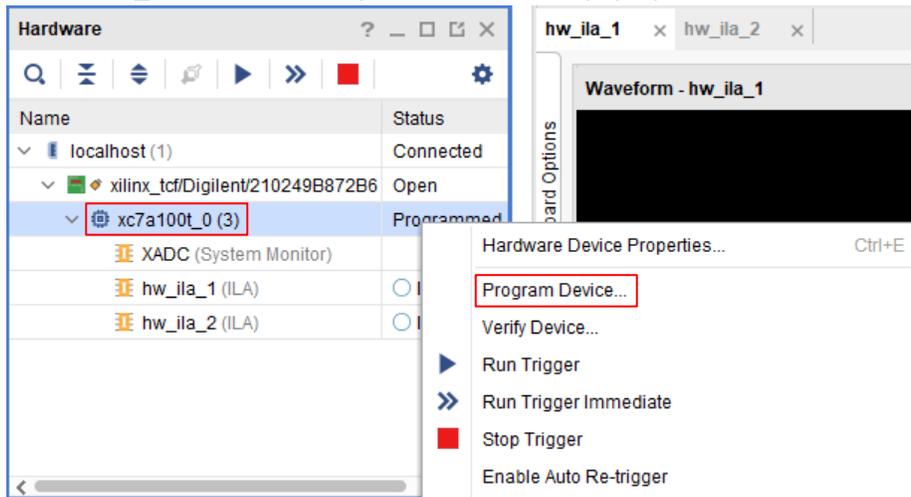


Figure 4-2. Programming FPGA Menu

- e. In the pop up menu click on ... on the *Bitstream file* row and navigate to the bitfiles folder in the ADC3910D125EVM_API_Rev0.1 folder. Select the *10b_DDR.bit* file.

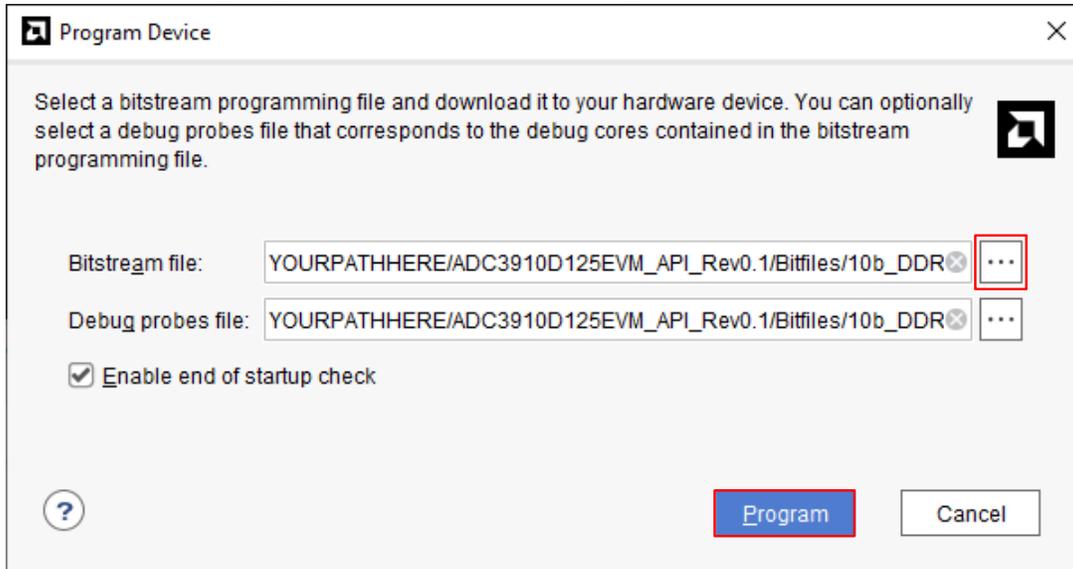


Figure 4-3. Bitfiles to Program FPGA

- f. Click on *Program*
 - i. There is a new window now called *hw_ila_1*.
- g. In the *hw_ila_1* waveform view, select all the values and right click. In the pop-up menu, hover over *Radix* and in the next pop-up menu, select *Signed Decimal*.

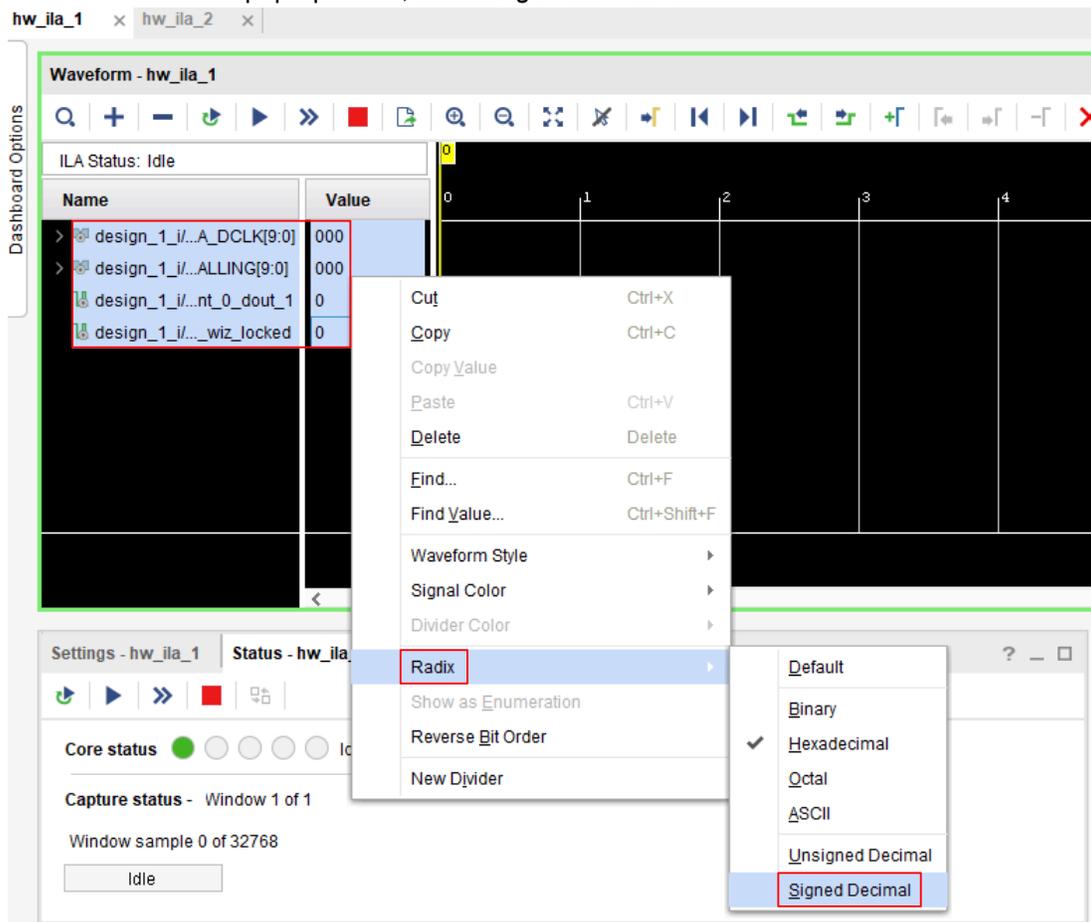


Figure 4-4. Changing ILA radix to signed decimal

- h. In the *Tcl Console* command line, change the current directory to the location of the ADC3910D125EVM_API_Rev0.1 folder.

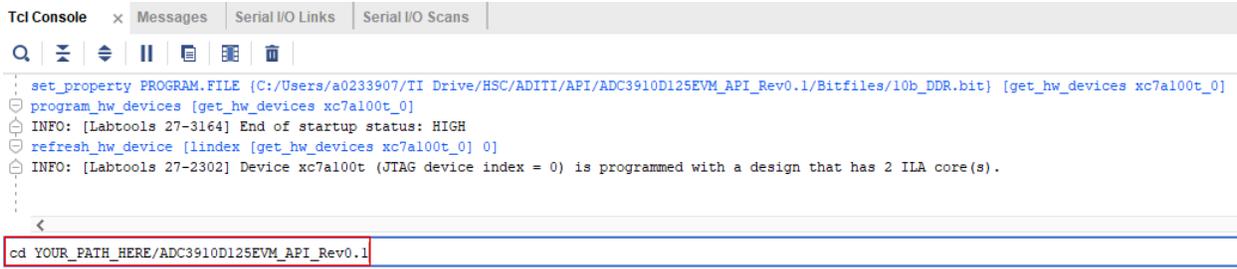


Figure 4-5. Change Current Directory in Vivado Lab 2023.2

- a. Launch and run `py_server.py` from ADC3910D125EVM_API_Rev0.1 folder.
 - i. After the running the file, *STARTING THE SERVER....* is printed by the python terminal.
- b. Launch HSDC Pro, click *OK* in the first pop-up menu and click *OK* again in the next pop-up window.
- c. In Vivado™ Lab 2023.2 in the *Tcl Console* type the following command: `source ./tcl_client.tcl`
- d. Now, the `py_server.py` python terminal shows *Input a command*.
 - i. The available commands are *Capture* and *Quit*.
- e. In the `py_server.py` python terminal, type *Capture* (this is case sensitive).
- f. In HSDC Pro, an FFT of the input signals needs to be captured.

4.2 EVM Capture

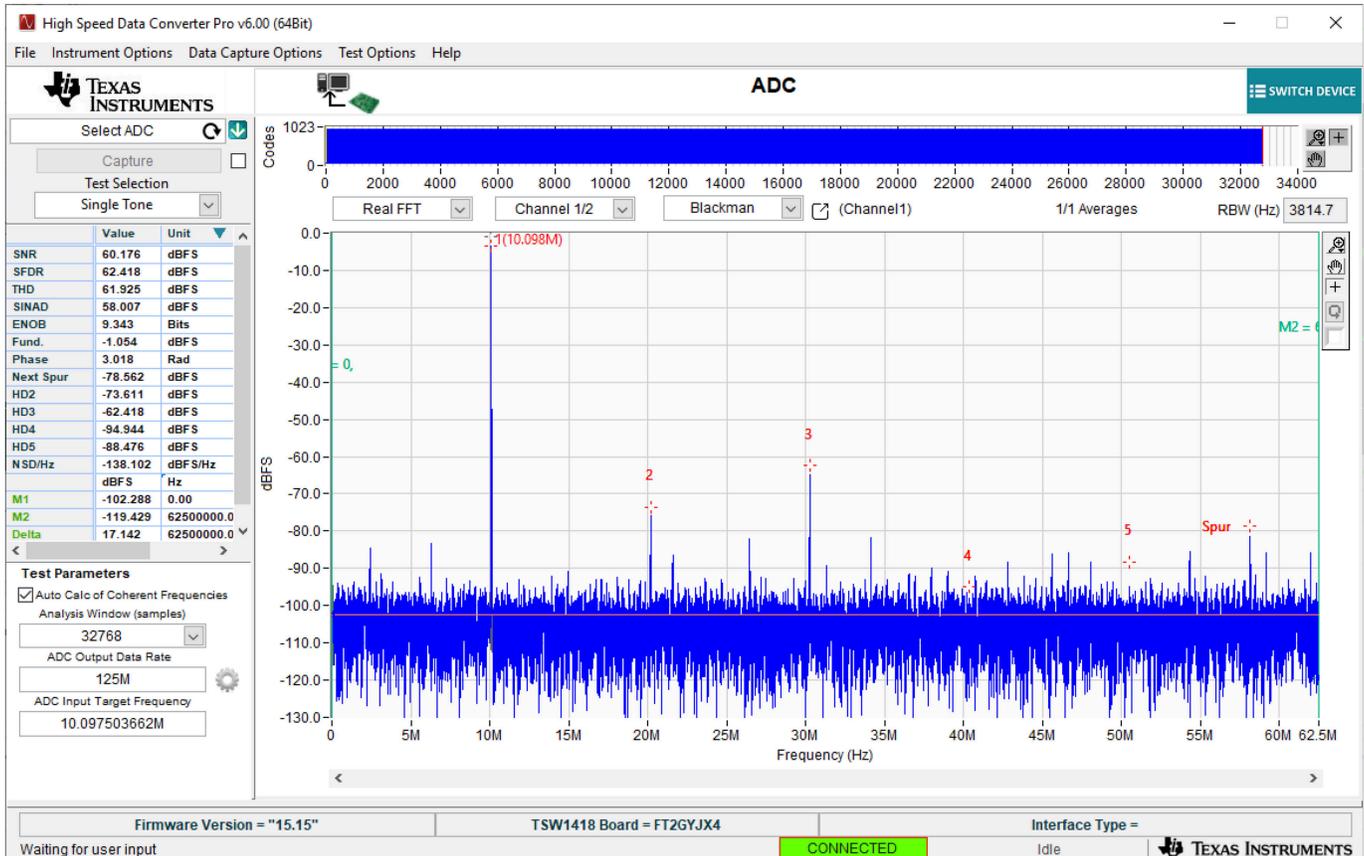


Figure 4-6. FS = 125MSPS; Fin = 10.097503662M @ 8.2dBm

5 Hardware Design Files

5.1 Schematics

The schematics are available on the product page of [ADC3910D125EVM](#).

5.2 PCB Layouts

The board layout is available on the product page of [ADC3910D125EVM](#).

5.3 Bill of Materials (BOM)

The bill of materials is available on the product page of [ADC3910D125EVM](#).

6 Additional Information

6.1 Trademarks

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7 References

- [TSW1418 Evaluation Module User's Guide \(Rev. A\)](#)
- [High-Speed Data Converter Pro GUI User's Guide \(Rev. E\)](#)

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CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

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(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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