User's Guide **Programming AFE7769D to Interface with RNS802 for 2T2R**



ABSTRACT

This user's guide provides a walkthrough of hardware and software setup with supplemental images as a visual representation, followed by bringup steps.

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1 Introduction

This guide is intended to be used in conjunction with the document ID PC-004159-DC version 3 from RANsemi.

This user's guide introduces a small cell application using Texas Instruments' AFE7769D evaluation module (EVM) in collaboration with RANsemi, a semiconductor company that provides industry-standard systems on chips (SoCs) for small cell wireless infrastructure. This reference solution serves to help customers ramp system integration of the analog front-end (AFE), and allows for seamless interfacing with the RANsemi RNS802 SoC.

The AFE7769D is a 4T4R2F RF transceiver with integrated Digital Pre-Distortion (DPD) that serves to linearize power amplifiers (PAs) for improved wireless coverage to the end customer. The small cell 5-watt radio unit (RU) uses the EVM version of the device that connects with the RANsemi component of the solution for seamless interfacing. The RNS802 is a SoC that is designed for 5GNR/LTE small cell disaggregated and integrated RAN architectures, per RANsemi's website.

Note

In the following sections, the code includes text like Picocom and PC802, as RANsemi was previously a part of Picocom before RANsemi became an independent company in November 2023. The names of the files were updated, but the hardware and software remain unchanged.

2 Basic EVM Test Procedures

2.1 Safety

- Safety glasses must be worn.
- This test must be performed by qualified personnel trained in electronics theory and understand the risks and hazards of the assembly to be tested.
- ESD precautions must be followed while handling electronic assemblies while performing this test.
- Take precautions to avoid touching areas of the assembly that may get hot or present a shock hazard during testing.
- No ESD wrist strap shall be worn for Hi Voltage testing (≥50 Vrms or ≥75 VDC) use Ionizer.

2.2 Quality

Test data or reports are made available upon request by Texas Instruments.

2.3 Apparel

- Safety glasses
- Electrostatic smock
- Electrostatic gloves or finger cots
- Ground ESD wrist strap

2.4 Hardware and Software Requirements

2.4.1 Test Equipment Required

- DC power supply at 5.5V, 5A
- DC multimeter
- USB mini-B cable
- USB 3.0 cable
- PC with USB port
- Intel USB Blaster or USB Blaster II
- Signal generator
- 1:8 relay
- Spectrum analyzer
- BNC cables, splitter
- USB hub

2

TSW14J58 Rev A5



2.4.2 Software Required

AFE77xxD Latte v1.4 or later

3 AFE7769DEVM Setup

3.1 AFE7769D Hardware Changes

Make the following changes to the AFE7769DEVM to separate the SYNCOUT pins as shown in Figure 3-1.



Figure 3-1. Separating the SYNCOUT Pins

In conjunction to the schematic, see Table 3-1 for the list of switches to make.

AFE Reference Designator	Change From	Change To
R16	0Ω	DNI
R19	0Ω	DNI
R3	0Ω	DNI
R5	0Ω	DNI
R1	DNI	0Ω
R2	DNI	0Ω
R21	DNI	0Ω
R22	DNI	0Ω

Table 3-1. List of Pin Changes, AFE7769DEVM

3.2 AFE7769D Connections

- Connect the 5.5V power supply to power jack connector (J22) of the AFE7769DEVM.
 a. Check and make sure the D14 (POWER) LED lights up.
- 2. Connect the USB Type Mini-B Cable from PC to the USB port (J20) of the AFE7769DEVM.
 - a. Check and make sure the D13 (USB_PWR) LED lights up.
- 3. Connect the AFE7769DEVM to the RNS802 through the FMC connector.
- 4. Connect the 122.88MHz reference clock (SYNC_CLOCK) from the RNS802 (J1106) to the LMK_CLKIN (J19) of the AFE7769DEVM, as shown in Figure 3-2.





Figure 3-2. Hardware Setup and Connections AFE7769DEVM-RNS802

3.3 AFE7769D Software Setup

- 1. Install the AFE77xxD Latte GUI from zipped folder called "V1p4.zip" in the TI drive.
- 2. After installing the AFE77xxD GUI, copy the PC802_LMKDIV.py script and paste it under the following directory "...\Documents\Texas Instruments\AFE77xxDLatte\projects\AFE77xxD\AFE7769D".
- 3. Copy the "AFE77xxD_Picocom_pc802_K1L.xlsx" file and paste it under "\Documents\Texas Instruments\AFE77xxDLatte\lib\configs".

3.4 AFE7769D Programming Method 1: Automated

 Open the AFE77xxD Latte GUI version 1.4. Make sure the interface looks like Figure 3-3, then click Continue. The message "Couldn't Detect FPGA Reset FTDI. Please reset FPGA manually" is expected and can be ignored.

AFE77xxD	•
0x77D	•
None	+
EVM-1Device358	•
0×10	•
Basic	•
RS232-HS	
I. Please reset FPGA manually.	
	AFE/7XXD 0x77D None EVM-1Device358 0x10 Basic IS232:HS I. Please reset FPGA manually.

Figure 3-3. Launching AFE77xxD Latte Software



2. Wait until the GUI loads. Figure 3-4 shows the landing page.

AFE77xxD File Edit View Run Log Session He	p Latte Mode	- 0 X
■ AFETNOD File Eati View Run Log Session He Tree View User-Configuration > Installation > Installation > Trat > Status > PROA-Operations CAPI-Sequence-Generator	y Let Mode User Caulage Let user Caulage Mark Caulage Let user Caulage	
50 1.000 ± 00 ± 00 1.000 ± 000 ± 0000 ± 00 1.000 ± 000 ± 00 1.000 ± 000 1.000 ± 0000 ± 000 1.	Ø Commad ine Ø/Science Interior Commad limit MicS:0 =======# Interior Commad limit Ø/Science Interior Commad limit Interior Commad limit Interior Commad limit	
`		🜵 Texas Instruments
		MA 25'8

Figure 3-4. AFE77xxD Latte Landing Page

3. At the top, click on Latte Mode and navigate to Script Mode, as shown in Figure 3-5.

Đ	â Af	E77xxl	D							
ł	file	Edit	View	Run	Log	Session	Help	Latt	e Mode	
	Tree	View					_		GUI Mode	Ctrl+Shift+L
	licer-Guide								Script Mode	Ctrl+Shift+S
	~	AFE-Co	onfigura tializatio	ition n				Т		

Figure 3-5. Switching to Script Mode

4. Open the PC802_2T2R_Script.py script on the tree view on the left as shown in Figure 3-6.

Ed AFE//XXD		
<u>Eile Edit View Run Log S</u> ession	Help	Latte Mode
Scripts	Ð	1 #####Bloading Excel File######
Files		2 xJFfierr'C:/Users/DC-WI/Documents/Texas Instruments/AFE77xxDLattellb/configs/AFE77xxD_Picocom_pc802_KLL.xlsx' #This is the path to the excel configuration file to be loaded
× AFE77xxD		3 Ars.LoadyStemwaramssxcel(XIFLe) = Moading the parameters from the excel file
✓ AFE7769D		5 #####Setting LMK Params######
PC802_2T2R_Script.py		setupParams.lmklib.lmkParams.pllEn = True
PC802_LMKDIV.py		setuparams.imkib.imkparams.inputcik = 142.00
usefulFunctions.py		S ######Device Bringup######
> PC802_LMK	3	0 AFE.deviceBringup()
> picocom_031723		1 Million Setting LMK Divideration
		ink.nedu.page.sbil_config.trintbuvides.tilv_crkint_it_1sg_ = +
		setting TDD on
	1	5 AFE.TOP.overrideTdd(0,0,1)
	3	<pre>i6 #ChFE.overrideTdd(0,0,0,0,1)</pre>
		7 #####Sync Command#####
		o skun this command after you start sending data from the PC002

Figure 3-6. RNS802 Script

 Run the script by pressing F5 or by clicking Run > Buffer. An output in the log window like that shown in Figure 3-7 signals that the script was run with no errors. After running this script, the LMK_LOCKED LED (D11) turns on if the 122.88MHz reference from the RNS802 is connected.



AFE7769DEVM Setup

👪 AFE77xxD	12					- 🗆 ×
File Edit View	Run Log Session	Help L	atte Mode			
Scripts	Buffer	F5	.head.page.FLL1_Config.Clkin0_1_2_Divider.div_clkin0_lt_13_0_gt_ = 4			Instrument List 8
Files	Run Selection	F7	head.page.PLL1_Config.Clkin0_1_2_Divider.div_clkin1_lt_13_0_gt_ = 4			Device Source clk
✓ AFE77xxD	File	F8	head.page.PLL1_Config.N_Divider_PLL1.N_DIV_PLL1_lt_13_0_gt_ = 4			RF Source clk
✓ AFE7769D	Pause	E9				Signal Source
PC802_Lf	Stop	F10				
> PC802 LMK						Device List 8
> picocom_031	Create Server					CPLD
	Wait time for serve					IMK Clock Divider
	Main Thread time o	ut				
						Engine List
						HSCEngineWithILDDCDGC
						,
						Custom GUI List
						CGui_Custom_GUI
lee				-	Command Line	
ASE and a set of Car						
#=======	===== ERRORS:5, WA	RNINGS	0 ==============#		from globalDefs import *	
#	VD /AEE 7760D /DC902 MVD1	V.mv			202	
#Start Time 2023-05-1	16 11:11:15.700000	wpy -				
#Done executing AF #End Time 2023-05-16	FE77xxD/AFE7769D/PC802_ 6 11:11:15.705000	.MKDIV.py				
#Execution Time = 0.0	00499987602234 s	DAUTRICO				
*	ETTER EKRORS:0, WA	KNINGS	V ==========#	*		
						🐗 Texas Instruments
						•

Figure 3-7. Running the RNS802 Script

3.5 AFE7769D Programming Method 2: Using GUI Mode

Note

For GUI Mode automation, the final step will require reference to Picocom's **PC802 EVB RFIC Demonstration User Guide** (Version 3), which can be procured through submitting a request on the company site.

 Open the AFE77xxD Latte GUI version 1.4. Make sure the insterface looks like Figure 3-8, then click Continue. The message "Couldn't Detect FPGA Reset FTDI. Please reset FPGA manually." is expected and can be ignored.

Open AFE77xxD Latte		
Device	AFE77xxD	٠
AFE_CHIP_ID	0x77D	•
FPGA_Type	None	•
AFE_Board_Type	EVM-1DeviceJ58	•
AFE_CHIP_VERSION	0×10	•
SetupType	Basic	÷
AFE_Board_USB_Handle Qu	ad RS232-HS	
AFE EVM Card Detected. Couldn't Detect FPGA Reset	FTDI. Please reset FPGA manually.	

Figure 3-8. Launching AFE77xxD Latte Software



2. Wait until the GUI loads to the User Guide window, as shown in Figure 3-9. Click the *AFE-Configuration* tab under the tree view on the left for the main parameters screen.

-Guide Configuration	User Guide
Test Status GA-Operations PI-Sequence-Generator	AFE-Configuration Test Status FPGA-Operations
	Configuration Generation
	 Navigate to "AFE-Configuration" page, and select the appropriate settings such as Fref, IBW, IQ rate, LO Frequency, etc., to be configured for testing. Note: The power value entered in "Tx Input RMS (dBFS)" will be the maximum expected input signal power from the FPGA for the PA to operate at its rated output power level.
	 Click on the "Generate Configuration" button to generate the system parameters and store in the Excel configuration file.
	 Once the Excel configuration file has been generated, some of the settings such as CFR bandwidth configuration, AGC, PAP, etc., can be reviewed in their respective pages under the "Initialization" section, by clicking on the "Refresh GUI" button under the appropriate pages. Note: Only one channel must be selected when clicking on the "Refresh GUI" button. This will display settings currently used for that channel. If no channel is selected, then TX1 will be updated by default.
	 If any of the parameters must be modified, select one or more channels to be updated with new settings, modify the required fields, and click on the "Update Excel" button.
	 After generating or loading the Excel configuration file, click on "Run Device Bring-up" in the "AFE-Configuration" page. Once the bring-up is complete, "AFE configuration Complete" message will be printed in the "Log" window.

Figure 3-9. User-Guide, AFE77xxD Latte Software

 Click Browse under Load System Parameters and select the "AFE77xxD_Picocom_pc802_K1L.xlsx" config file under "\Documents\Texas Instruments\AFE77xxDLatte\lib\configs". After selecting the file, click LOAD. Figure 3-10 shows the main window screen. You should also see a message in the Log window saying that the configuration was loaded.







Figure 3-10. Main Window: AFE-Configuration

4. After that, under *Hardware Connection*, click the refresh GUI button to see a message on the log window saying "Refreshed GUI". Then click *Device Bringup* to start the bringup for the device. For proper navigation, see Figure 3-11.



Figure 3-11. Execute Device Configuration



5. After the device bringup is done, you will see some errors on the log window (shown in Figure 3-12). Two of these errors should be "FPGA Reset device not found" and the rest should be under the "Device DAC JESD-RX 0 Link Status" line. These errors are expected because the JESD link is not up.

Log
LMK Configured.
Fuse farm load autoload done successful
No autload error
Fuse farm load autoload done successful
No autload error
AFE Reset Done.
pll1: True; LO Frequency: 2949.12
FPGA Reset device not found
FPGA Reset device not found
FPGA Configured.
AFE MCU Wake up done.
pll0: True; LO Frequency: 3500.01
pll1: True; LO Frequency: 2949.12
AFE all PLLs configured.
FB DSA 3.5G Band
AFE SerDes configured.
AFE Digital Chains configured.
AFE DAC Analog Writes configured.
AFE RX Analog Writes configured.
AFE FB Analog Writes configured.
AFE JESD configured.
AFE GPIO configured.
AFE TX IQMC-LOL Correction configuration Complete
AFE DPD Block configuration
AFE DPD Block configuration Complete
AFE RX IQMC configuration Complete
AFE RX AGC configuration Complete
###########Device DAC JESD-RX 0 Link Status##############
Comma Align Lock Lane0: False; Please check if the transmitter is sending data and eye is good.
lane0 Errors=0b1000000000000; Got errors: Serdes loss of signal(LOS) indicator;
CS State TX0: 0b00000000 . It is expected to be 0b00000010
FS State TX0: 0b00000000 . It is expected to be 0b00000001
Couldn't get the link up for device RX: 0

AFE configuration Complete
#=====================================

Figure 3-12. Latte Log Window Post-Device Configuration

6. At the top, click *Latte Mode* and navigate to *Script Mode* as shown in Figure 3-13.

Ē	Xi AFE77xxD												
I	File	Edit	it View Run Log Session Help Latte					Latte Mode					
	Tree	Tere View							GUI Mode	Ctrl+Shift+L			
	User-Guide								Script Mode	Ctrl+Shift+S			
	~	AFE-Co	onfigura tializatio	ation on									

Figure 3-13. Switching to Script Mode

7. Open the PC802_LMKDIV.py script on the tree view on the left, as shown in Figure 3-14.

👪 AFE77xxD







8. Run the script by pressing F5 or by clicking Run > Buffer. An output in the log window like Figure 3-15 signals that the script was run with no errors. After running this script, the LMK_LOCKED LED (D11) turns on if the 122.88MHz reference from the RNS802 is connected.

AFE77xxD	G.						- 🗆 ×
File Edit View	Run Log S	ession	Help La	tte Mode			
Scripts Files V AFE77xxD AFE7769D	Buffer Run Selec File Pause	tion	F5 F7 F8 F9	I head page JLLL Config ClimD.1.2 Divider dis_climD.1.5.10.gst = 4 head page JLLL Config ClimD.1.2 Divider dis_clim1.5.11.0.gst = 4 .head page JLLL Config ClimD.1.2 Divider dis_climD.1.5.10.gst = 4 head page JLLL Config N.Divider JLL.N.DUV JLLL 15.0.gst = 4			Instrument List 6 Device Source clk RF Source clk Signal Source
> PC802_LMK > picocom_03*	Stop Create Se Wait time Main Thre	for server ad time c	F10				Device List de CPLD DONOT_OPEN_Afe77xxDPG1p0_FULL LMK Clock Divider
							Engine List Ø HSCEngineWithILDDCDGC
							Custom GUI List B CGui_Custom_GUI
Log					6	Command Line	8
AFE configuration Com #Executing AFE77xx #Start Time 2023-05-1 #Done executing AF #End Time 2023-05-16 #Execution Time = 0.0. #Execution Time = 0.0.	plete CO/AFE7769D/PCI 6 11:11:15.7000 E77xx0/AFE7769 11:11:15.70500 0499987602234 ===== ERR01	85:5, WA	RNINGS: %py .MKDI%py RNINGS:	0 <i>f</i>	< v	Welcome to Asterix Command Line!! from globalDefs import '	
							🜵 Texas Instruments

- Figure 3-15. Running the LMK Script
- 9. Click *Latte Mode* and navigate to *GUI Mode* as shown in Figure 3-16.

La A	FE//xx	D							
File Edit View Run Log		Session	Help	Latte Mode					
Tre	e View							GUI Mode	Ctrl+Shift+L
~	Tree View User-Guide ✓ AFE-Configuration > Initialization							Script Mode	Ctrl+Shift+S



10. Click *TX-Test* under the tree view, as shown in Figure 3-17.



Figure 3-17. Switching to the Channel Controls Tab in Latte

11. Enable the TDD for the TX channels by setting them to green like in Figure 3-18. Then, click Set TX TDD. A message should appear on the log window that says "TDD set".





Figure 3-18. Enabling TX TDD

12. Proceed to set up the RNS802 by following the PC802 EVB RFIC Demonstration User Guide (Version 3) from section 2.2. When you get to section 2.2.5, after you enter the *start* command on the test mode tool to start sending data, type the "AFE.adcDacSync(1)" command in the Command line of the AFE77xxD GUI. You should now be able to see a report in the log window that the JESD link is up with no errors like in Figure 3-19. Data now flows through the AFE TX channel.

Log	5	Command Line
APE Compute complete #====== #Executing AFE77xxD/AFE7769D/PC802_LMKDIV.py #Start Time 2023-05-16 16:29:36.212000 #Done executing AFE77xxD/AFE7769D/PC802_LMKDIV.py #End Time 2023-05-16 16:29:36.216000 #Execution Time = 0.00400018692017 s #============= ERRORS:0, WARNINGS:0 =========# TDD Set. ####################################		<pre>Welcome to Asterix Command Line!! from globalDefs import * >>> AFE.adcDacSync(1) >>></pre>

Figure 3-19. JESD Link Bringup

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2023) to Revision A (May 2025)					
•	Added RANsemi RNS802 SoC information to the document	2			
•	Changed required software from: AFE77xxD Latte v0.4 to: AFE77xxD Latte v1.4 or later	3			
•	Changed AFE77xxD Latte GUI zip folder name from: V0p4.zip to: V1p4.zip	4			
•	Changed the AFE7769D Programming Method 1: Automated instructions	4			
•	Changed the AFE7769D Programming Method 2: Using GUI Mode instructions	6			

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