EVM User's Guide: ADS131E08EVM-PDK

ADS131E08EVM-PDK Evaluation Module

Description

The ADS131E08 evaluation module (EVM) is a platform for evaluating the performance of the ADS131E08, which is a 24-bit, 64-kSPS, 8-channel, simultaneous-sampling delta-sigma ADC for energy metering and power protection applications. The evaluation kit includes the ADS131E08EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over USB for data capture, configuration, and analysis. This user's guide includes a complete circuit description, schematic diagram, and bill of materials.

Get Started

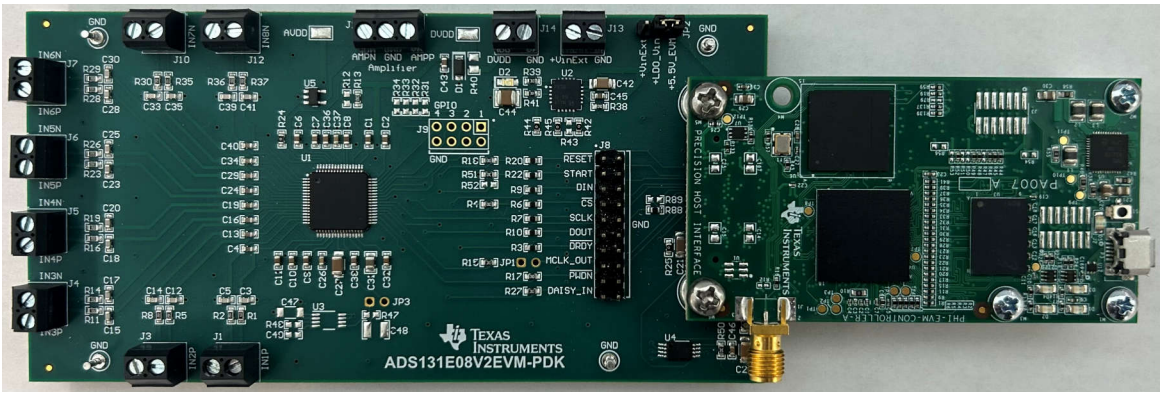
1. Order the EVM from the ADS131E08EVM-PDK tools page.
2. Download the GUI software from ADS131E08EVM-PDK.
3. Connect the EVM to the PHI and connect the PHI to the computer running the EVM GUI.
4. Launch the ADS131E08 EVM GUI.
5. Refer to the ADS131E08 data sheet for IC details.
6. Visit the E2E forums for support and questions.

Features

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS131E08
- The PHI controller provides a convenient communication interface to the ADS131E08 over USB 2.0 (or higher) for digital input and output
- Easy-to-use evaluation software for 64-bit Microsoft® Windows® 10 operating system
- The software suite includes graphical tools for data capture, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file for post-processing

Applications

- Power protection: circuit breakers, and relay protection
- Energy metering: single phase, polyphase, and power quality
- Battery test systems
- Test and measurement
- Simultaneous sampling data acquisition systems



1 Evaluation Module Overview

1.1 Introduction

The ADS131E08EVM-PDK is a platform for evaluating the performance of the ADS131E08, a 24-bit, 64-kSPS, 8-channel, simultaneous-sampling delta-sigma ADC. The evaluation kit includes the ADS131E08 EVM and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over USB for data capture and analysis. The ADS131E08 EVM includes the ADS131E08 and all the peripheral analog circuits and components required to evaluate the performance of the ADS131E08. The PHI controller primarily serves three functions:

- Provides a communication interface from the ADS131E08 EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS131E08 ADC
- Supplies power to all active circuitry on the ADS131E08 EVM

This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS131E08 EVM.

1.2 Kit Contents

The ADS131E08EVM-PDK includes the following components, as shown in Figure 1-1:

1. The PHI controller board.
2. The EVM that includes the ADS131E08 and peripheral circuitry required for device operation and communication with the PHI board.
3. An A-to-micro-B USB cable for communication between the PHI board and the EVM GUI.
4. The EVM GUI, which can be found online in the EVM tool folder.

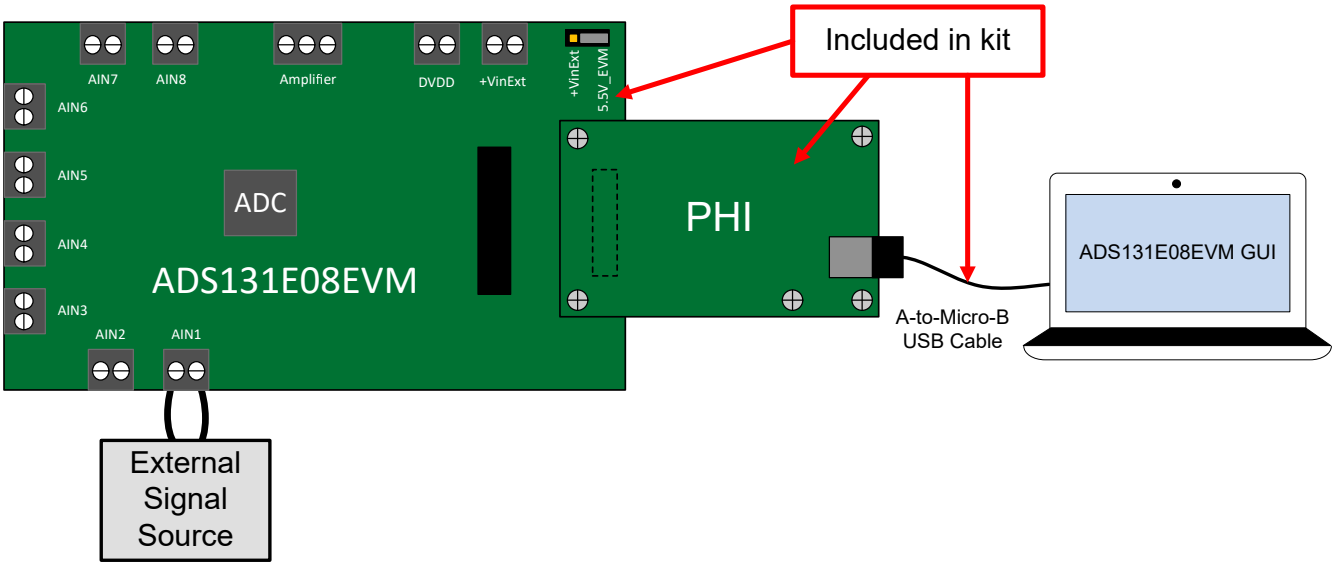


Figure 1-1. System Connection for Evaluation

1.3 Device Information

Please refer to the ADS131E08 data sheet for complete specifications.

Table 1-1. ADS131E08 Specifications

DEVICE SPECIFICATION	VALUE
Package size	12.00mm x 12.00mm
Operating temperature range	-40°C to 105°C
AVDD (AVSS = DGND) supply voltage	2.7V to 5.25V
DVDD to DGND supply voltage	1.7V to 3.6V
Voltage reference inputs	2V to AVDD (AVSS = DGND)

1.4 Specification

The following specifications are applicable to the EVM and the PHI controller.

Table 1-2. ADS131E08EVM-PDK Specifications

PARAMETER	CONDITIONS	VALUE
Temperature	Recommended operating free-air temperature range, T_A	15°C to 35°C
Power supply input range	Voltage input range for J13 ()	+5.5V to +6.5V
	Supply current range $\|I_S\|$	300mA ≤ $\|I_S\|$ ≤ 500mA
Analog input voltage range	Recommended analog input voltage for CH1-CH8	0V to Vref/Gain
EXT clock frequency	CLKSEL pin = 0, (AVDD - AVSS) = 3V	1.7 to 2.25MHz
	CLKSEL pin = 0, (AVDD - AVSS) = 5V	1.0 to 2.25MHz
Digital logic input levels	Recommended digital voltage high level (V_{IH})	0.8 DVDD ≤ V_{IH} ≤ DVDD+0.1
	Recommended digital voltage low level (V_{IL})	0.2 DVDD ≥ V_{IL} ≥ DGND
ADS131E08 AVDD Voltage range	Voltage supplied to ADS131E08 AVDD pins from onboard regulator or external source	+2.7V to +5.25V
ADS131E08 DVDD voltage range	Voltage supplied to ADS131E08 DVDD pin from PHI or external source	+1.7V to +3.6V
ADS131E08 VREF voltage range	Voltage supplied to JP3 (optional VREF input)	+2V to AVDD

2 Hardware

The ADS131E08 EVM is designed for easy interfacing with analog input sources. This section describes the details of the front-end circuit, power supplies, ADC connections, and other board connections.

2.1 EVM Analog Inputs

The EVM provides users the option to apply signals from any arbitrary signal source directly. Eight analog signals can be applied at terminal blocks J1, J3, J4, J5, J6, J7, J10 and J12. The ADS131E08 analog inputs are fully differential. Drive the analog inputs with one of the following general methods: pseudo-differential or fully-differential. Refer to the *Analog Input* section of the ADS131E08 data sheet for details regarding how to drive the ADS131E08 inputs. Refer to the *Input Common-Mode Range* section of the ADS131E08 data sheet for details on the usable input common-mode range of the analog front-end.

Each analog input channel includes an anti-aliasing filter that consists of series resistors, a differential capacitor, and common-mode capacitors. The anti-alias filter cutoff frequencies set by these components are:

Common mode filter cutoff :

$$\left(f_{CM}\right) = \frac{1}{2\pi R_{IN} C_{CM}} = \frac{1}{2\pi(1k\Omega)(470pF)} = 339kHz$$

Differential filter cutoff:

$$\left(f_{DIF}\right) = \frac{1}{2\pi\left(2R_{IN}\right)\left(C_{DIF} + \frac{1}{2}C_{CM}\right)} = \frac{1}{2\pi\left(2 * 1k\Omega\right)\left(4700pF + \frac{1}{2}470pF\right)} = 16.125kHz$$

The differential capacitor value is 10 times larger than the common-mode capacitor. Choosing this ratio of capacitors sets the differential mode cutoff frequency approximately 20 times lower than the common-mode cutoff frequency. Using this ratio of filter cutoff frequencies prevents common-mode noise from being converted into differential noise due to component tolerances.

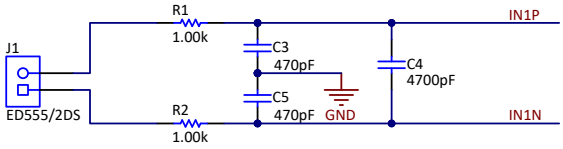


Figure 2-1. Analog Inputs

2.2 Power Supplies

The ADS131E08 EVM is directly powered by the PHI controller by default. The PHI provides 5.5V to a TPS7A47 LDO. The LDO output provides a stable supply for the ADC analog supply (AVDD). The default output of the LDO is 5V and can be reprogrammed to output 3V by populating or depopulating R42, R43, and R45. The PHI also supplies the voltage for the ADC digital supply (DVDD). Figure 2-2 shows the power supply circuitry. The EVM optionally supports external power supplies. Provide external power supplies by following the steps outlined below:

1. Depopulate R25 and populate R40 to use an external supply for DVDD. Provide the DVDD supply voltage through terminal block J14.
2. Move JP2 jumper to connect +VinExt to +LDO_Vin to provide an external supply to the LDO. Provide external power to the LDO though terminal block J14.
3. Remove R44, install TP10 and apply the AVDD voltage to TP10 to power AVDD directly without using the onboard LDO.

The ADS131E08EVM only supports unipolar power supplies.

The AVDD voltage rail also includes an indicator LED to verify the LDO is working properly. AVDD and DVDD have a test point for convenient verification of power supply functionality.

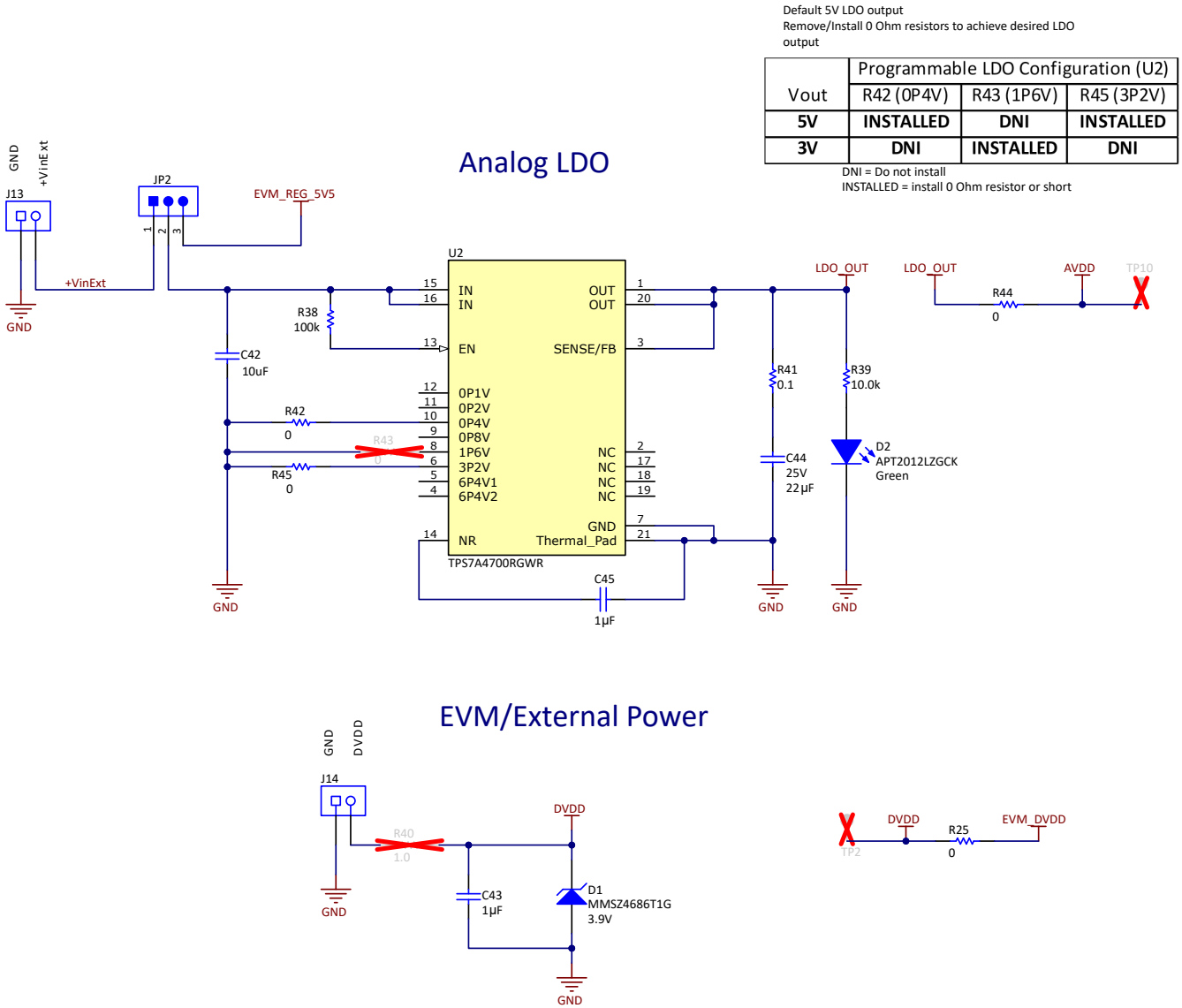


Figure 2-2. Power Supply Circuitry

2.3 ADC Connections and Decoupling

Figure 2-3 shows all connections to the ADS131E08 (U1). Each analog power supply connection has a 1µF decoupling capacitor. Place these capacitors physically close to the device and make sure the capacitors have a good connection to the GND plane. Also, each digital input has a 10Ω series resistor. These resistors smooth the edges of the digital signals so that the signals have minimal overshoot and ringing. Although not strictly required, these components can be included in final designs to improve digital signal integrity.

The EVM uses the ADS131E08 internal clock by default. Alternatively, use an external clock by installing the JP1 header and then applying a clock signal to the CLK pin of JP1.

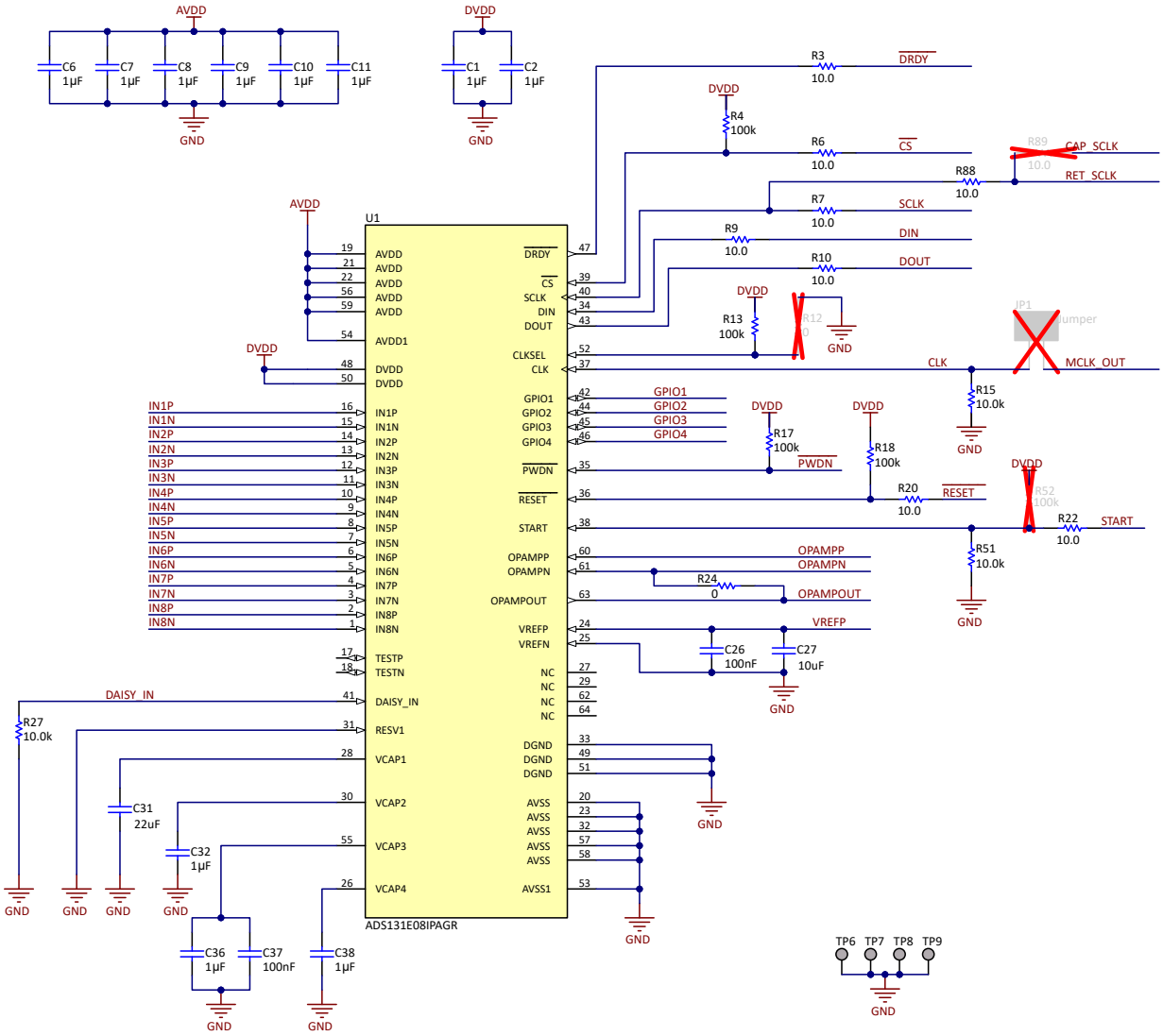


Figure 2-3. ADS131E08 Connections and Decoupling

2.4 Voltage Reference

The ADS131E08 has an integrated voltage reference that provides a 2.4V or 4V reference voltage to the device. Alternatively, power down the internal reference and apply an external reference voltage on the VREFP pin of JP3. Apply the voltage reference externally by installing JP3 and providing the externally generated reference through JP3. Figure 2-4 shows the EVM circuitry for an external voltage reference (U3) such as the REF6241. The external voltage reference must be installed by the user. Set the external reference voltage between 2V and AVDD, depending on the analog supply voltage.

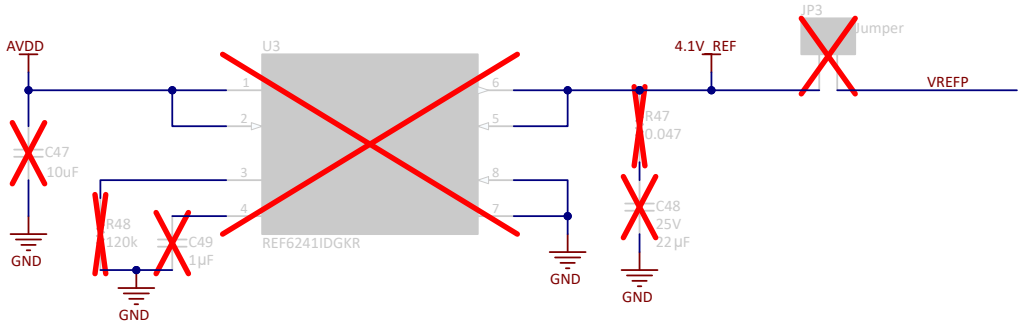


Figure 2-4. External Reference Circuitry

2.5 Op Amp Common-Mode Bias

The analog input network must be biased to mid-supply because the EVM only supports a unipolar-supply analog configuration (AVSS = 0V, AVDD = 2.7V to 5.5V). The ADS131E08 includes an internal op amp whose output can be used as a common-mode bias voltage [(AVDD + AVSS) / 2] when using a unipolar power supply.

The EVM includes a buffer for the integrated op amp because this op amp has very limited current sink and source capability. Figure 2-5 shows the buffer circuitry that uses an OPA320.

Generate the common-mode bias voltage from the ADS131E08 by configuring the internal op amp in a unity-gain configuration using the feedback resistor (R24) and setting the OPAMP_REF bit of the CONFIG3 register to 1. Alternatively, generate the common-mode bias voltage externally with a resistor divider network between the positive and negative supplies.

Access the op amp output through terminal block J11.

Reference the *Voltage Sensing* section of the ADS131E08 data sheet for additional information and application examples regarding how to implement the op amp common-mode bias voltage reference.

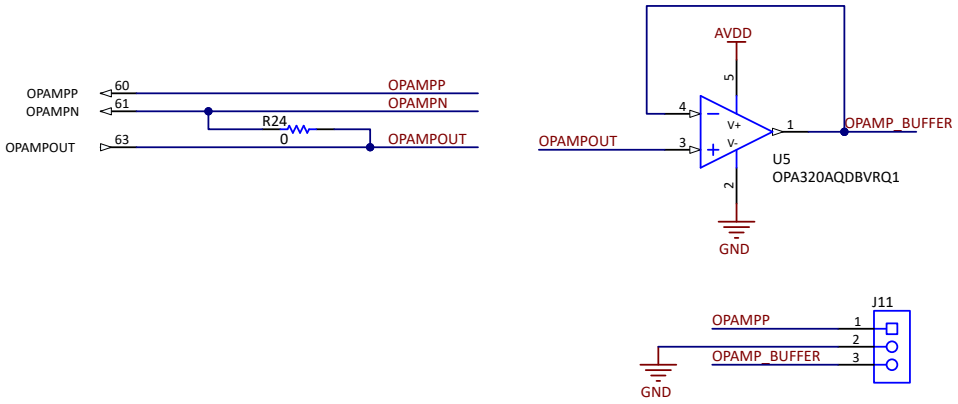


Figure 2-5. Op Amp Bias Reference Circuit

2.6 Digital Interface

Figure 2-6 shows the digital connections between the EVM and the PHI. The EVM interfaces with the PHI and communicates with the computer over USB. The PHI communicates with two devices on the EVM: the ADS131E08 (over SPI) and the EEPROM (over I2C). The EEPROM comes preprogrammed with the information required to configure and initialize the ADS131E08 platform. The EEPROM is no longer used when the hardware is initialized. The ADS131E08 uses SPI serial communication in mode 1 (CPOL = 0, CPHA = 1). The PHI also provides power for the EVM.

Header J8 provides test points to probe the digital signals. Install header J9 to access the ADS131E08 general-purpose input/output pins. The GPIO pins are pulled down to GND by 10kΩ resistors when not used as per the data sheet.

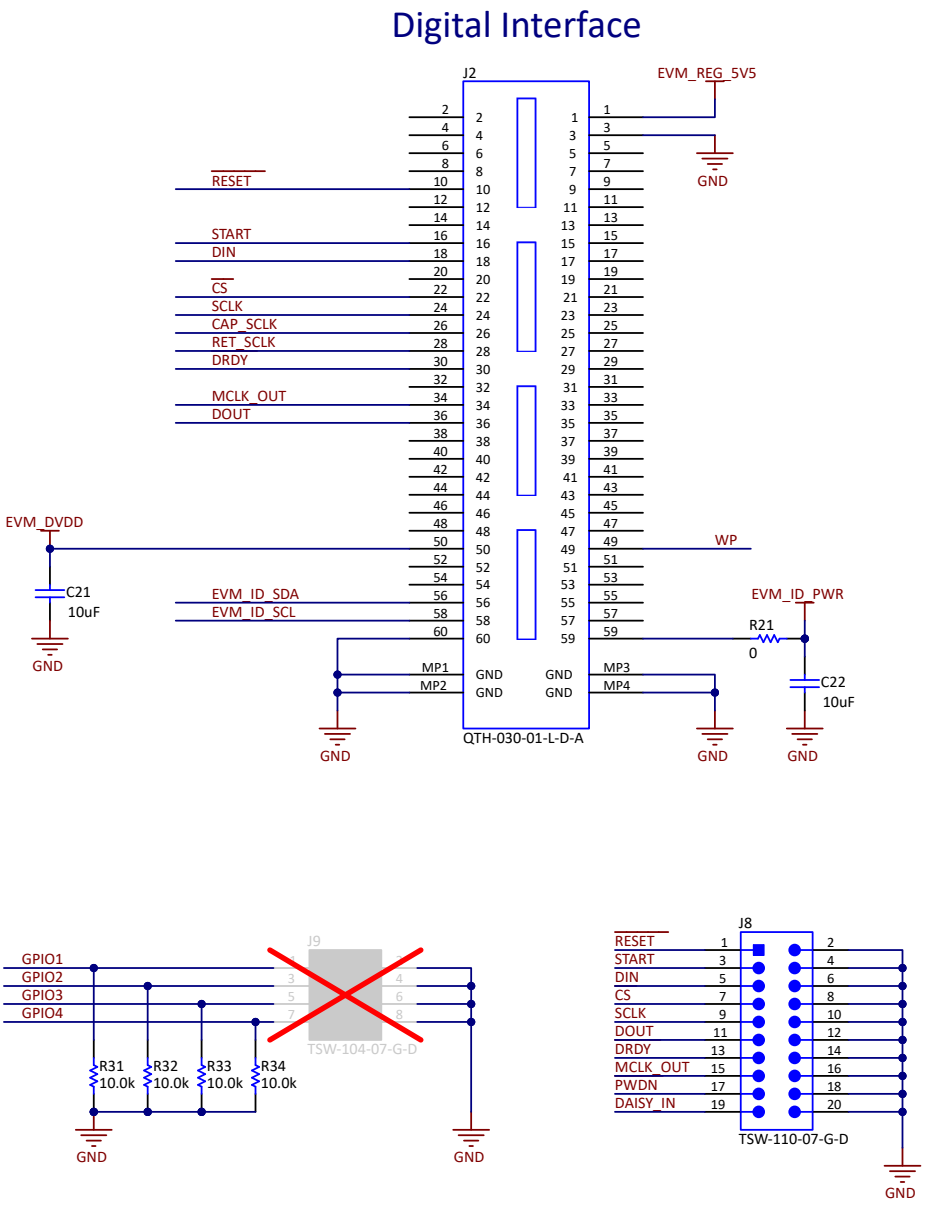


Figure 2-6. Digital Interface Connections

2.7 EEPROM

Figure 2-7 shows the circuitry used with the EVM controller (PHI) for EVM identification. The EEPROM communicates with the PHI over an I2C bus and is not shared with the ADS131E08. This circuit is not required by the ADS131E08 for operation and is not powered when not used with the PHI.

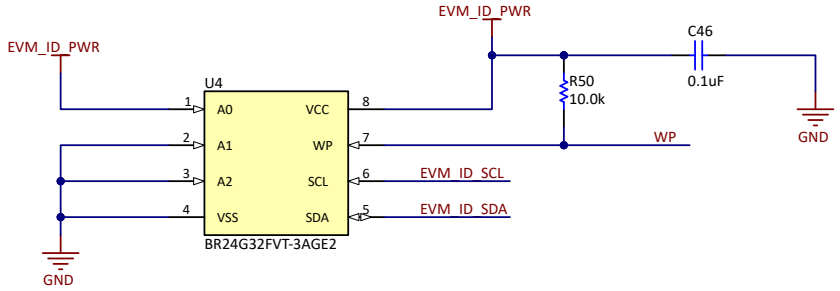


Figure 2-7. EEPROM for EVM ID

3 Software

3.1 Software Description

The ADS131E08EVM-PDK-GUI software suite includes graphical tools for data capture, full ADS131E08 register configuration, time domain analysis, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file for post-processing.

3.2 Software Installation

Download the latest version of the EVM GUI installer from the *Tools and Software* section of the ADS131E08EVM product page and run the GUI installer to install the EVM GUI software on a computer.

> **CAUTION**
> Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message can appear or the installer.exe file can be deleted.

Accept the license agreements and follow the on-screen instructions to complete the installation.

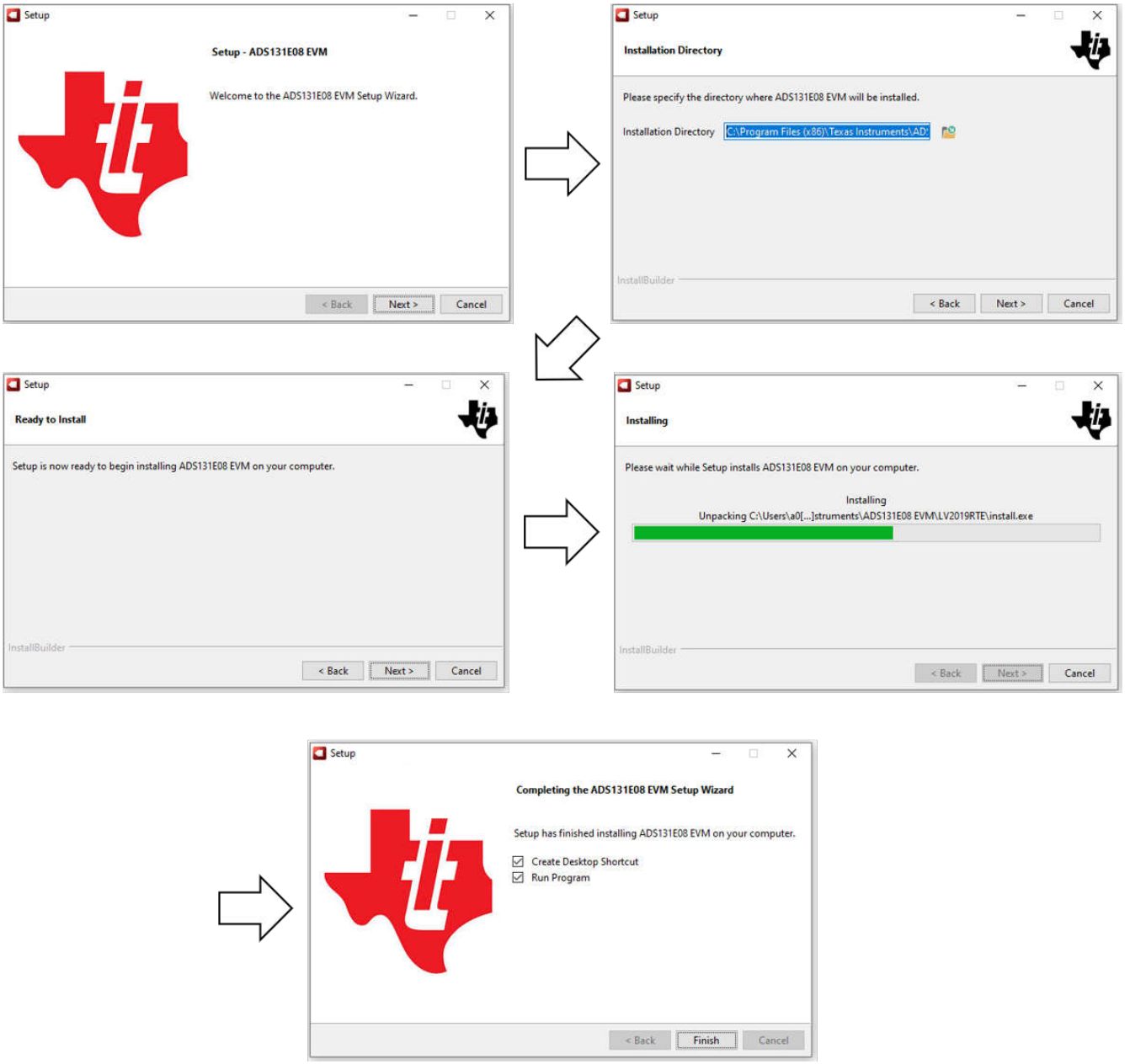


Figure 3-1. Software Installation and Prompts

4 Implementation Results

4.1 Hardware Connections

Connect the EVM as shown in Figure 4-1 after installing the software:

1. Physically connect P2 of the PHI to J2 of the ADS131E08 EVM.
2. Install the screws to provide a robust connection. Connect the USB on the PHI to the computer.
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
   b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC.
3. Start the software GUI by selecting from the start menu or associated shortcut as shown in Figure 4-2. Notice that the LEDs on the PHI blink slowly when the FPGA firmware is loaded on the PHI. Loading takes a few seconds.
4. Connect the signal generator. The ADS131E08 analog inputs are fully differential. The differential input voltage (VINxP – VINxN) can span from –VREF / gain to VREF / gain. Use the ADS131E08 in a differential configuration to maximize the dynamic range of the data converter. For best performance, set the common-mode voltage at the midpoint of the analog supplies [(AVDD + AVSS) / 2].

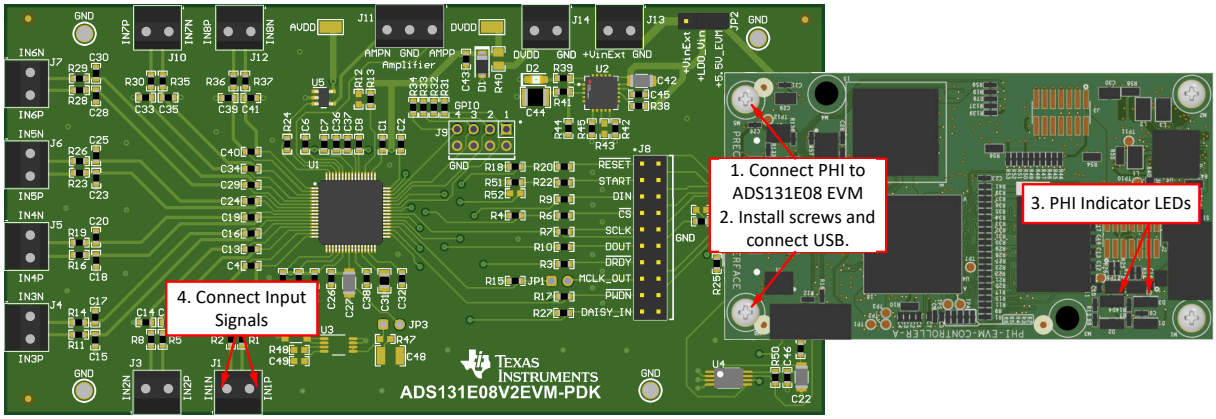


Figure 4-1. Hardware Connections

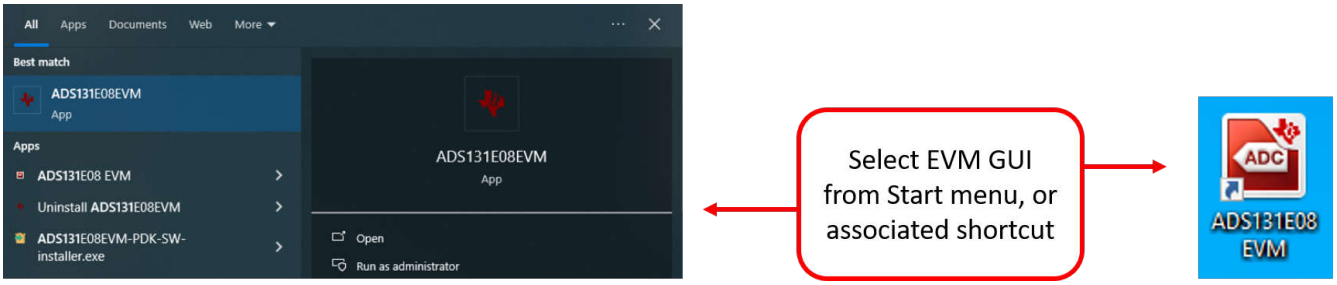


Figure 4-2. Launch the ADS131E08EVM GUI Software

4.2 Optional EVM Configuration

Figure 4-3 shows optional connections to the communication pins, clock, voltage reference, GPIOs, external supplies and op amp bias output. These connections are not required for initial setup of the EVM but can help evaluate device features.

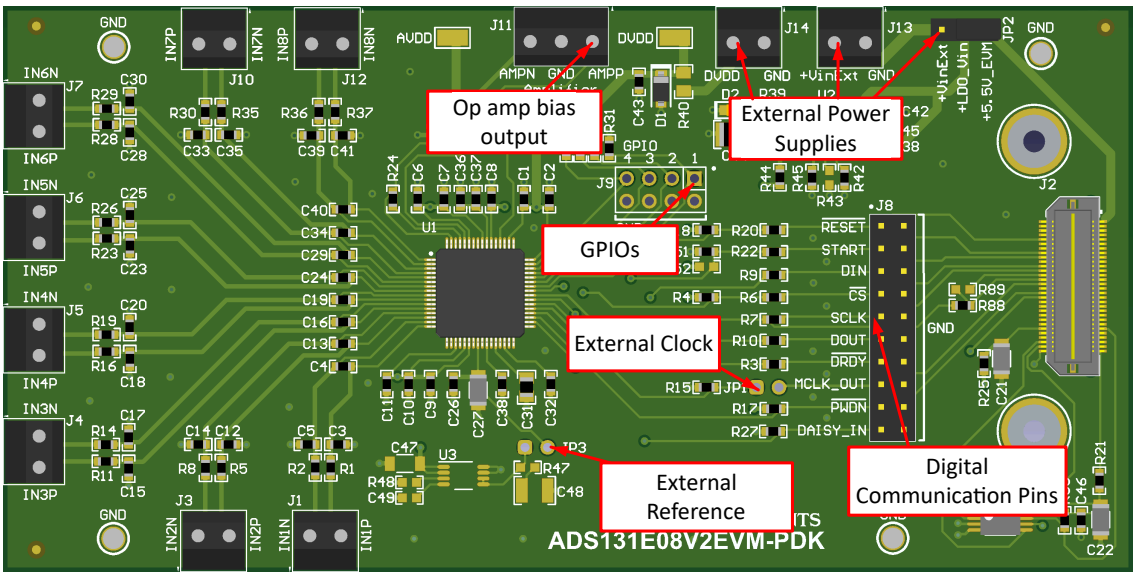


Figure 4-3. Optional EVM Connections

4.3 GUI Software Operation

The following sections describe the pages and functionality of the graphical user interface of the EVM.

4.3.1 EVM Register Settings

Figure 4-4 shows the ADC register configurations. The registers can be used to set the different device modes such as data rate, PGA gain, and others. This page can be accessed by selecting the Register Configurations under *Pages* on the left side of the GUI.

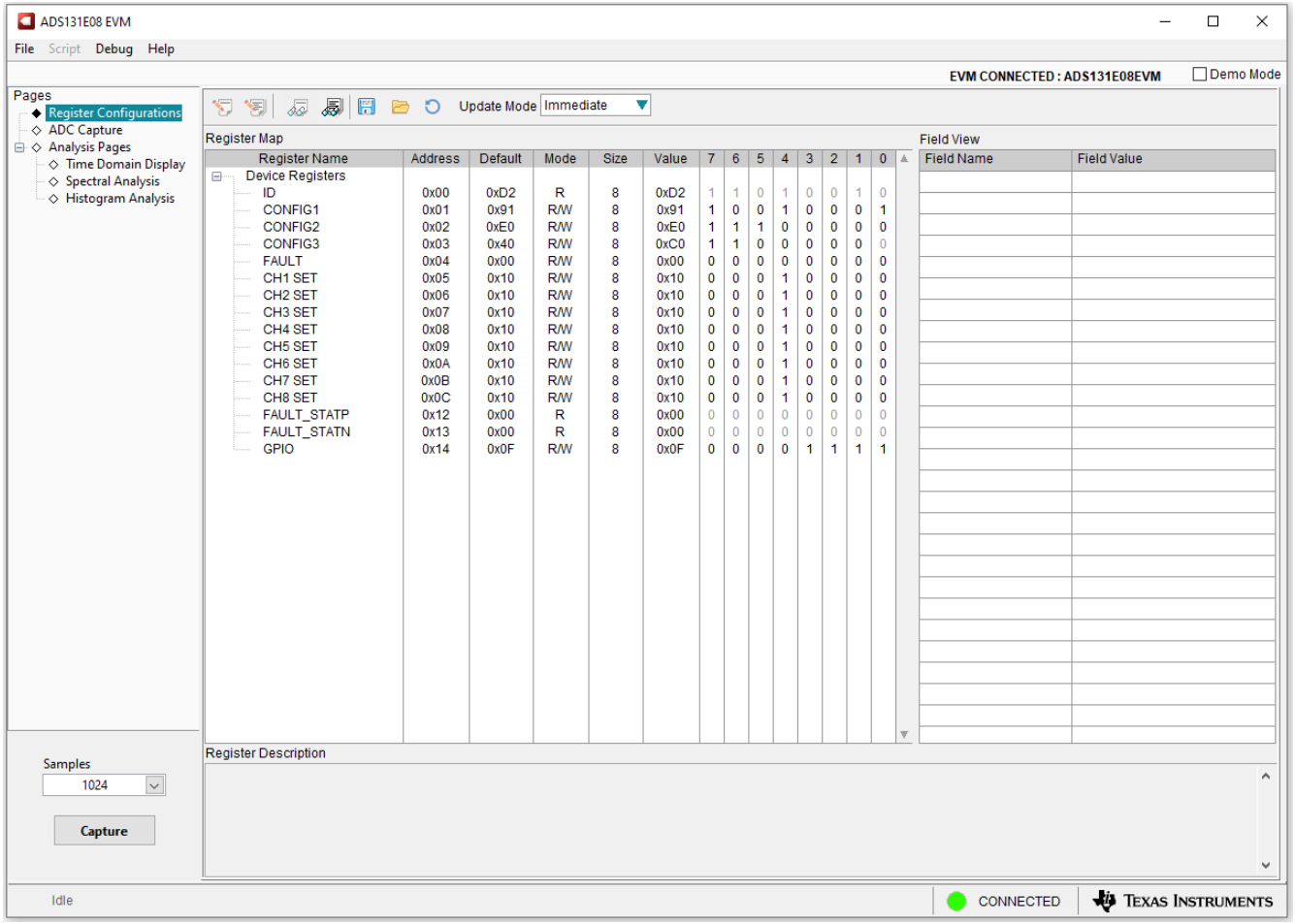


Figure 4-4. EVM Register Configuration

4.3.2 GUI Settings for ADC Control

Figure 4-5 shows the ADC Capture page. This page enables the user to set the desired ADC configurations for data capture. These controls include output data rate and resolution, clock frequency settings, reference voltage, and other important parameters.

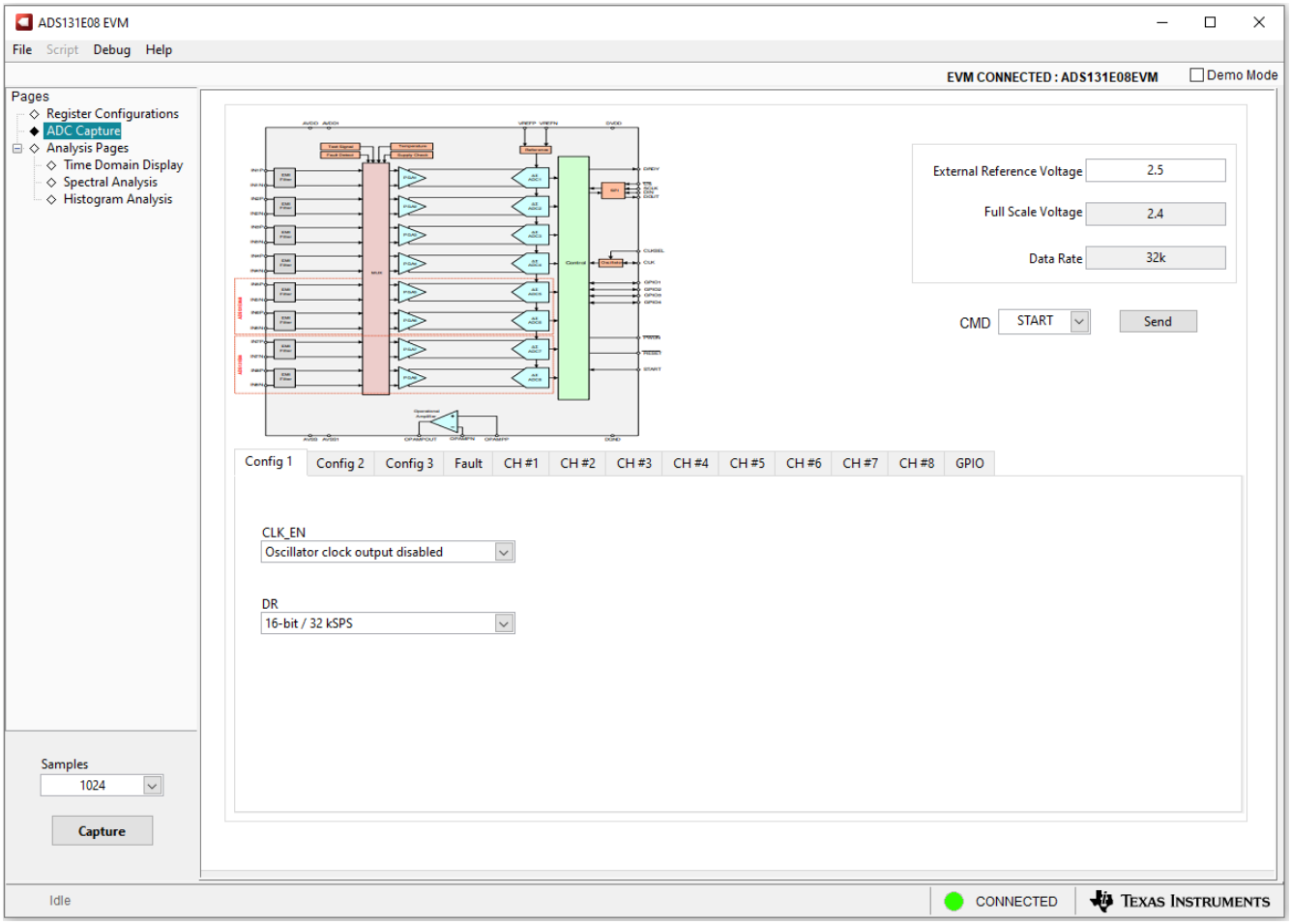


Figure 4-5. ADC Configuration

4.3.3 Time Domain Display

Figure 4-6 shows the time domain display tool that allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits. Capture the selected number of samples from the EVM by using the *Capture* button. The sample indices are on the x-axis while the y-axis shows the corresponding output codes or the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the analysis tools described in the subsequent sections causes calculations to be performed on the same set of data.

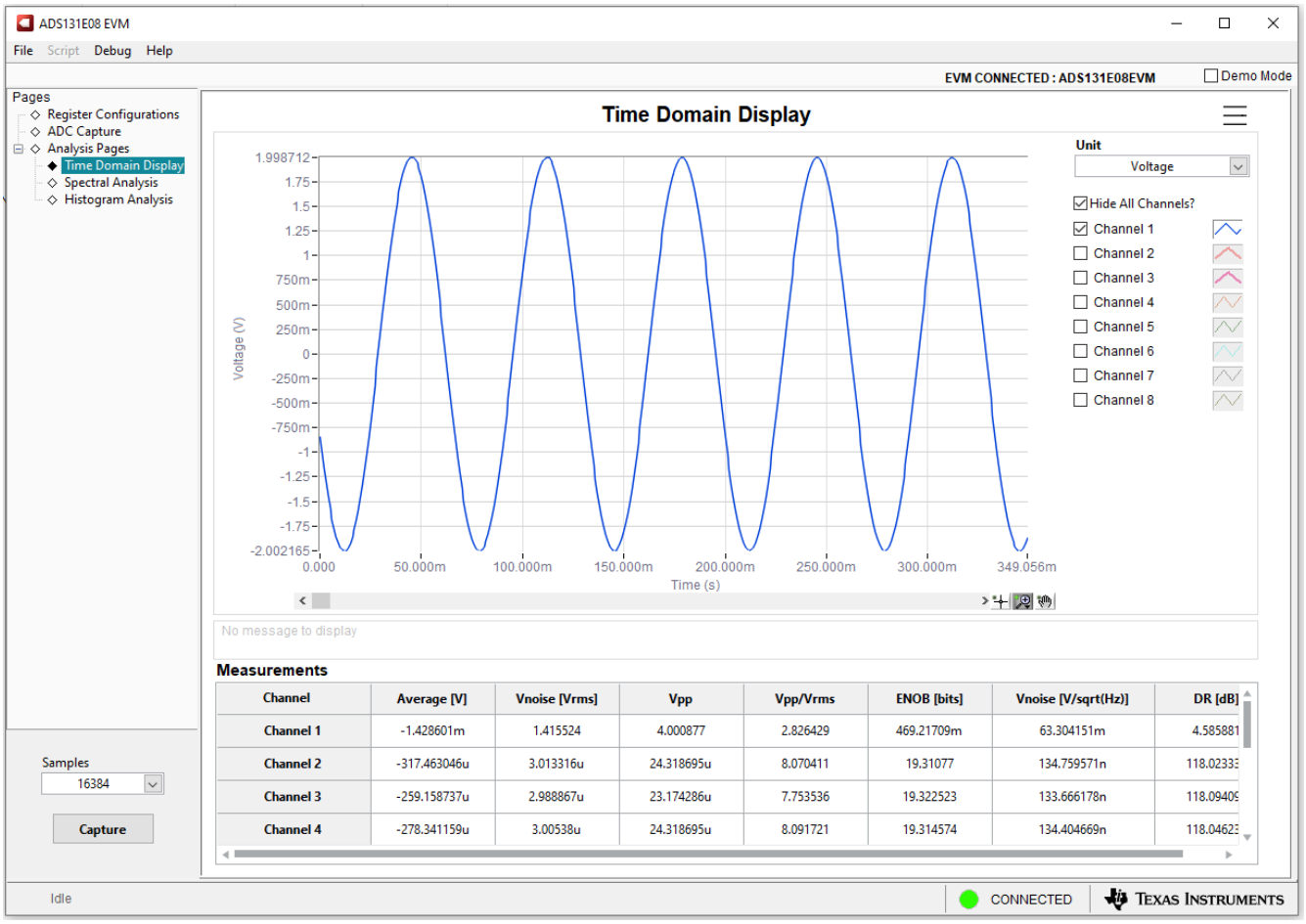


Figure 4-6. Time Domain Display

4.3.4 Frequency Domain Display

Figure 4-7 shows the spectral analysis tool which is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS131E08 ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-Term Blackman-Harris window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The *None* option corresponds to not using a window (or a rectangular window) and is not recommended.

Figure 4-7. Frequency Domain Display

4.3.5 Histogram Display

Figure 4-8 shows the histogram analysis tool. Noise degrades ADC resolution and the histogram tool can be used to estimate effective resolution. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, reference drive circuit, ADC power supply, and the ADC is reflected in the standard deviation of the ADC output code histogram. The histogram is obtained by performing multiple conversions of an input applied to a given channel. The histogram corresponding to an input is displayed by clicking the *Capture* button.

Figure 4-8. Histogram Display

5 Hardware Design Files

This section contains the ADS131E08 EVM schematics, and PCB layout, and bill of materials (BOM).

5.1 Schematics

This section shows the schematics for the ADS131E08 EVM.

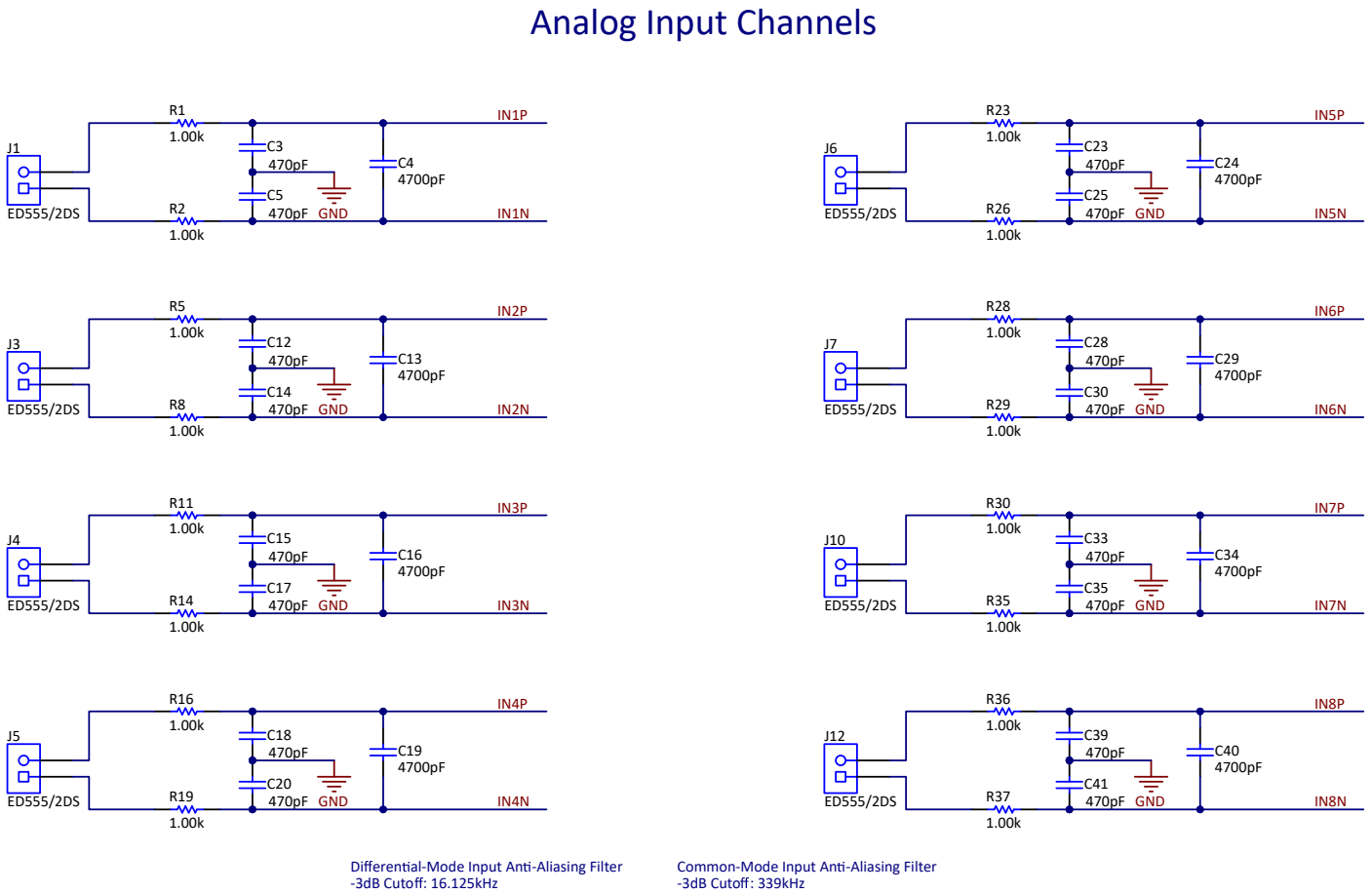


Figure 5-1. Analog Input Channels

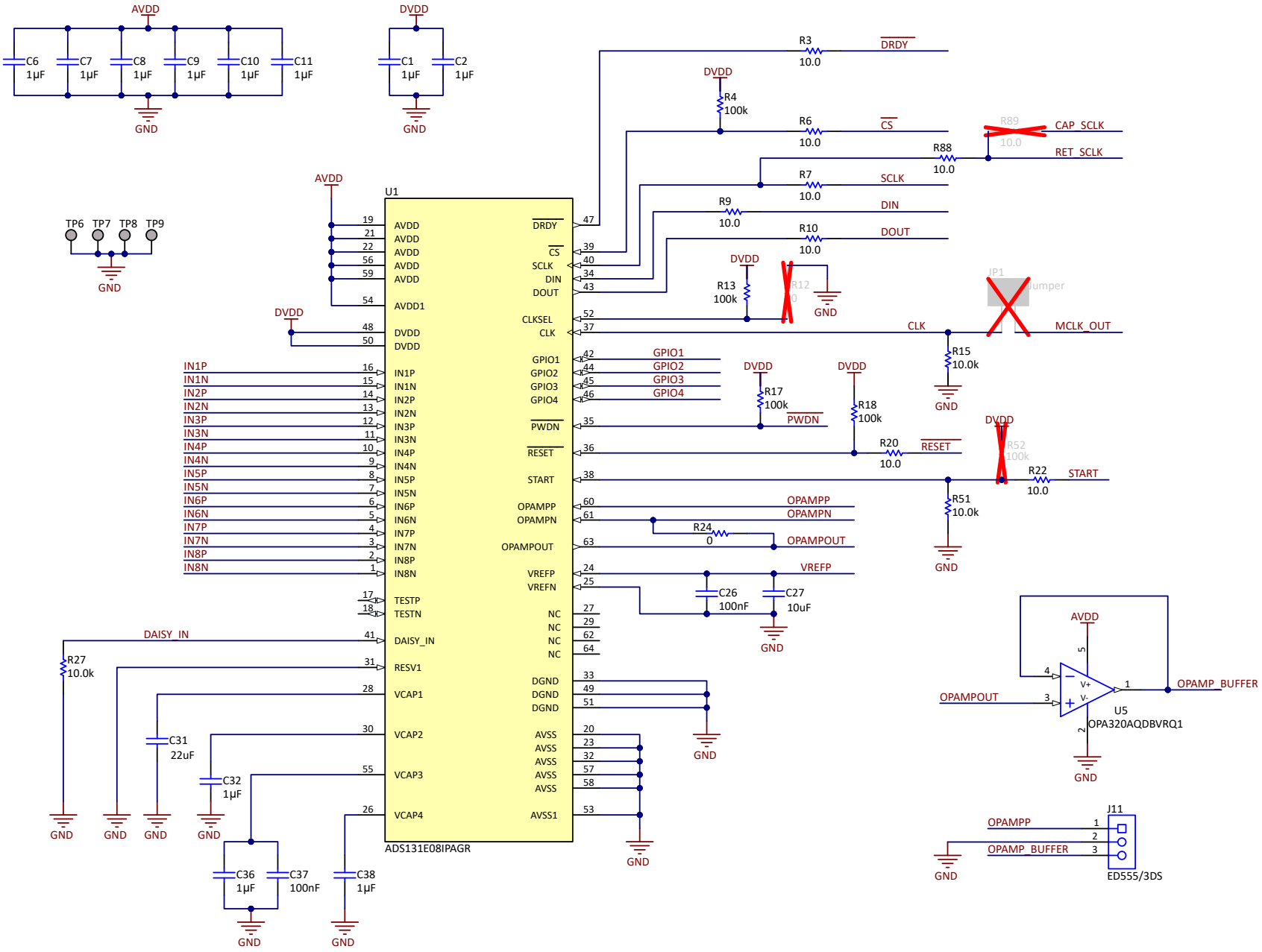


Figure 5-2. ADS131E08 Connections and Decoupling

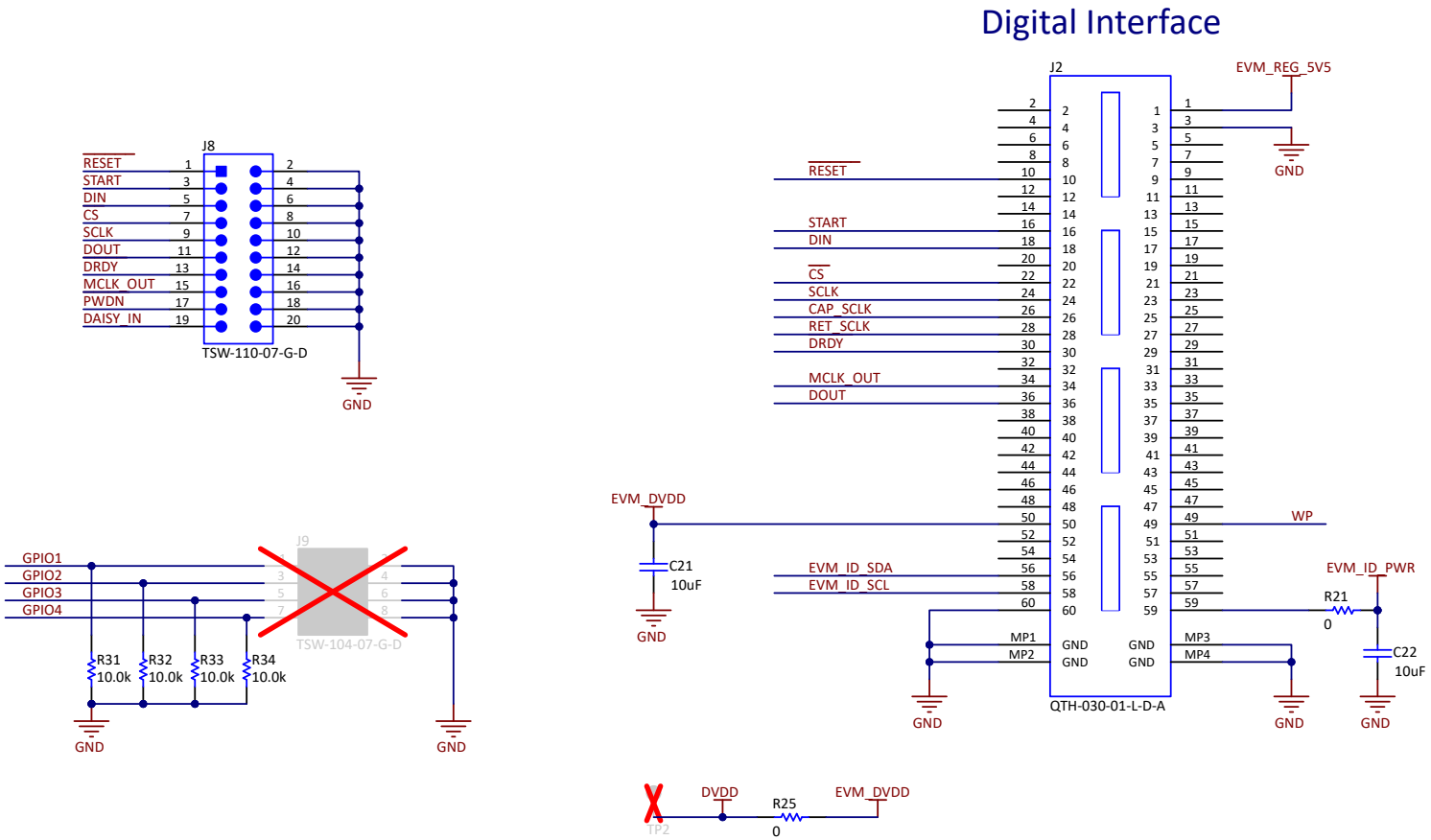


Figure 5-3. Digital Interface and Header Connections

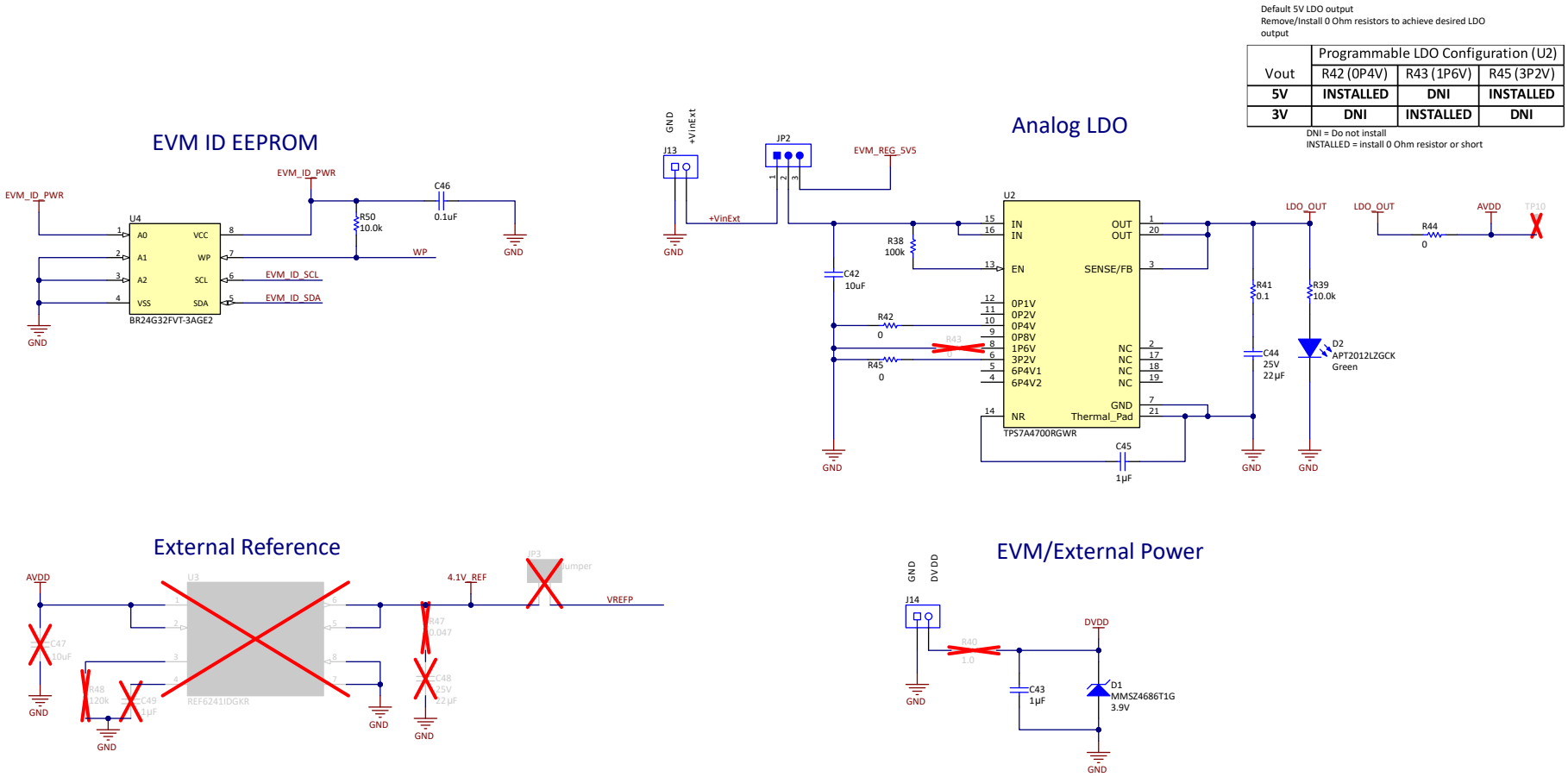


Figure 5-4. Power Supplies, EEPROM and External Reference

5.2 PCB Layouts

Figure 5-5 through Figure 5-8 show the PCB layouts for the ADS131E08 EVM.

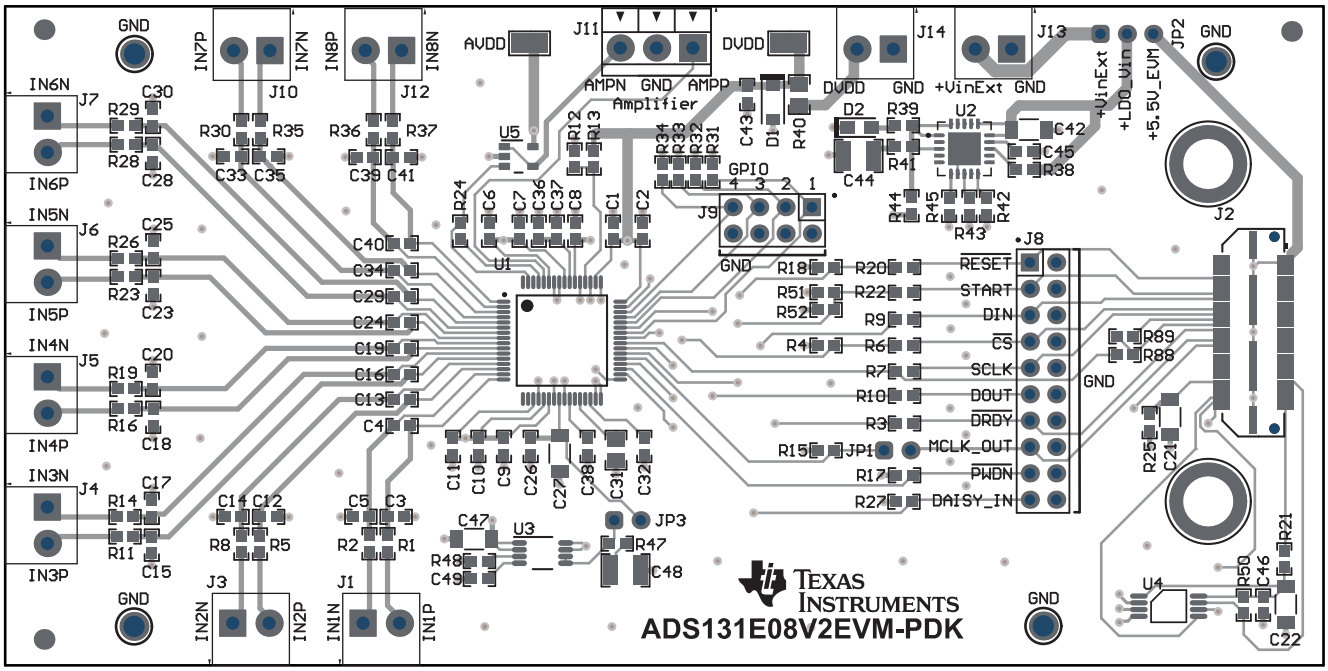


Figure 5-5. PCB Layout for the ADS131E08EVM (Top View)

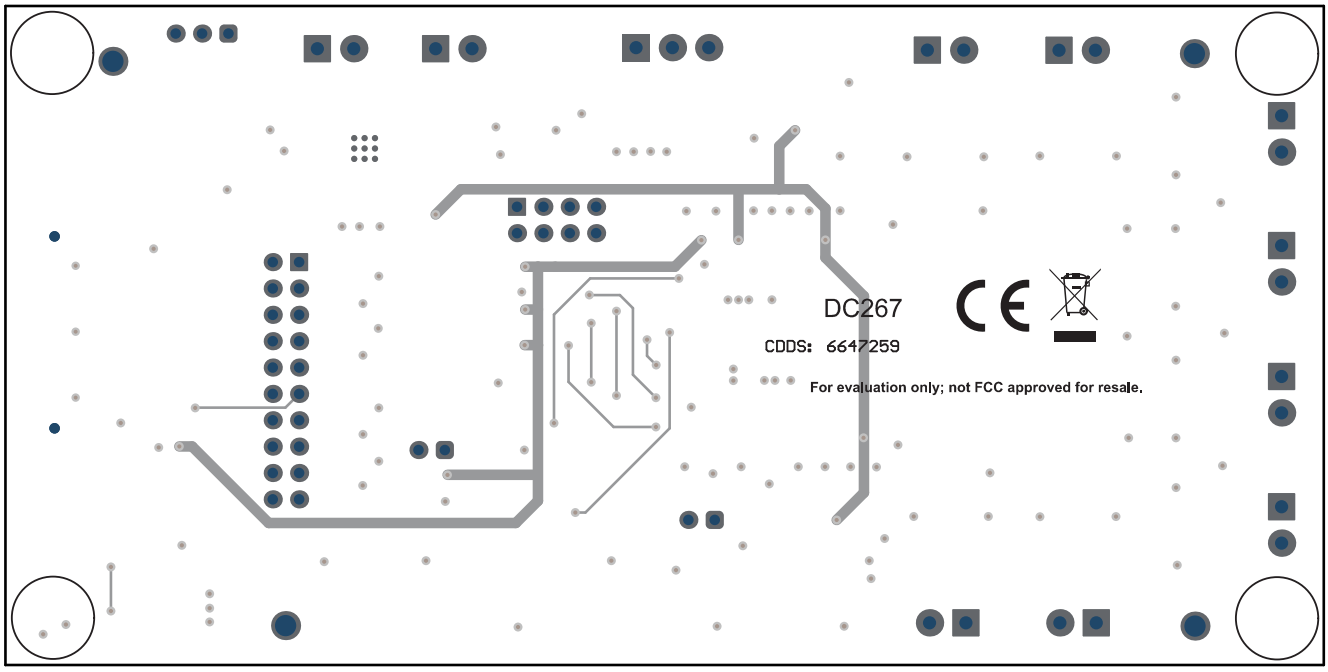


Figure 5-6. PCB Layout for the ADS131E08EVM (Bottom View)

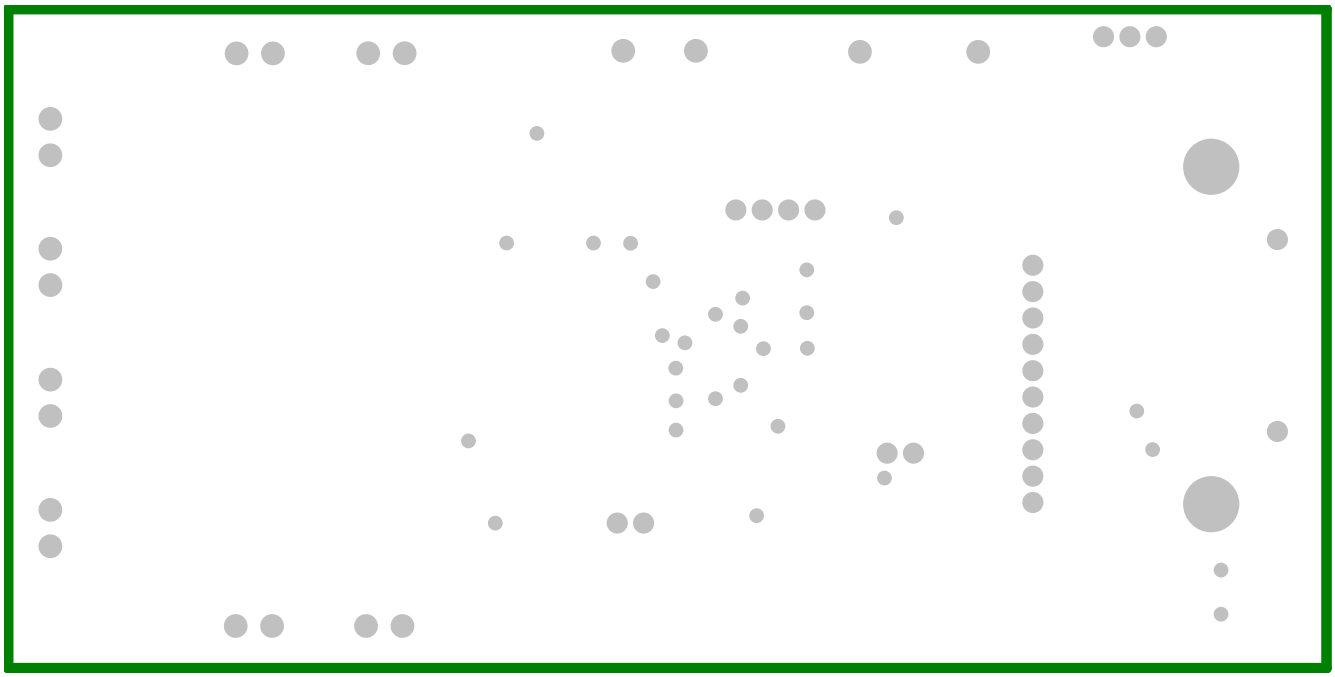


Figure 5-7. PCB Layout (internal AVSS/GND plane 1) for the ADS131E08EVM

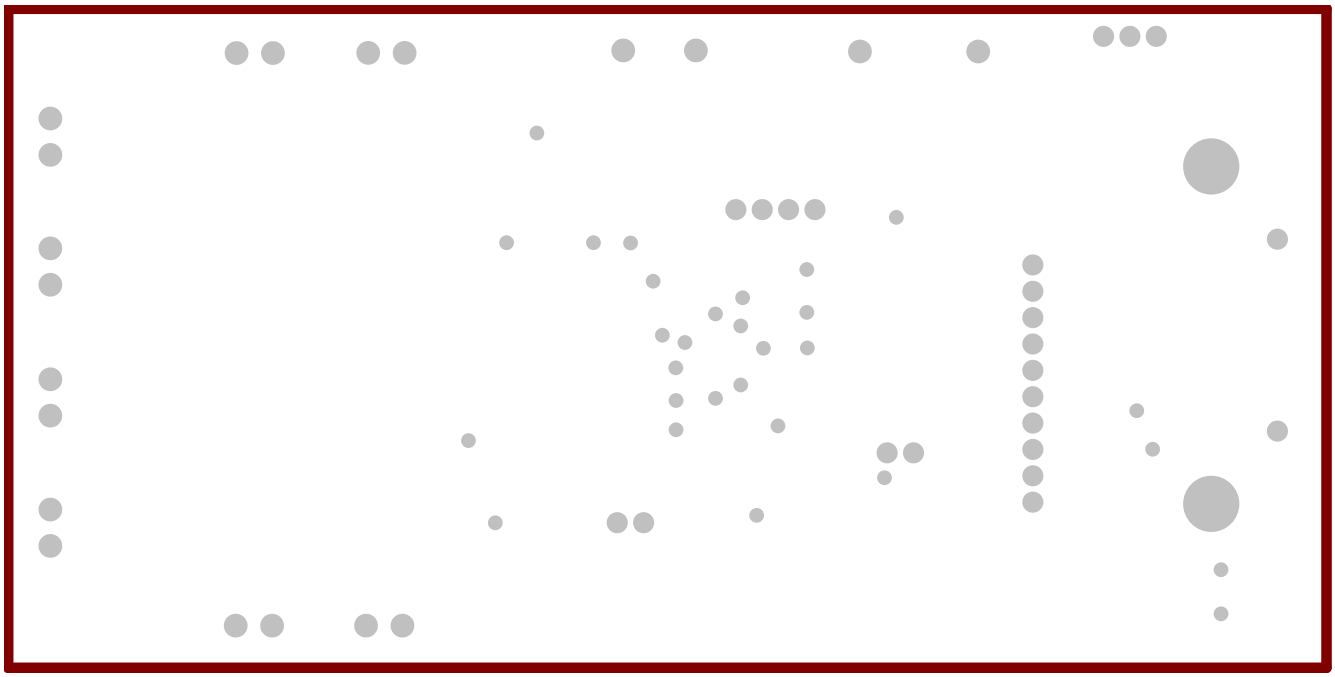


Figure 5-8. PCB Layout (internal AVSS/GND plane 2) for the ADS131E08EVM

5.3 Bill of Materials (BOM)

Table 5-1 lists the bill of materials (BOM) for the ADS131E08 EVM.

Table 5-1. ADS131E08EVM Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		DC267	Any
C1, C2, C6, C7, C8, C9, C10, C11, C32, C36, C38, C43, C45	13	1uF	CAP, CERM, 1uF, 25V, +/- 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet
C3, C5, C12, C14, C15, C17, C18, C20, C23, C25, C28, C30, C33, C35, C39, C41	16	470pF	CAP, CERM, 470pF, 50V, +/- 5%, C0G/NP0, 0603	0603	06035A471JAT2A	AVX
C4, C13, C16, C19, C24, C29, C34, C40	8	4700pF	CAP, CERM, 4700pF, 100V, +/- 5%, C0G/NP0, 0603	0603	C0603C472J1GAC7867	Kemet
C21, C22, C27, C42	4	10uF	CAP, CERM, 10uF, 25V, +/- 10%, X7R, 1206_190	1206_190	C1206C106K3RACTU	Kemet
C26, C37, C46	3	0.1uF	CAP, CERM, 0.1uF, 25V, +/- 5%, X7R, 0603	0603	C0603C104J3RAC	Kemet
C31	1	22uF	CAP, CERM, 22uF, 6.3V, +/- 10%, X5R, 0805	0805	CL21A226KQQNNNE	Samsung Electro-Mechanics
C44	1	22uF	CAP, CERM, 22µF, 25V,+/- 10%, X7R, 1210	1210	CL32B226KAJNFNE	Samsung Electro-Mechanics
D1	1	3.9V	Diode, Zener, 3.9V, 500mW, SOD-123	SOD-123	MMSZ4686T1G	ON Semiconductor
D2	1	Green	LED, Green, SMD	LED_0805	APT2012LZGCK	Kingbright
H1, H2	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL
H3, H4	2		ROUND STANDOFF M3 STEEL 5MM	ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik
H9, H10, H11, H12	4		Bumpon, Cylindrical, 0.312 X 0.200, Black	Black Bumpon	SJ61A1	3M
J1, J3, J4, J5, J6, J7, J10, J12, J13, J14	10		Terminal Block, 3.5mm Pitch, 2x1, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
J2	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A	Samtec
J8	1		Header, 100mil, 10x2, Gold, TH	10x2 Header	TSW-110-07-G-D	Samtec
J11	1		Terminal Block, 3.5mm Pitch, 3x1, TH	10.5x8.2x6.5mm	ED555/3DS	On-Shore Technology

Table 5-1. ADS131E08EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
JP2	1		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
R1, R2, R5, R8, R11, R14, R16, R19, R23, R26, R28, R29, R30, R35, R36, R37	16	1.00k	RES, 1.00 k, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERA3AEB102V	Panasonic
R3, R6, R7, R9, R10, R20, R22, R88	8	10	RES, 10.0, 1%, 0.25 W, 0603	0603	CRCW060310R0FKEAHP	Vishay-Dale
R4, R13, R17, R18, R38	5	100k	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
R15, R27, R31, R32, R33, R34, R39, R50, R51	9	10.0k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603FT10K0	Stackpole Electronics Inc
R21, R24, R25, R42, R44, R45	6	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
R41	1	0.1	RES, 0.1, 1%, 0.1 W, AEC-Q200 Grade 1, 0603	0603	ERJ-L03KF10CV	Panasonic
SH-J1	1	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
TP6, TP7, TP8, TP9	4		Terminal, Turret, TH, Double	Keystone1573-2	1573-2	Keystone
U1	1		Analog Front-End for Power Monitoring, Control and Protection, PAG0064A (TQFP-64)	PAG0064A	ADS131E08IPAGR	Texas Instruments
U2	1		36V, 1A, 4.17µVRMS, RF low-dropout (LDO) voltage regulator 20-VQFN -40℃ to 125℃	VQFN20	TPS7A4700RGWR	Texas Instruments
U4	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm
U5	1		Automotive Qualified Precision, Zero-Crossover, 20MHz, 0.9pA Ib, RRIO, CMOS Operational Amplifier, DBV0005A (SOT-23-5)	DBV0005A	OPA320AQDBVRQ1	Texas Instruments
C47	0	10uF	CAP, CERM, 10uF, 25V, +/- 10%, X7R, 1206_190	1206_190	C1206C106K3RACTU	Kemet
C48	0	22uF	CAP, CERM, 22µF, 25V,+/- 10%, X7R, 1210	1210	CL32B226KAJNFNE	Samsung Electro-Mechanics
C49	0	1uF	CAP, CERM, 1uF, 25V, +/- 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet

Table 5-1. ADS131E08EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J9	0		Header, 100mil, 4x2, Gold, TH	4x2 Header	TSW-104-07-G-D	Samtec
JP1, JP3	0		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
R12, R43	0	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
R40	0	1	RES, 1.0, 5%, 0.4 W, AEC-Q200 Grade 0, 0805	0805	ESR10EZPJ1R0	Rohm
R47	0	0.047	RES, 0.047, 1%, 0.1 W, AEC-Q200 Grade 1, 0603	0603	ERJ-L03KF47MV	Panasonic
R48	0	120k	RES, 120 k, 0.1%, 0.1 W, 0603	0603	RG1608P-124-B-T5	Susumu Co Ltd
R52	0	100k	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
R89	0	10	RES, 10.0, 1%, 0.25 W, 0603	0603	CRCW060310R0FKEAHP	Vishay-Dale
TP2, TP10	0		Test Point, Miniature, SMT	Test point_Keystone_Miniature	5015	Keystone
U3	0		High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	DGK0008A	REF6241IDGKR	Texas Instruments

6 Additional Information

6.1 Trademarks

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STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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