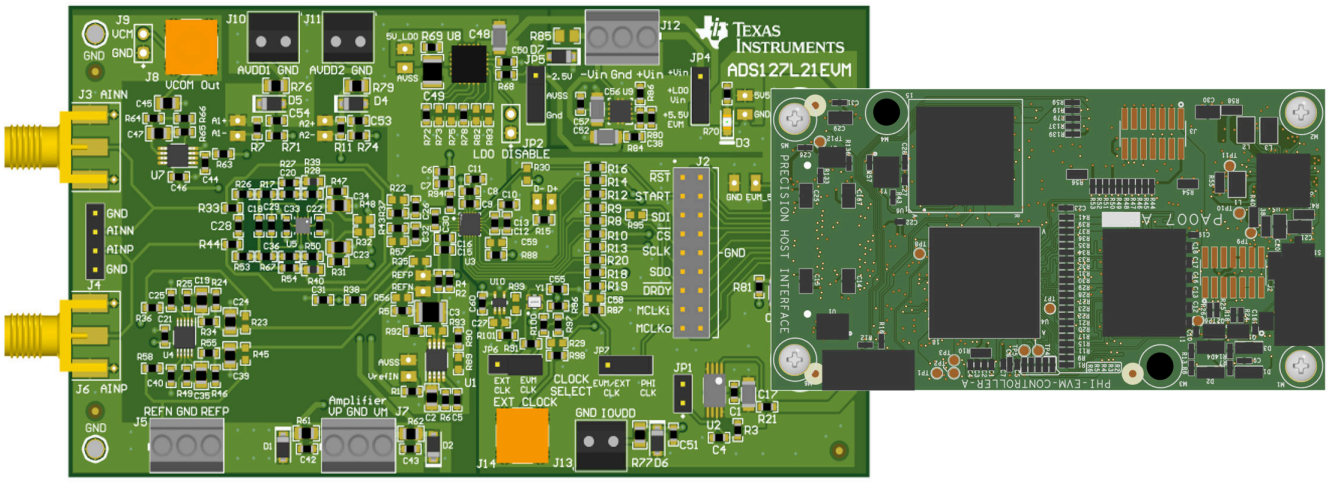
User's Guide

ADS127L21EVM-PDK Evaluation Module

ABSTRACT



This user's guide describes the characteristics, operation, and use of the ADS127L21 evaluation module (EVM). This kit is an evaluation platform for the ADS127L21, which is a 24-bit, high-speed, wide-bandwidth, delta-sigma (ΔΣ) analog-to-digital converter (ADC). The ADS127L21 offers excellent ac and dc performance, along with multiple internal digital filter options including a fully programmable finite impulse response (FIR) and infinite impulse response (IIR) filter, making the device useful for a wide variety of data acquisition applications. The ADS127L21EVM eases the evaluation of the device with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS127L21EVM.

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1 EVM Overview

The ADS127L21EVM is a platform for evaluating the performance of the ADS127L21, which is a 24-bit, high-speed, wide-bandwidth ΔΣ ADC. The evaluation kit includes the ADS127L21EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over the USB for data capture, configuration, and analysis. The ADS127L21EVM board includes the ADS127L21 ADC and all the peripheral analog circuits and components required to extract optimum performance from the ADC. The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS127L21
- Supplies power to all active circuitry on the ADS127L21EVM board

1.1 ADS127L21 EVM Kit

The ADS127L21 evaluation module kit includes the following features (Figure 1-1):

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS127L21 ADC.
- USB powered—no external power supply is required.
- The PHI controller that provides a convenient communication interface to the ADS127L21 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output.
- Windows® 10 operating systems.
- Easy-to-use evaluation software for 64-bit Microsoft® Windows®.
- The software suite includes graphical tools for data capture, histogram analysis, spectral analysis, and custom configuration of the programmable digital filters. This suite also has a provision for exporting data to a text file for post-processing.

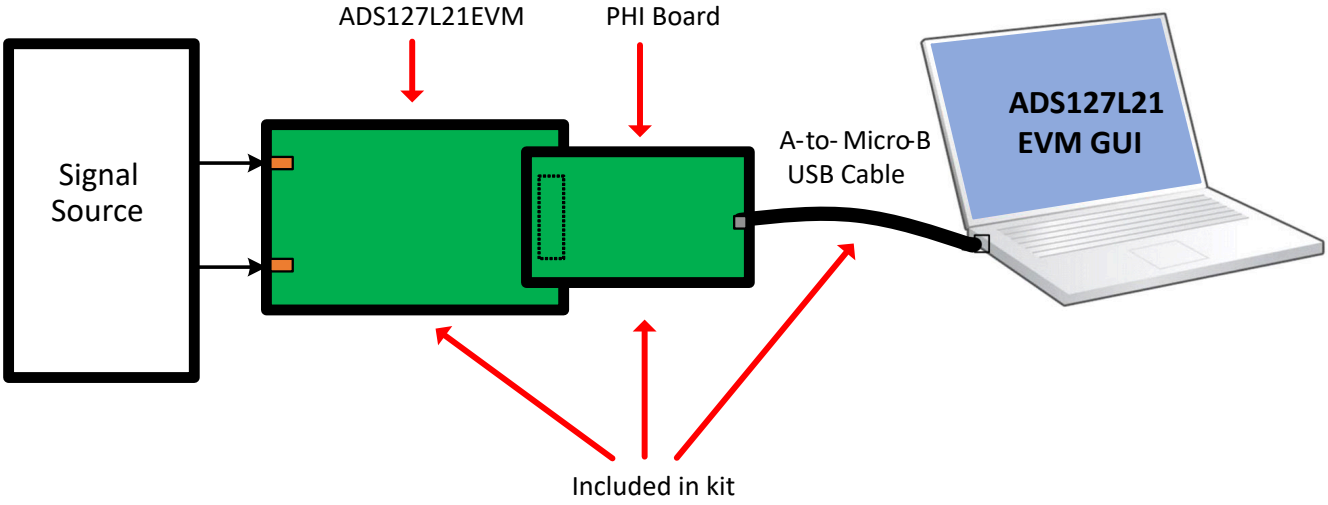

Figure 1-1. System Connection for Evaluation

1.2 ADS127L21EVM Board

The ADS127L21EVM board includes the following features:

- External signal source from differential pair subminiature version A (SMA) connectors
- Options to use external analog and digital power supplies
- Serial interface header for easy connection to the PHI controller
- Pin connections to monitor digital signals with a logic analyzer
- Onboard ultra-low noise, low-dropout (LDO) regulator for excellent 5-V, single-supply regulation of all analog circuits

1.3 ADS127L21EVM-PDK-GUI Unsupported Features

The following features of the ADS127L21 device are currently not supported in the ADS127L21 EVM GUI, but will be on a future version of the software. To provide proper operation of the EVM, do not modify the corresponding register settings from the default values.

- CONFIG2_REG; bits 5:4, START_MODE, default 00b, only start and stop conversions are supported
- CONFIG3_REG; bit 2, SPI_CRC, default 0b, CRC not supported
- CONFIG3_REG; bit 0, STATUS, default 0b, status readback not supported
- FILTER3_REG; bits 1:0, DATA_MODE, default 01b, SDO is dual function

1.4 Related Documentation

Table 1-1 shows the related documentation from Texas Instruments.

Table 1-1. Related Documentation

Document	Literature Number
ADS127L21 product data sheet	SBASAK4

2 Analog Interface

The ADS127L21EVM is designed for easy interfacing with analog sources. This section covers the details of the front-end circuit, including jumper configuration for different input test signals and board connectors for signal sources.

2.1 EVM Analog Input Options

For best performance, differential analog input signals can be connected through the SMA connectors (J3 and J6). Header J4 can also directly connect inputs for dc measurements, or where best ac performance is not needed. For single-ended inputs, header J4 can connect AINN or AINP to GND. Then use either J3 or J6 as the single-ended input. The input driver circuit uses the THS4561 fully-differential amplifier in a unity-gain, second-order, low-pass filter configuration with a single-pole RC filter at the output. Multiple passive components around the amplifier are intentionally left uninstalled to give users the flexibility to customize the input drive circuit for their specific application.

When differential inputs are connected to the SMA connectors (J3 and J6), make sure header J4 does not have any connection to pins 1 or 4.

2.2 ADC Connections and Decoupling

The circuit shown in Figure 2-1 shows all connections to the ADS127L21 data converter (U3). Each power-supply connection has a 1-µF and 100-nF decoupling capacitor. Make sure these capacitors are physically close to the device and have a good connection to the GND plane. The supply connections also have a series 0.1-Ω resistor. The purpose of this component is to facilitate current measurement for the ADC. Also, each digital input has a 10-Ω series resistor. These resistors smooth the edges of the digital signals to provide minimal overshoot and ringing. Although not strictly required, these components can be included in the final design to improve digital signal integrity.

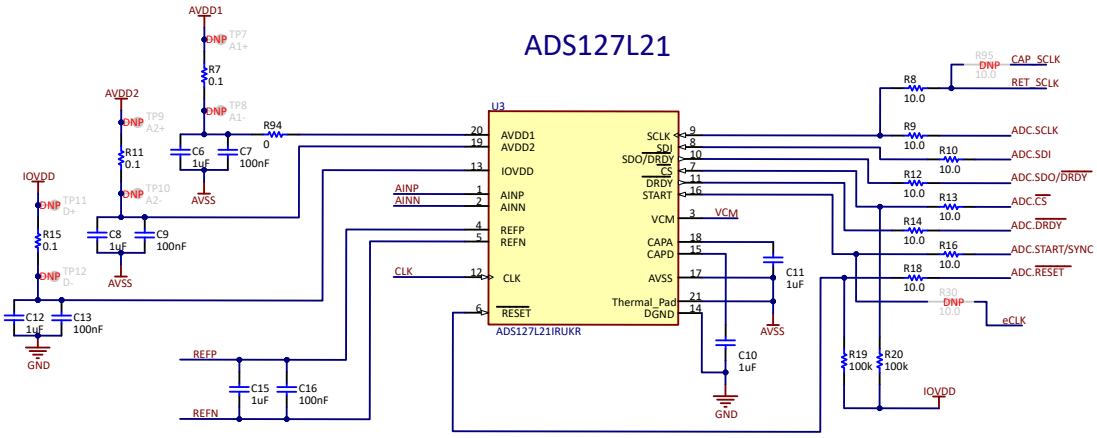

Figure 2-1. ADS127L21 Connections and Decoupling

2.3 ADC Input Drive Amplifiers

The circuit shown in Figure 2-2 is the fully differential amplifier (THS4561) that drives the ADC. The input applied to J3 and J6 must be a low-distortion differential signal. The common-mode output for the amplifier is controlled by pin 7 on U5 (VOCM). The common-mode signal is set by the data converter (pin 3, VCM). The output of the amplifier connects to an RC filter that connects to the ADC input (R37, R43, C30, C26, and C32). The amplified configuration has several do not populate (DNP) components. These components provide flexibility, but are not required for good performance. The amplifier power supplies are connected by default to the AVDD and AVSS supplies that are also used for the ADC. The amplifier supplies can be changed to external supplies VP and VM by removing the 0-Ω resistors that connect to AVDD1 and AVSS (R31 and R47), and installing these resistors to connect VP and VM (R32 and R48).

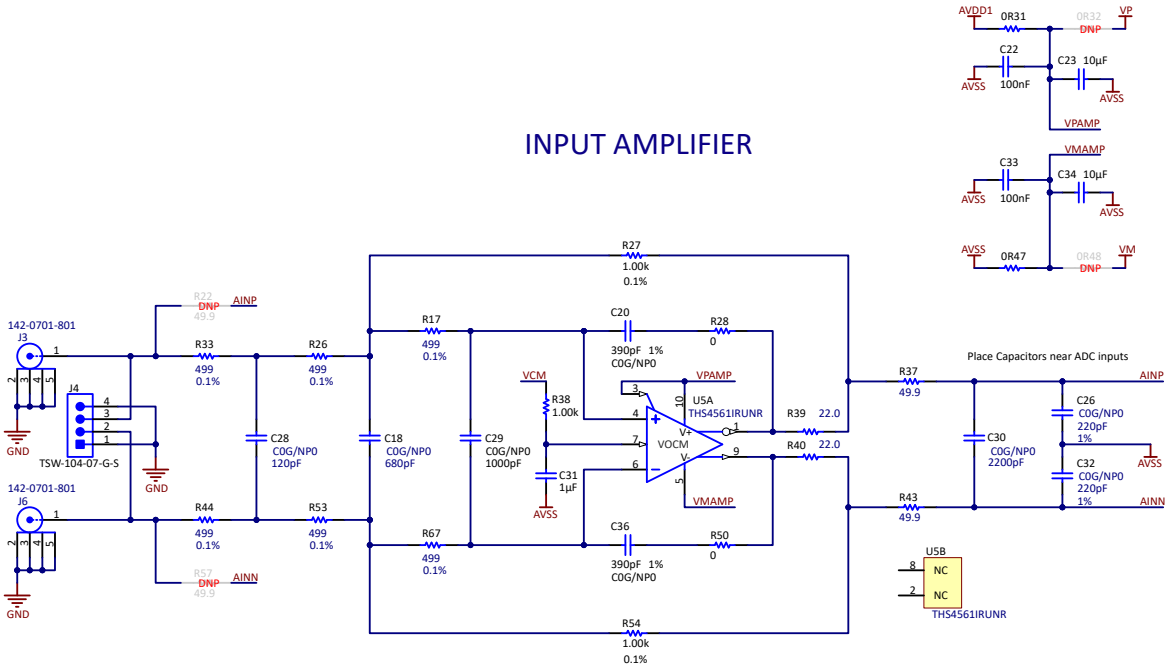

Figure 2-2. ADC Drive Amplifier

2.4 VCOM Buffer

The circuit shown in Figure 2-3 buffers the VCM signal from the ADC and connects this signal to the J8 SMA connector. This process is useful if the VCOM signal must be connected to an external piece of test equipment to set the common-mode voltage. A common use case is to connect this signal to the Audio Precision SYS-2722 to set the signal generators common-mode output. This circuit is not required in the end application and is only used for testing purposes.

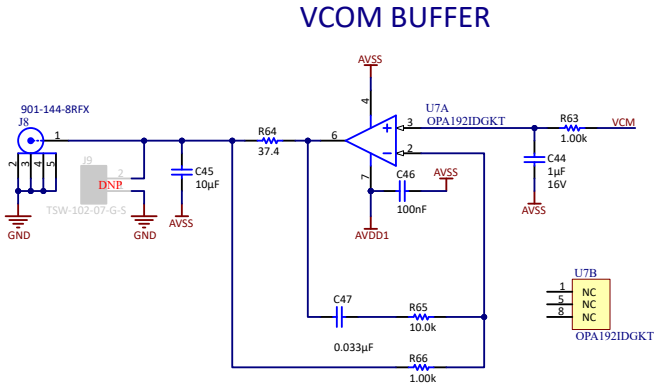

Figure 2-3. VCOM Buffer

2.5 Onboard Voltage Reference

Figure 2-4 shows the REF6225 configuration. This reference includes an integrated wide bandwidth buffer that makes the REF6225 designed for driving the switched-capacitor input to the ADS127L21. There are also unpopulated 0-Ω resistors that allow use of the REF70 reference if higher DC precision is needed. The EVM provides a buffer and connections if a different voltage reference is chosen. This reference is sufficient to meet the ADS127L21 data sheet specifications for dynamic performance.

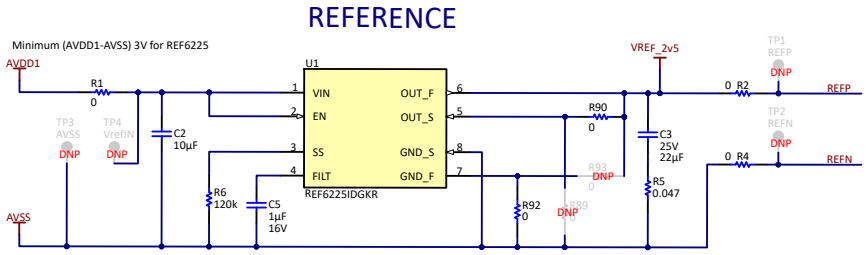

Figure 2-4. Onboard Voltage Reference

2.6 External Voltage Reference

Figure 2-5 shows a reference buffer that allows connection of an external voltage reference to connector J5. This circuit and connections are not required if the onboard voltage reference is used (see Figure 2-4). This amplifier was selected for low voltage offset and low offset drift. The amplifier topology is designed to drive capacitive loads. For information on this topology, see the Op Amp Stability Videos in TI Precision Labs.

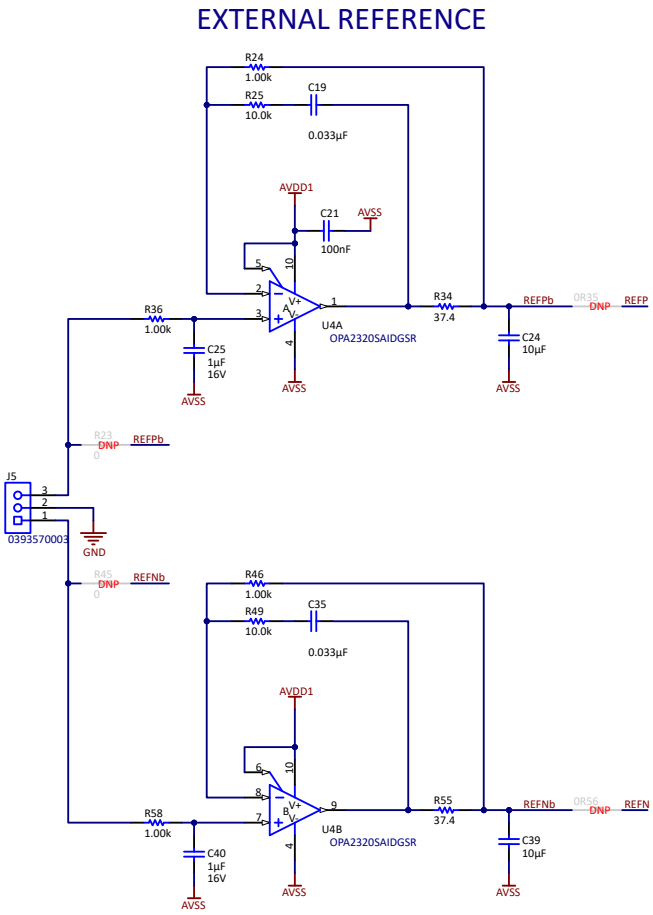

Figure 2-5. External Reference Connection and Buffer

2.7 Clock Tree

Figure 2-6 shows the different clock options for the ADS127L21EVM. The default position for jumper (JP7) 2-3 routes the PHI digital controller board clock to the CLK pin on the ADS127L21 (U3). If the ADS127L21EVM is used without the PHI board, then change the shunt on jumper (JP7) to position 1-2 to directly route the local clock to ADS127L21 (U3). Jumper (JP6) 2-3 enables the local 32.768-MHz oscillator (Y1) on the ADS127L21EVM board, or if inactive (JP6) 1-2, allows an external clock supplied on the SMA connector (J14). The default position for jumper (JP6) 2-3 selects the local 32.768-MHz oscillator (Y1). The ADS127L21EVM-PDK-GUI software by default uses the 32.768-MHz (Y1) oscillator, but can also select the 24-MHz PHI clock source. If an external clock source is used, jumper (JP6) 1-2 position, use a CMOS square-wave signal with an amplitude equal to IOVDD (2.5 V when using the PHI board) and a frequency within the specified range of the ADS127L21.

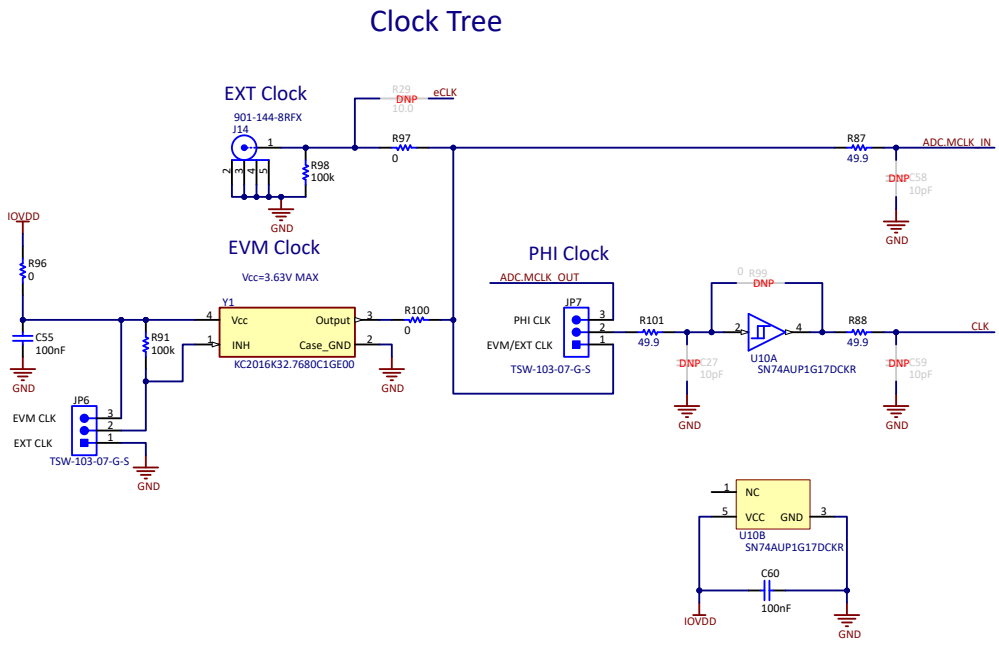

Figure 2-6. Clock Tree

3 Digital Interface

As discussed in Section 1, the EVM interfaces with the PHI and communicates with the computer over the USB. There are two devices on the EVM with which the PHI communicates: the ADS127L21 ADC (over SPI) and the EEPROM (over I^2C). The electrically erasable programmable read-only memory (EEPROM) comes preprogrammed with the information required to configure and initialize the ADS127L21 platform. When the hardware is initialized, the EEPROM is no longer used.

3.1 Serial Interface

Figure 3-1 shows the digital connections between the ADS127L21EVM and the PHI. The ADS127L21 ADC uses SPI serial communication in mode 1 (CPOL = 0, CPHA = 1). Because the serial clock (SCLK) frequency can be as fast as 50 MHz, the ADS127L21EVM offers 10-Ω resistors between the SPI signals to aid with signal integrity. Typically, in high-speed SPI communication, fast signal edges can cause overshoot; these 10-Ω resistors slow down the signal edges to minimize signal overshoot. J2 provides test points to measure the digital signals.

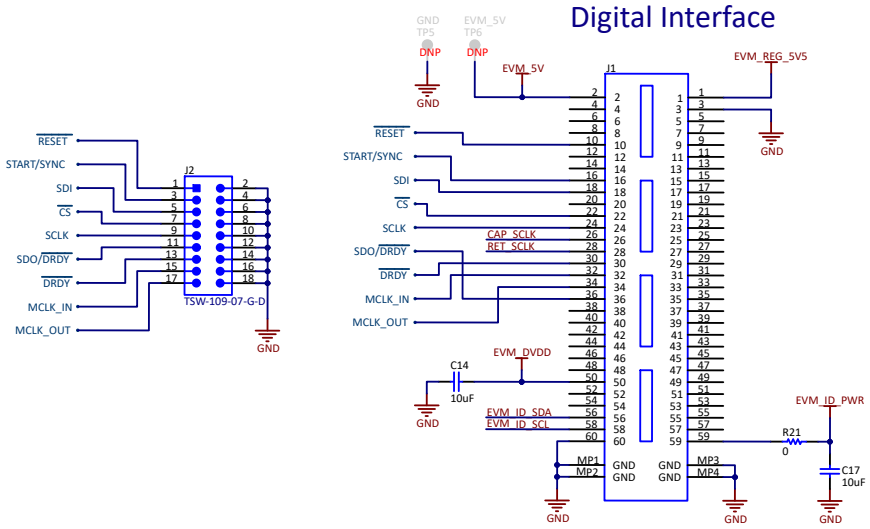

Figure 3-1. Connections to Digital Signals on PHI and Test Points

3.2 I2C bus for Onboard EEPROM

The circuit shown in Figure 3-2 is used with the EVM controller (PHI) for EVM identification. This circuit is not required by the ADS127L21 for operation. The jumper (JP1) is write protected and does not need to be changed for EVM operation.

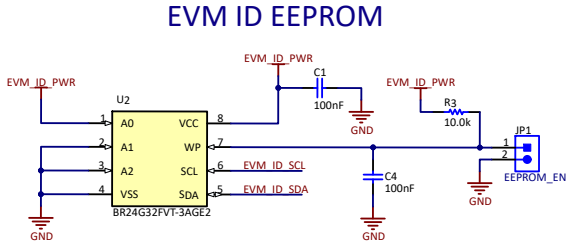

Figure 3-2. EEPROM for EVM ID

4 Power Supplies

The default state of the EVM is that all power supplies are generated using the USB power from the PHI controller. This section shows how external power connections can be made and how the default configuration for AVDD is generated with a 5-V low-dropout regulator (LDO).

4.1 Power Connection and Configuration

Figure 4-1 shows connections to external supplies for the amplifier, reference, and data converter. The default state of the EVM is that the power is provided by the PHI digital controller board via the USB port. The external power connections can be used in cases where the PHI does not provide the needed voltage. For example, the PHI does not provide negative voltages, so if a negative AVSS is needed an external power supply is required. To use the external power connections for AVDD and IOVDD, remove the 0-Ω resistor connections (R71, R74, and R81). Connector J12 can optionally be used to supply power to the onboard 5-V and –2.5-V regulators. In this case, the allowable voltage range for –VinExt is –15.5 V < –VinExt < –3.5 V and +VinExt is 6 V < +VinExt < 15.5 V.

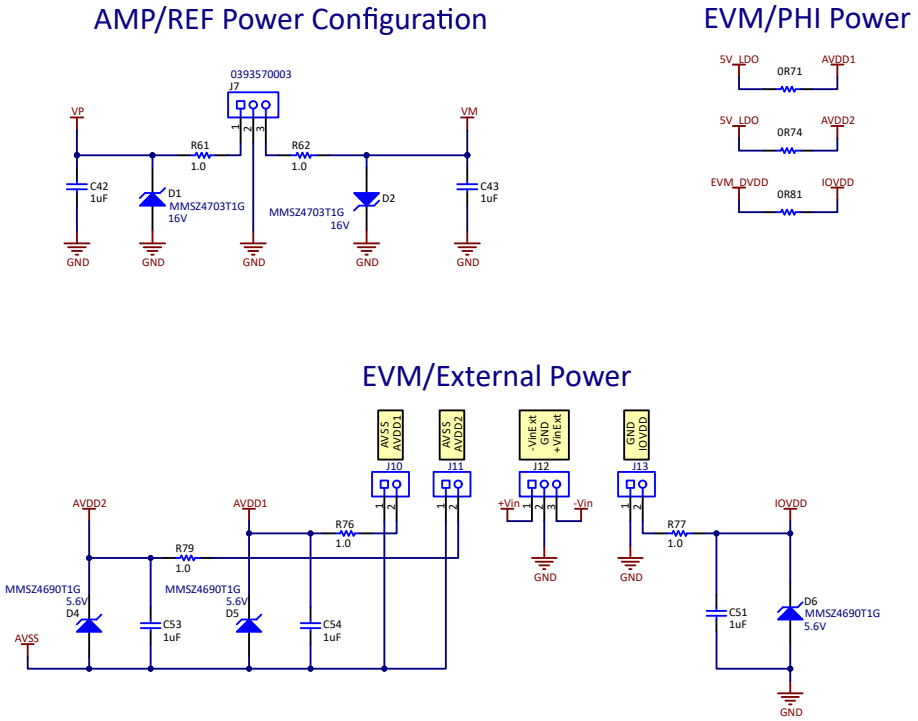

Figure 4-1. Power Connection and Configuration

4.2 Low Dropout Regulator (LDO)

Figure 4-2 shows how the 5.5-V power from the PHI is regulated to 5 V using a low-noise TPS7A47 LDO. By default, the shunt on (JP4) 1-2 routes 5.5 V from the PHI to the LDO. The 5-V LDO can also be supplied by external power on J12 by moving the shunt on (JP4) to position 2-3. The 5-V LDO output is used for the AVDD connections and can be reprogrammed to different output voltages using R72, R73, R75, R78, R82, and R83. An additional LDO generates –2.5 V for AVSS, using the low-noise TPS7A30 LDO. This LDO is only supplied by external power on J12. By default, AVSS is connected to GND with a shunt on (JP5) 1-2. If AVSS must be set to –2.5 V, then connect an external negative supply to J12 and move the shunt on (JP5) to position 2-3.

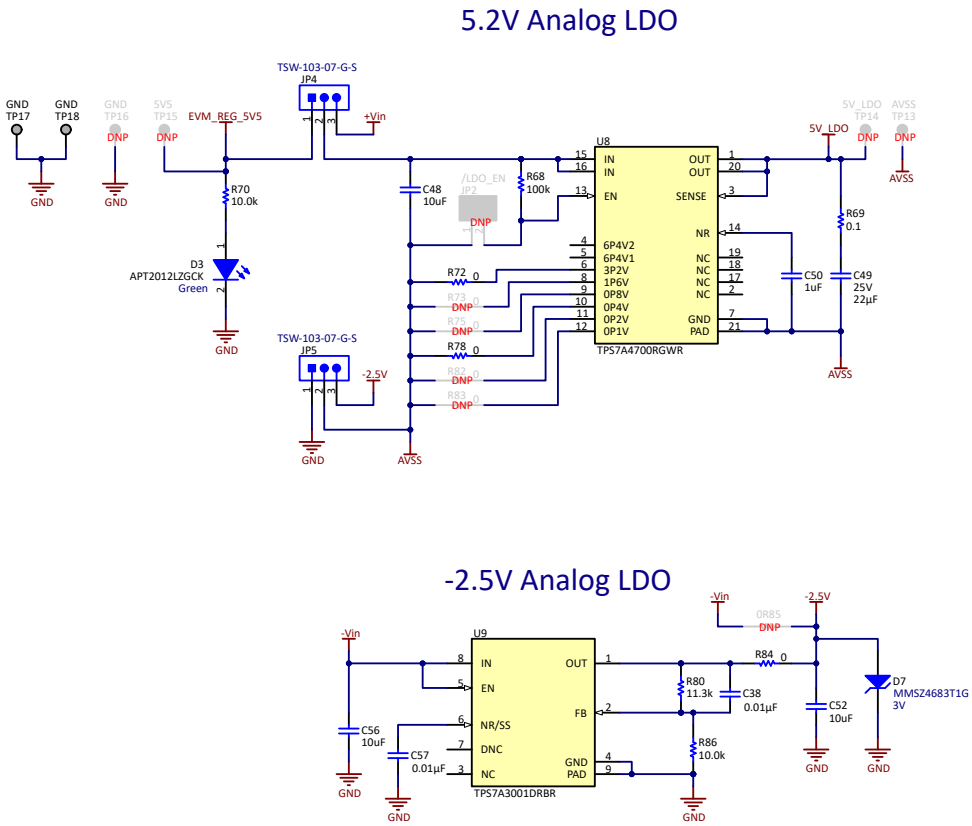

Figure 4-2. LDO Regulators for 5 V and –2.5 V

5 ADS127L21 EVM Software Installation

Download the latest version of the EVM GUI installer from the *Tools and Software* folder of the ADS127L21EVM and run the GUI installer to install the EVM GUI software on your computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message can possibly appear or the installer.exe file can be deleted.

As shown in Figure 5-1, accept the license agreements and follow the on-screen instructions to complete the installation.

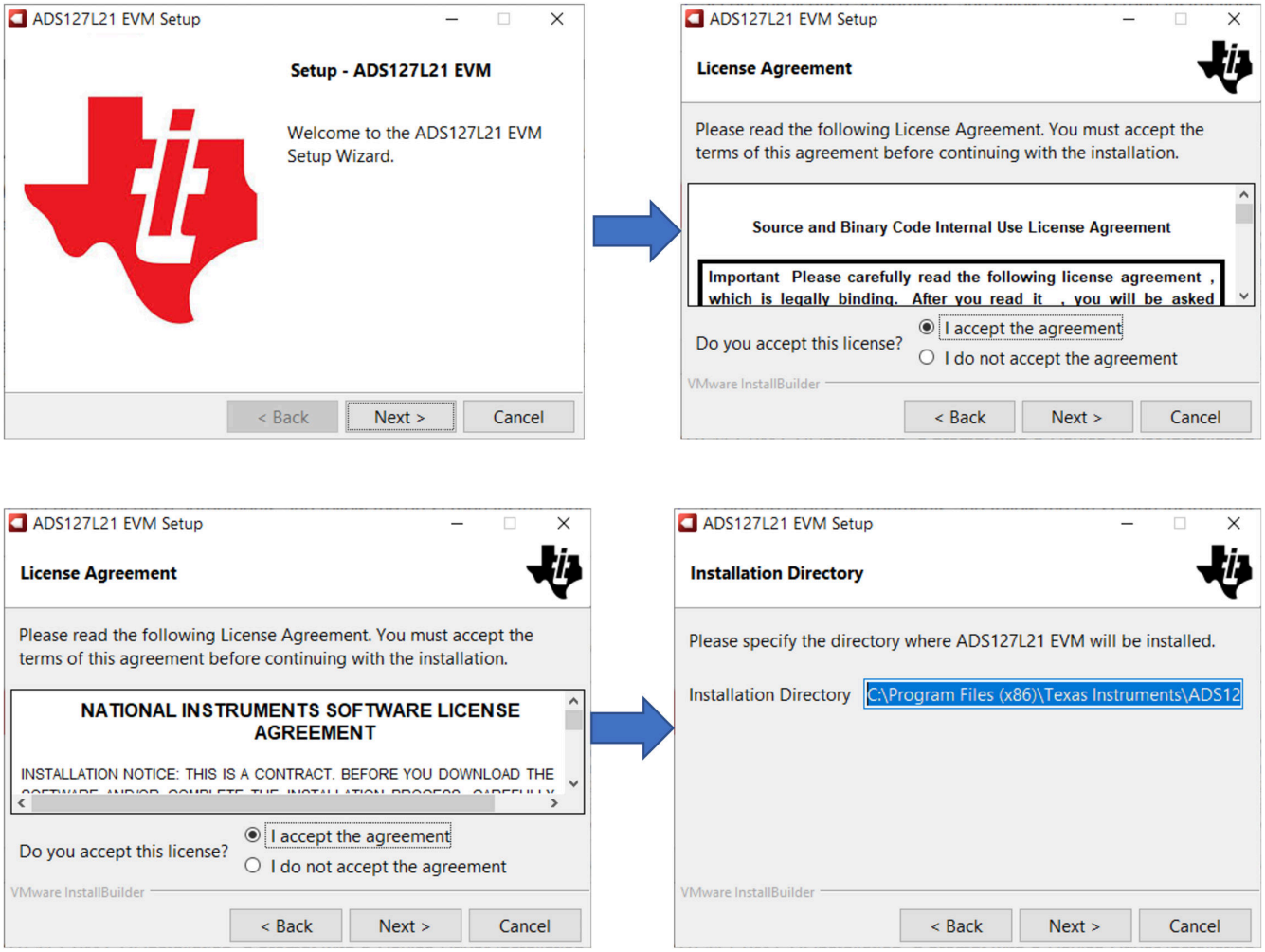

Figure 5-1. Software Installation and Prompts

As part of the ADS127L21 EVM GUI installation, and as shown in Figure 5-2, a prompt with a *Device Driver Installation* appears on the screen. Click **Next** to proceed.

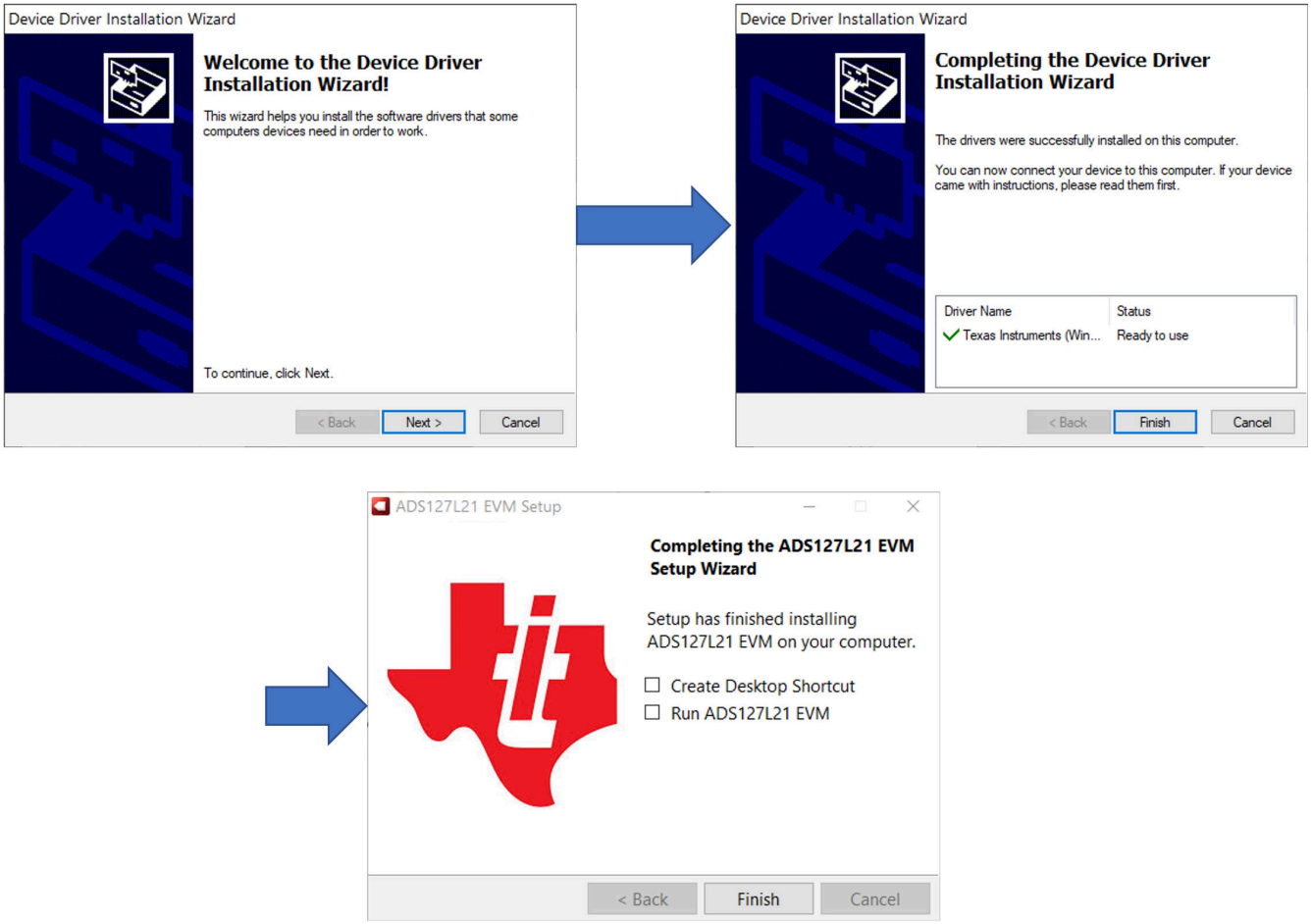

Figure 5-2. Device Driver Installation

The ADS127L21EVM requires the LabVIEW™ run-time engine and can possibly prompt for the installation of this software, as shown in Figure 5-3, if not already installed.

Figure 5-3. LabVIEW Run-Time Engine Installation

6 EVM Operation

6.1 Connecting the Hardware

Connect the EVM as shown in Figure 6-1 after installing the software:

1. Physically connect P2 of the PHI to J1 of the ADS127L21 EVM.
2. Install the screws to provide a robust connection. Connect the USB on the PHI to the computer first.
   a. LED D5 on the PHI lights up, indicating that the PHI is powered up.
   b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC; Figure 6-1 shows the resulting LED indicators.
3. Start the software GUI as shown in Figure 6-2. Notice that the LEDs blink slowly when the FPGA firmware is loaded on the PHI. This loading takes a few seconds, then the AVDD and DVDD power supplies turn on.
4. Connect the signal generator. The input range is 0 V to 5 V. A common input signal applied is a 4.9-V_{PP} signal with a 2.5-V offset. This signal is adjusted just below the full-scale range to avoid clipping.

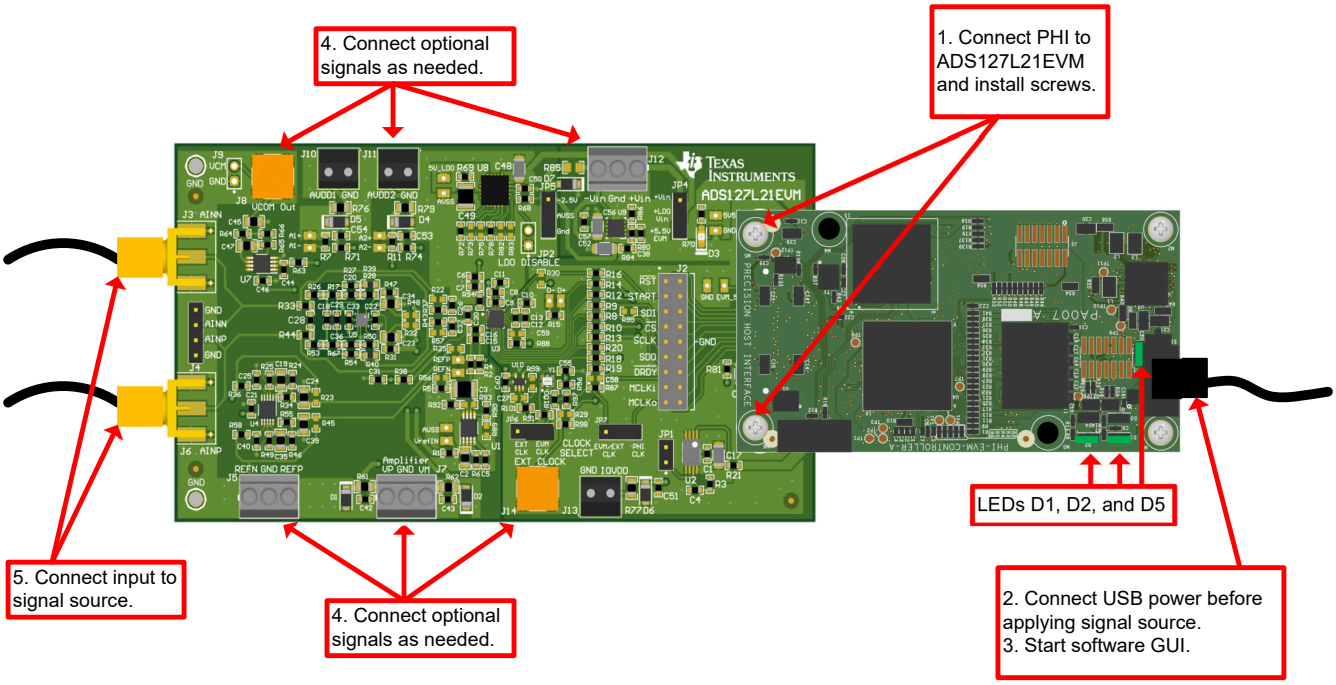

Figure 6-1. Connecting the Hardware to the ADS127L21EVM

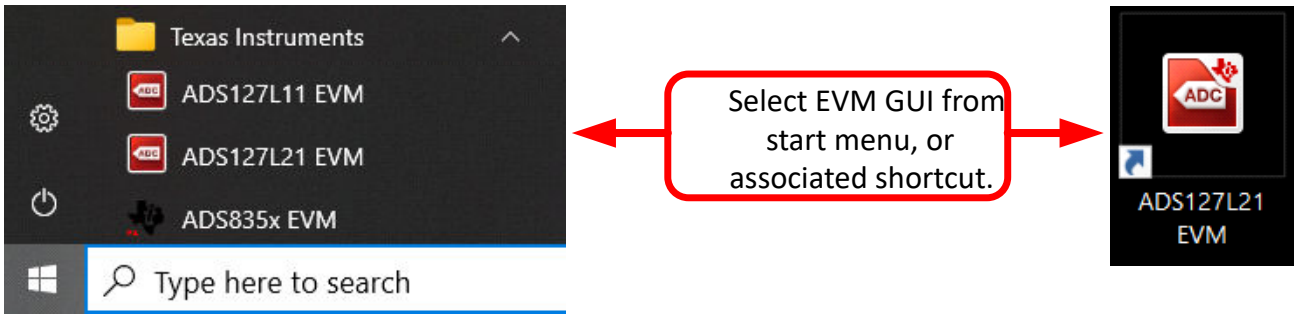

Figure 6-2. Launch the EVM GUI Software

6.2 Optional EVM Connections

Figure 6-3 shows optional connections to the power, clock, and VCM. These connections are not required for initial setup of the EVM but can be helpful to configure the EVM more closely to the end application configuration. Review the schematic and hardware sections of this document to understand how these connections are used.

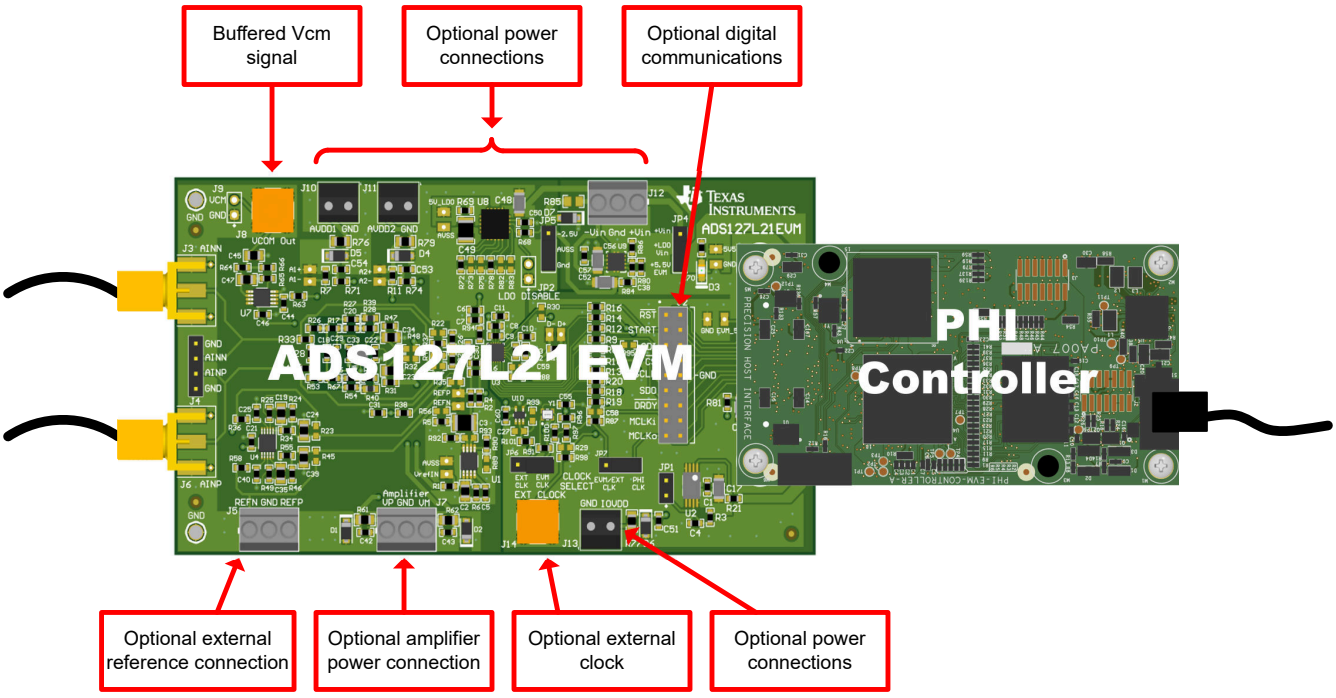

Figure 6-3. Optional EVM Connections

6.3 EVM GUI Global Settings for ADC Control

Figure 6-4 shows that the EVM global controls are located on the left-hand side of the GUI. These controls include the number of samples, MCLK (ADC external clock frequency), SCLK frequency, data rate, and others. In the upper left-hand side of the GUI is the *Pages* control that allows access to the other key pages in the GUI. Figure 6-4 also shows the ADC register settings. The registers can be used to set the different device modes (such as filter settings and power settings).

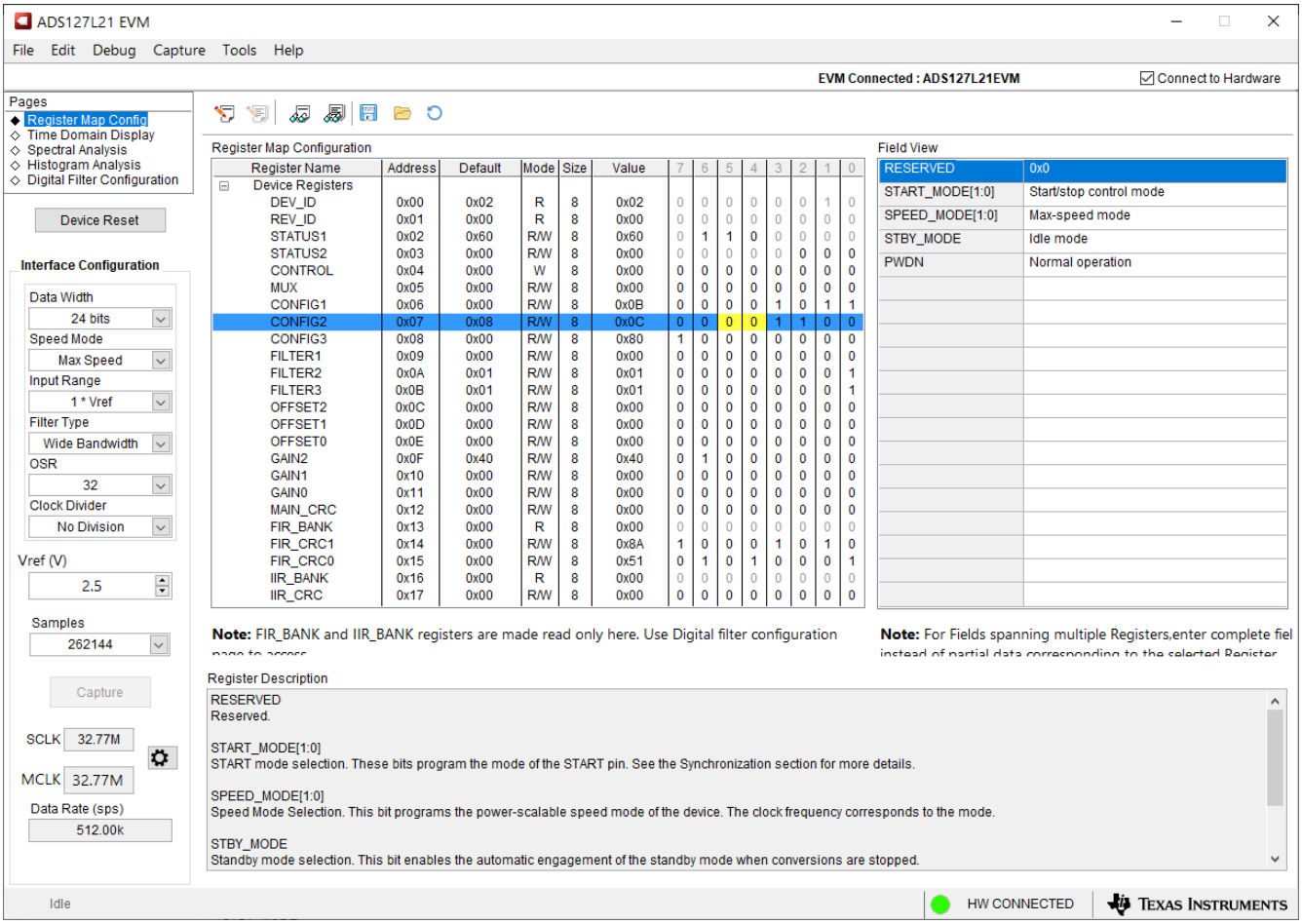

Figure 6-4. EVM GUI Global Settings for ADC Control

6.4 Time Domain Display

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits. The user can trigger a capture of the data of the selected number of samples from the ADS127L21EVM, as per the current interface mode settings indicated in Figure 6-5 by using the **Capture** button. The sample indices are on the x-axis and two y-axes show the corresponding output codes and the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the analysis tools described in the subsequent sections causes calculations to be performed on the same set of data.

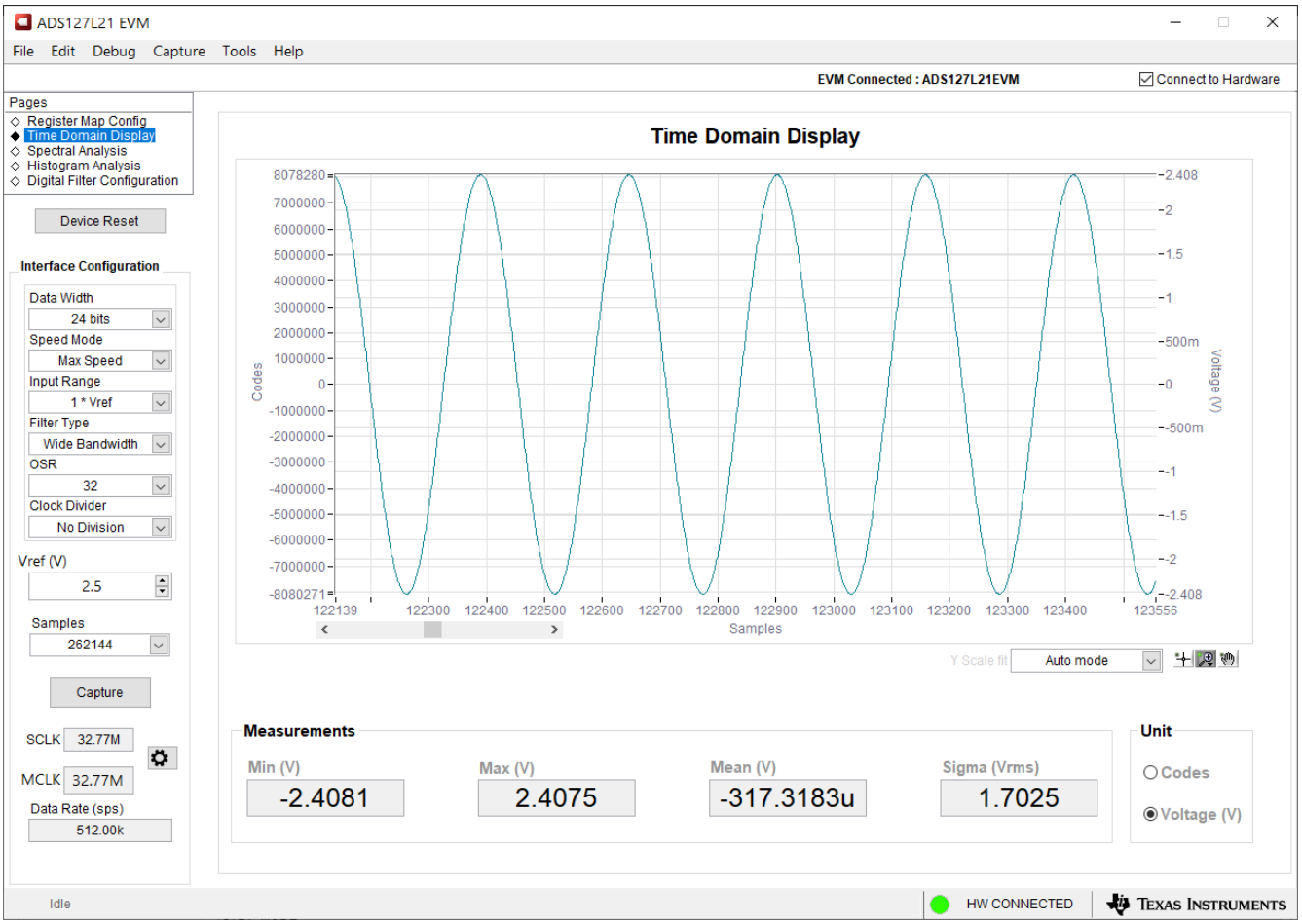

Figure 6-5. Time Domain Display

6.5 Frequency Domain Display

The spectral analysis tool, shown in Figure 6-6, is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS127L21 ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-Term Blackman-Harris window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The *None* option corresponds to not using a window (or a rectangular window) and is not recommended.

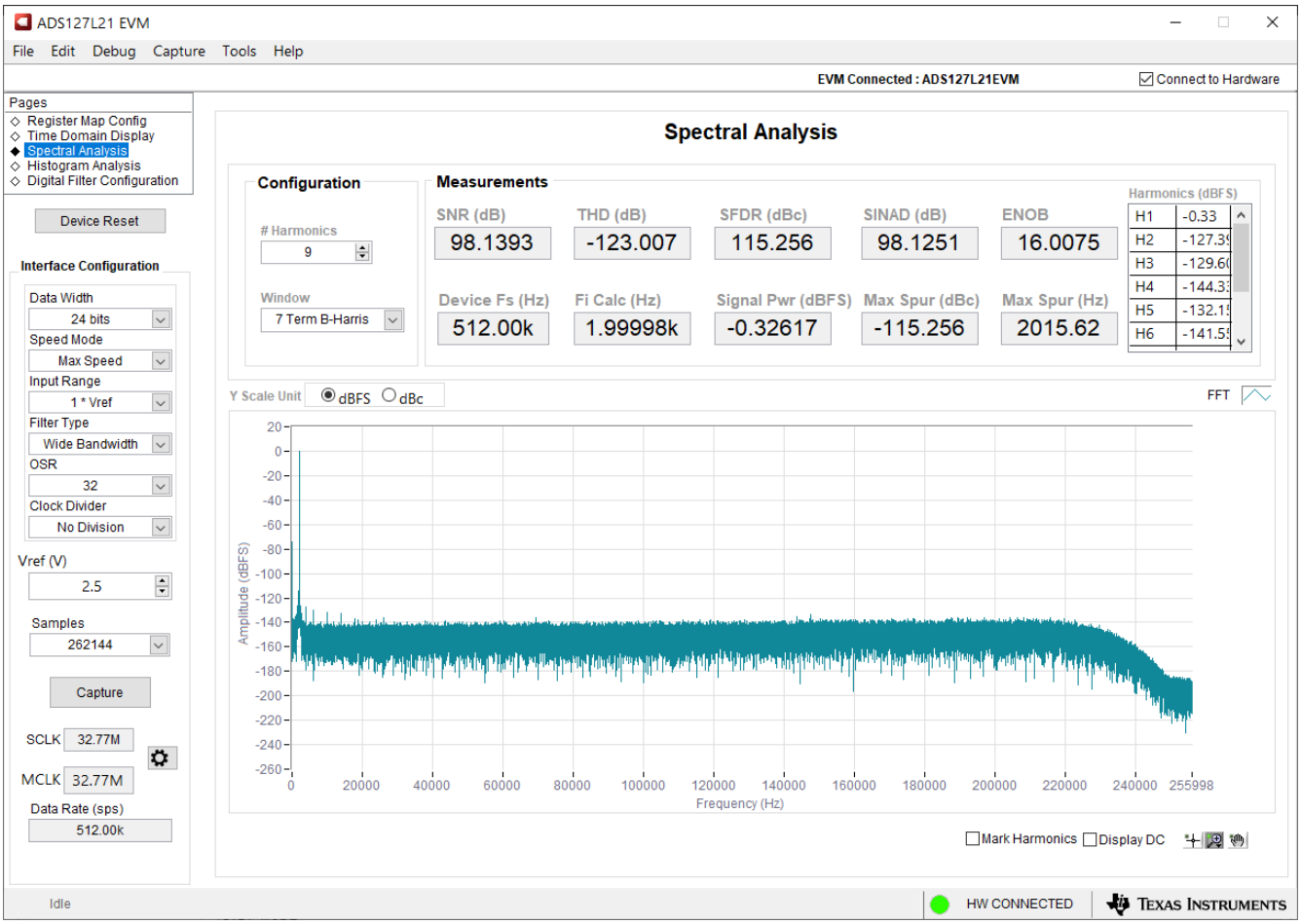

Figure 6-6. Frequency Domain Display

6.6 Histogram Display

Noise degrades ADC resolution and the histogram tool can be used to estimate effective resolution, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a dc signal. The cumulative effect of noise coupling to the ADC output from sources (such as the input drive circuits, reference drive circuit, ADC power supply, and the ADC) is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel. As shown in Figure 6-7, the histogram corresponding to a dc input is displayed on clicking the **Capture** button.

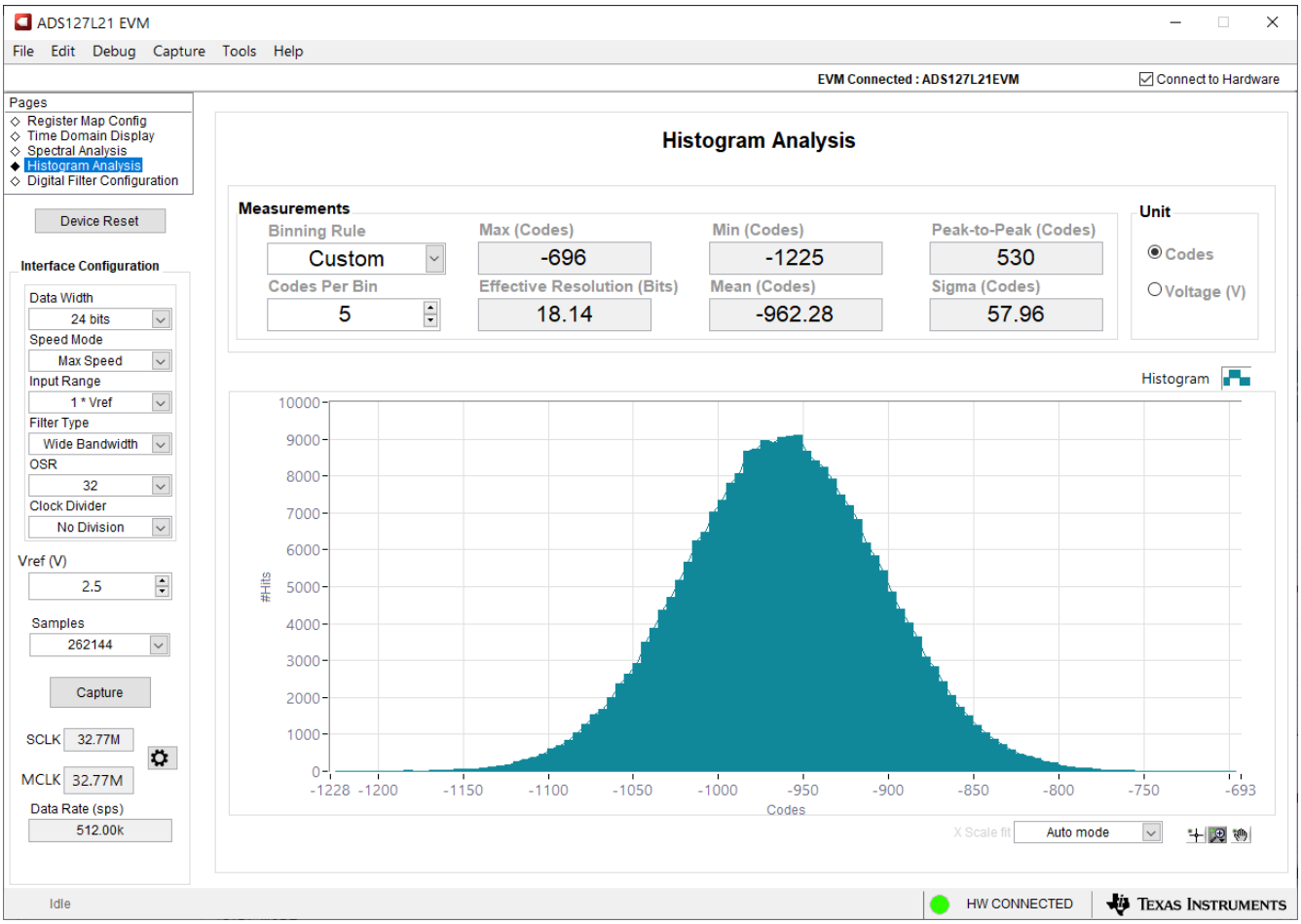

Figure 6-7. Histogram Display

6.7 Digital Filter Configuration

The *Digital Filter Configuration* page allows loading of custom digital filters into both the FIR and IIR programmable filter registers inside the ADS127L21 ADC. These filters are designed in separate tools, such as MATLAB®, and the coefficients can be viewed and transferred to the ADS127L21 filter registers. There are several options to enable or disable different filter stages inside the ADS127L21; see the ADS127L21 data sheet for details. As shown in Figure 6-8, the *Filter Sequence*, *Selection*, and *Type* can be selected. FIR and IIR coefficient files can also be loaded and the values can be viewed.

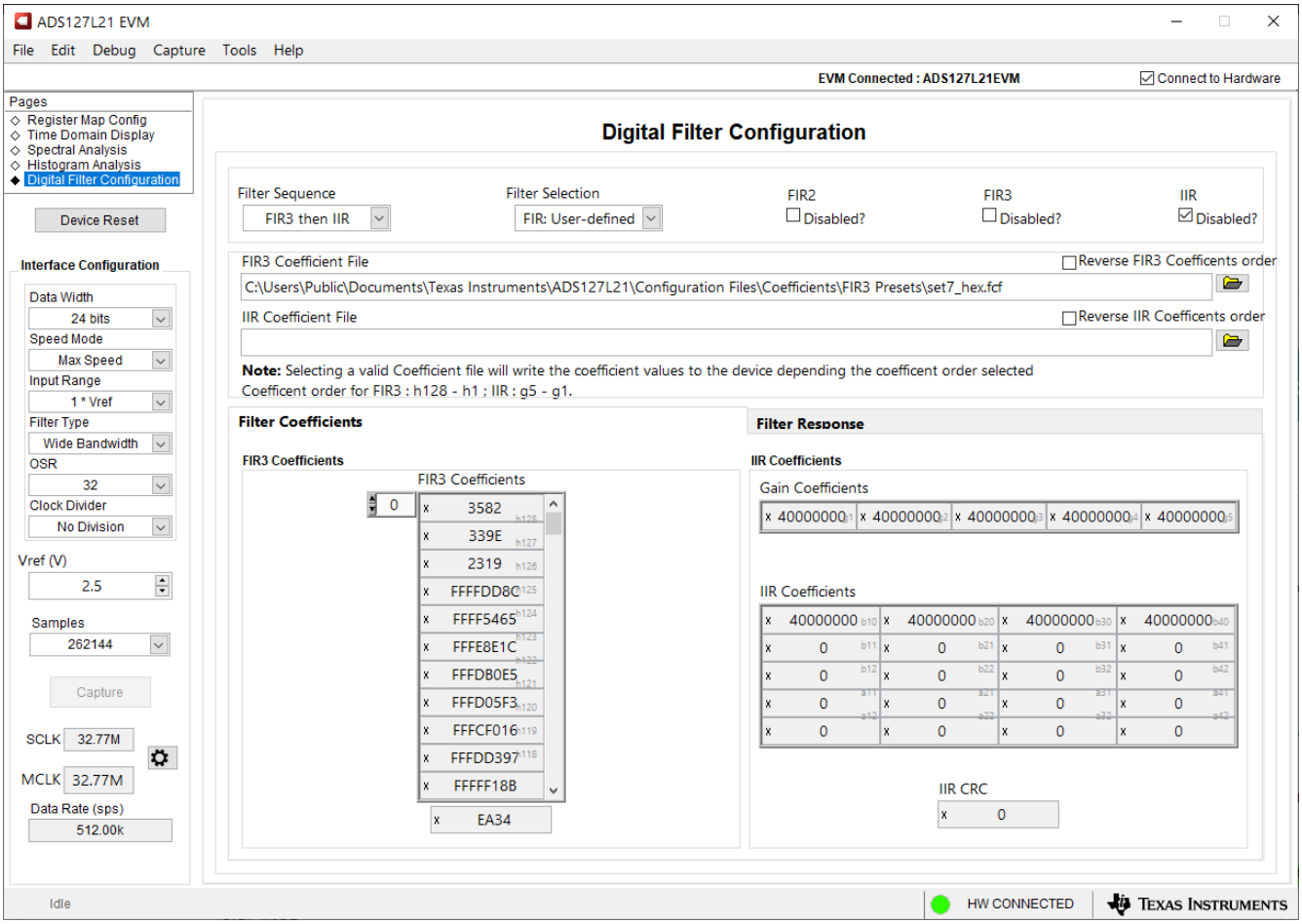

Figure 6-8. Digital Filter Configuration

6.8 Digital Filter Response

Figure 6-9 shows the user-programmed filter response. This frequency response includes all upstream filter stages in the ADS127L21. The filter response allows for a quick visual check of the desired filter.

There are several prebuilt filters available that can be downloaded to the ADS127L21. These prebuilt filter files can be used as a template for custom filter designs when using the EVM GUI to download to the ADS127L21. The prebuilt filters are copied to the C:\Users\Public\Documents\Texas Instruments\ADS127L21\Configuration Files\Coefficients\ directory when the EVM GUI is installed.

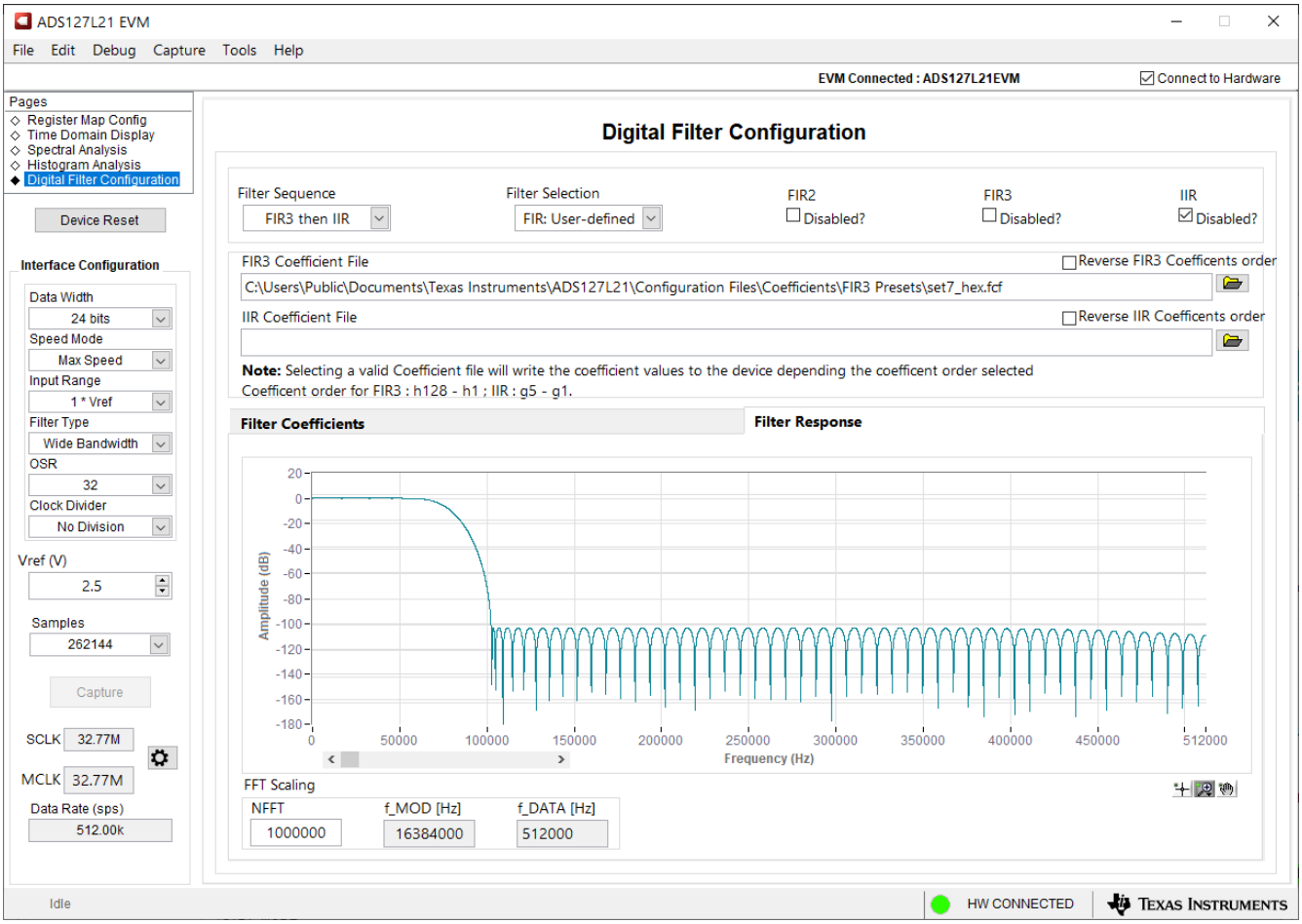

Figure 6-9. Digital Filter Response

7 Bill of Materials, Schematics, and Layout

This section contains the ADS127L21EVM bill of materials (BOM), EVM schematics, and PCB layout.

7.1 Bill of Materials

Table 7-1 lists the bill of materials (BOM) for the ADS127L21EVM.

Table 7-1. ADS127L21EVM BOM

Designator	Quantity	Value	Description	Pkg Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		DC192	Any
C1, C4, C7, C9, C13, C16, C21, C22, C33, C46, C55, C60	12	0.1 µF	CAP, CERM, 0.1 µF, 25 V, +/- 5%, X7R, 0603	0603	C0603C104J3RACTU	Kemet
C2, C23, C24, C34, C39, C45	6	10 µF	CAP, CERM, 10 µF, V,+/- 10%, X7R, 0805	0805	GRM21BR71A106KA73L	MuRata
C3, C49	2	22 µF	CAP, CERM, 22 µF, 25 V,+/- 10%, X7R, 1210	1210	CL32B226KAJNFNE	Samsung Electro-Mechanics
C5, C25, C31, C40, C44	5	1 µF	CAP, CERM, 1 µF, 16 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1C105K080AC	TDK
C6, C8, C10, C11, C12, C15, C42, C43, C50, C51, C53, C54	12	1 µF	CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet
C14, C17, C48, C52, C56	5	10 µF	CAP, CERM, 10 µF, 25 V, +/- 10%, X7R, 1206_190	1206_190	C1206C106K3RACTU	Kemet
C18	1	680 pF	CAP, CERM, 680 pF, 25 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1E681JA01D	MuRata
C19, C35, C47	3	0.033 µF	CAP, CERM, 0.033 µF, 50 V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0805	0805	CGA4J2C0G1H333J125AA	TDK
C20, C36	2	390 pF	CAP, CERM, 390 pF, 50 V, +/- 1%, C0G/NP0, 0603	0603	CC0603FRNPO9BN391	Yageo America
C26, C32	2	220 pF	CAP, CERM, 220 pF, 50 V, +/- 1%, C0G/NP0, 0603	0603	06035A221FAT2A	AVX
C28	1	120 pF	CAP, CERM, 120 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H121JA01D	MuRata
C29	1	1000 pF	CAP, CERM, 1000 pF, 25 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1E102JA01D	MuRata

Table 7-1. ADS127L21EVM BOM (continued)

Designator	Quantity	Value	Description	Pkg Reference	Part Number	Manufacturer
C30	1	2200 pF	CAP, CERM, 2200 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H222JA01D	MuRata
C38, C57	2	0.01 µF	CAP, CERM, 0.01 µF, 25 V,+/- 1%, C0G/NP0, 0603	0603	C0603C103F3GACTU	Kemet
D1, D2	2	16 V	Diode, Zener, 16 V, 500 mW, SOD-123	SOD-123	MMSZ4703T1G	ON Semiconductor
D3	1	Green	LED, Green, SMD	LED_0805	APT2012LZGCK	Kingbright
D4, D5, D6	3	5.6 V	Diode, Zener, 5.6 V, 500 mW, SOD-123	SOD-123	MMSZ4690T1G	ON Semiconductor
D7	1	3 V	Diode, Zener, 3 V, 500 mW, SOD-123	SOD-123	MMSZ4683T1G	ON Semiconductor
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
H5, H6	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL
H7, H8	2		ROUND STANDOFF M3 STEEL 5 MM	ROUND STANDOFF M3 STEEL 5 MM	9774050360R	Wurth Elektronik
J1	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A	Samtec
J2	1		Header, 100mil, 9x2, Gold, TH	9x2 Header	TSW-109-07-G-D	Samtec
J3, J6	2		Connector, End launch SMA, 50 ohm, SMT	End Launch SMA	142-0701-801	Cinch Connectivity
J4	1		Header, 100mil, 4x1, Gold, TH	4x1 Header	TSW-104-07-G-S	Samtec
J5, J7, J12	3		Terminal Block, 3.5 mm, 3x1, Tin, TH	Terminal Block, 3.5 mm, 3x1, TH	393570003	Molex
J8, J14	2		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF
J10, J11, J13	3		Terminal Block, 3.5mm Pitch, 2x1, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
JP1	1		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
JP4, JP5, JP6, JP7	4		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
LBL1	1			PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady

Table 7-1. ADS127L21EVM BOM (continued)

Designator	Quantity	Value	Description	Pkg Reference	Part Number	Manufacturer
R1, R2, R4, R21, R28, R31, R47, R50, R71, R72, R74, R78, R81, R84, R90, R92, R94, R96, R97, R100	20	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
R3, R25, R49, R65, R70, R86	6	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R5	1	0.047	RES, 0.047, 1%, 0.1 W, AEC-Q200 Grade 1, 0603	0603	ERJ-L03KF47MV	Panasonic
R6	1	120k	RES, 120 k, 0.1%, 0.1 W, 0603	0603	RG1608P-124-B-T5	Susumu Co Ltd
R7, R11, R15, R69	4	0.1	RES, 0.1, 1%, 0.1 W, AEC-Q200 Grade 1, 0603	0603	ERJ-L03KF10CV	Panasonic
R8, R9, R10, R12, R13, R14, R16, R18	8	10	RES, 10.0, 1%, 0.25 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310R0FKEAHP	Vishay-Dale
R17, R26, R33, R44, R53, R67	6	499	RES, 499, 0.1%, 0.1 W, 0603	0603	RG1608P-4990-B-T5	Susumu Co Ltd
R19, R20, R68, R91, R98	5	100k	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
R24, R36, R38, R46, R58, R63, R66	7	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
R27, R54	2	1.00k	RES, 1.00 k, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERA3AEB102V	Panasonic
R34, R55, R64	3	37.4	RES, 37.4, 1%, 0.1 W, 0603	0603	RC0603FR-0737R4L	Yageo
R37, R43, R87, R88, R101	5	49.9	RES, 49.9, 0.1%, 0.1 W, 0603	0603	RT0603BRD0749R9L	Yageo America
R39, R40	2	22	RES, 22.0, 0.1%, 0.063 W, 0603	0603	CPF0603B22RE1	TE Connectivity
R61, R62, R76, R77, R79	5	1	RES, 1.0, 5%, 0.4 W, AEC-Q200 Grade 0, 0805	0805	ESR10EZPJ1R0	Rohm
R80	1	11.3k	RES, 11.3 k, 1%, 0.1 W, 0603	0603	RC0603FR-0711K3L	Yageo

Table 7-1. ADS127L21EVM BOM (continued)

Designator	Quantity	Value	Description	Pkg Reference	Part Number	Manufacturer
SH-J1, SH-J2, SH-J3, SH-J4	4	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100 mil Shunt	SPC02SYAN	Sullins Connector Solutions
TP17, TP18	2		Terminal, Turret, TH, Double	Keystone1573-2	1573-2	Keystone
U1	1		High-Precision Voltage Reference with Integrated High-Bandwidth Buffer, DGK0008A (VSSOP-8)	DGK0008A	REF6225IDGKR	Texas Instruments
U2	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm
U3	1		512-kSPS, Wide-Bandwidth, 24-Bit, Delta-Sigma ADC	WQFN20	ADS127L21IRUKR	Texas Instruments
U4	1		Precision, 20 MHz, 0.9 pA Ib, RRIO, CMOS Operational Amplifier, DGS0010A (VSSOP-10)	DGS0010A	OPA2320SAIDGSR	Texas Instruments
U5	1		Low Power, High Supply Range, 70 MHz, Fully Differential Amplifier, RUN0010A (WQFN-10)	RUN0010A	THS4561IRUNR	Texas Instruments
U7	1		High-Voltage, Rail-to-Rail Input/Output, 5 µV, 0.2 µV/°C, Precision Operational Amplifier, DGK0008A (VSSOP-8)	DGK0008A	OPA192IDGKT	Texas Instruments
U8	1		36 V, 1 A, 4.17 µVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)	RGW0020A	TPS7A4700RGWR	Texas Instruments
U9	1		Vin -3V to -36V, -200mA, Ultra-Low-Noise, High-PSRR, Low-Dropout (LDO) Linear Regulator, DRB0008A (VSON-8)	DRB0008A	TPS7A3001DRBR	Texas Instruments
U10	1		Low-Power Single Schmitt-Trigger Buffer, DCK0005A, LARGE T&R	DCK0005A		Texas Instruments

Table 7-1. ADS127L21EVM BOM (continued)

Designator	Quantity	Value	Description	Pkg Reference	Part Number	Manufacturer
Y1	1		32.768 MHz XO (Standard) CMOS Oscillator 1.6 V ~ 3.63 V Standby (Power Down) 4-SMD, No Lead	SMT4_2MM0_1MM6	KC2016K32.7680C1GE00	Kyocera

7.2 Schematics

Figure 7-1 to Figure 7-3 illustrate the schematics for the ADS127L21EVM.

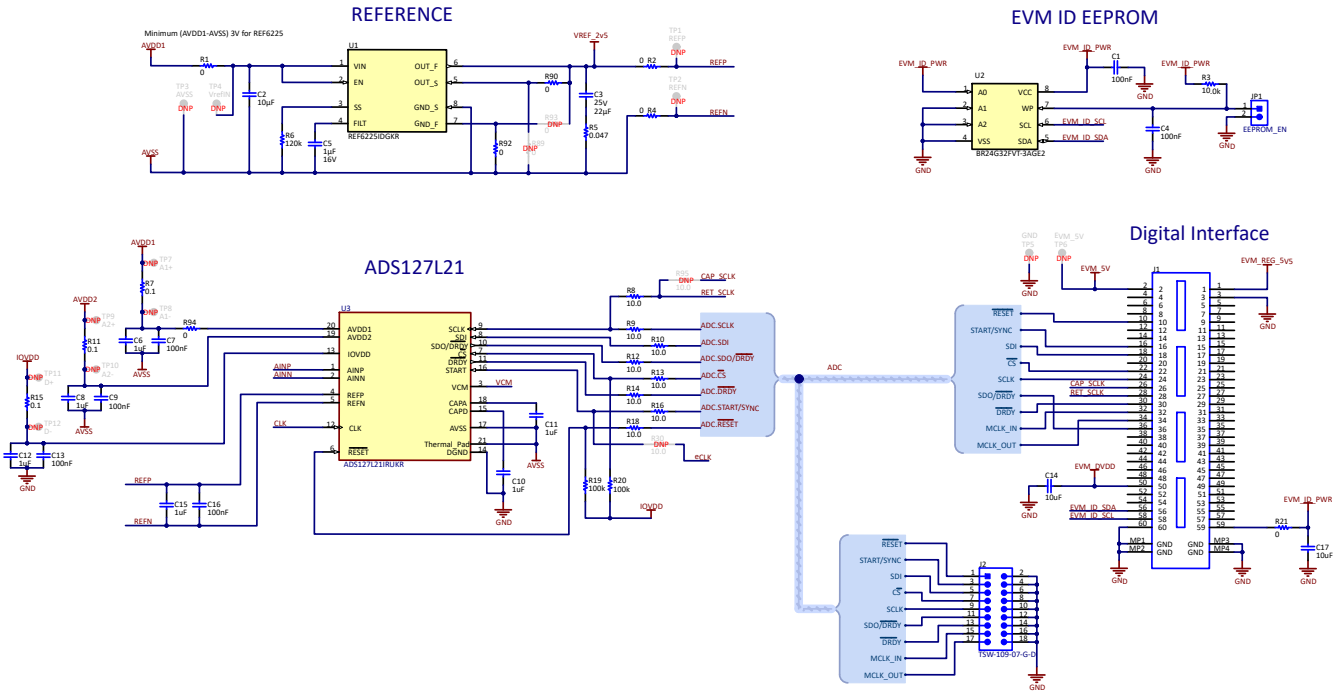

Figure 7-1. ADS127L21EVM ADC Connections and Reference Schematic

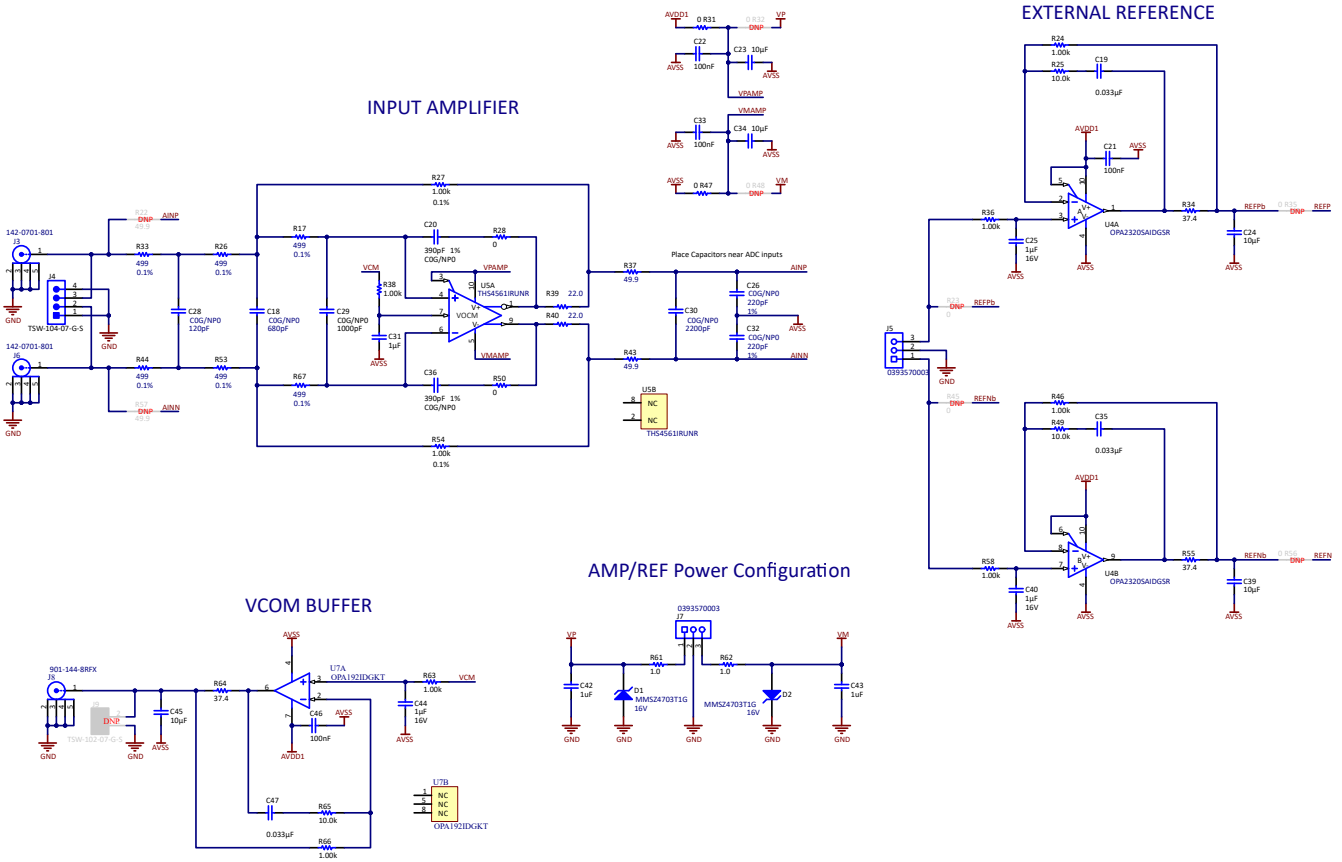

Figure 7-2. ADS127L21EVM External Reference Schematic for Input and VCOM Amplifiers

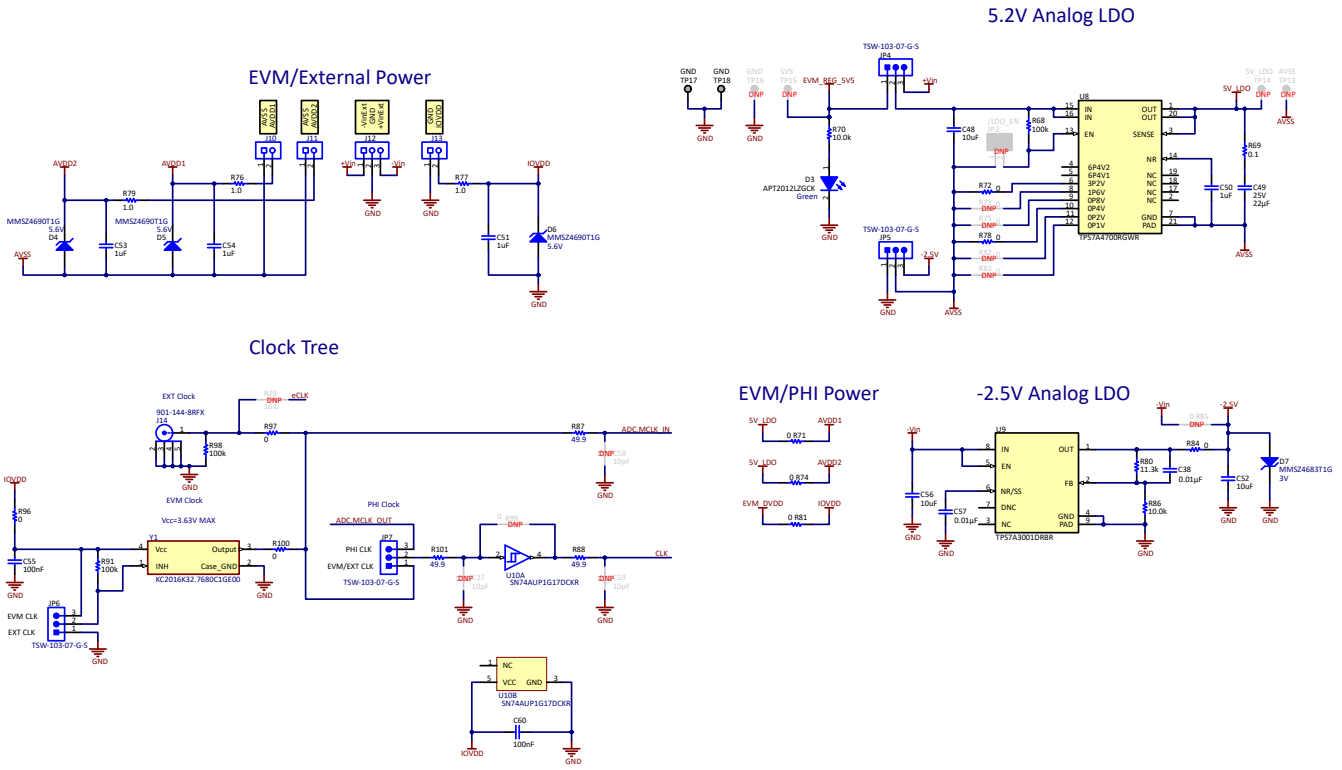

Figure 7-3. ADS127L21EVM Clock Tree and Power Schematic

7.3 Board Layout

Figure 7-4 shows the PCB layout for the ADS127L21EVM.

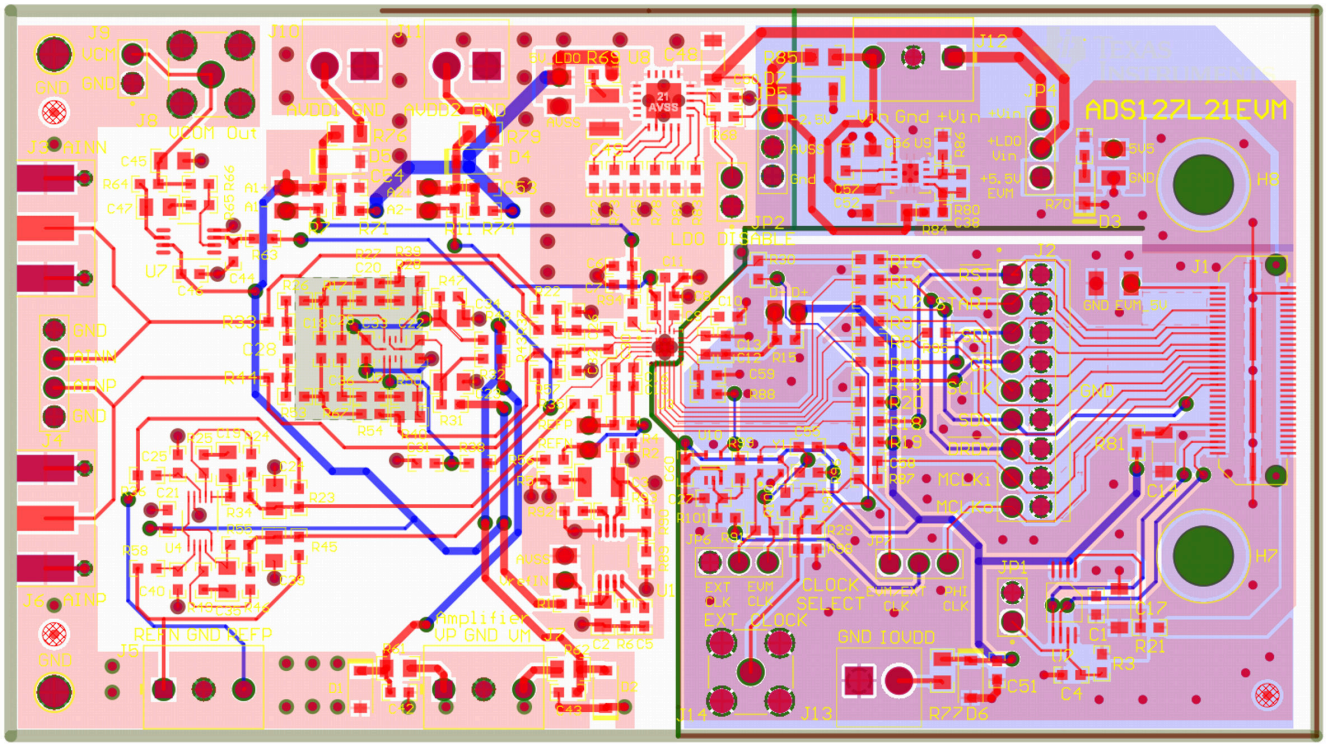

Figure 7-4. PCB Layout for the ADS127L21EVM

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

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2. 実験局の免許を取得後ご使用いただく。
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上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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