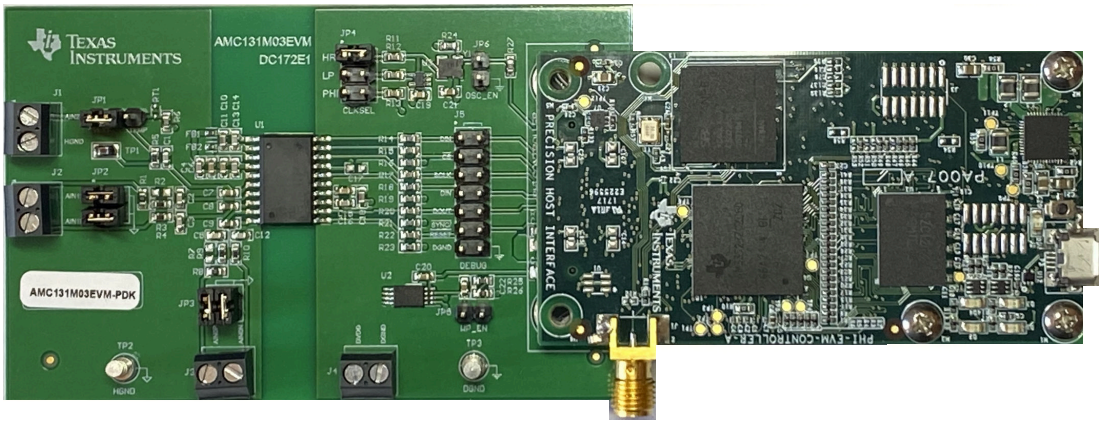
EVM User's Guide: AMC131M03EVM

AMC131M03 Evaluation Module

ABSTRACT



This user's guide describes the characteristics, operation, and use of the AMC131M03EVM-PDK. This evaluation module (EVM) is an evaluation platform for the AMC131M03, which is a 3-channel, simultaneously-sampling, 24-bit, reinforced isolated delta-sigma (ΔΣ) analog-to-digital converter (ADC) with integrated DC/DC converter and serial peripheral interface (SPI) interface. The AMC131M03 offers wide dynamic range, low power, and specific features for energy measurement, making the device an excellent fit for energy metering, power quality, protection relay, and circuit breaker applications.

The AMC131M03EVM eases the evaluation of the device with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the AMC131M03EVM. The following related documents are available through the Texas Instruments web site at www.ti.com.

Table 1-1. Related Documentation

Device	Literature Number
AMC131M03	SBAS994

Copyright © 2023 Texas Instruments Incorporated

Table of Contents

List of Figures

List of Tables

Copyright © 2023 Texas Instruments Incorporated

Trademarks

Windows® is a registered trademark of Microsoft.
LabVIEW® is a registered trademark of National Instruments.
All trademarks are the property of their respective owners.

Copyright © 2023 Texas Instruments Incorporated

1 Introduction

The AMC131M03EVM-PDK is a platform for evaluating the performance of the AMC131M03, which is a 3-channel, simultaneously-sampling, 24-bit, reinforced isolated ΔΣ ADC with integrated DC/DC converter. The evaluation kit includes the AMC131M03EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over the USB for data capture and analysis.

The AMC131M03EVM board includes the AMC131M03 ADC and all the peripheral analog circuits and components required to extract optimum performance from the ADC.

The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the AMC131M03
- Supplies power to all active circuitry on the AMC131M03EVM board

1.1 AMC131M03EVM Kit

The AMC131M03 evaluation module kit includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the AMC131M03 ADC
- USB powered—no external power supply is required
- The PHI controller that provides a convenient communication interface to the AMC131M03 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output
- Easy-to-use evaluation software for 64-bit Microsoft Windows® 7, Windows 8, and Windows 10 operating systems
- The software suite includes graphical tools for data capture, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file for post-processing.

Figure 1-1 illustrates an example system setup for evaluation.

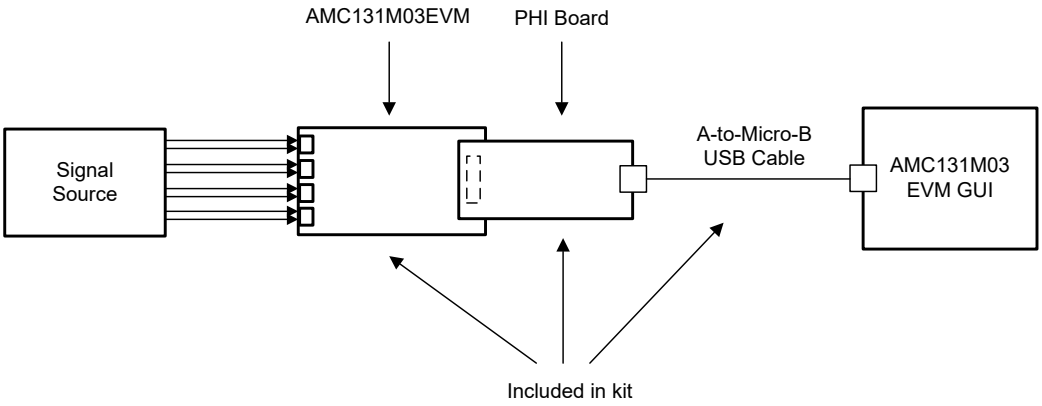


Figure 1-1. System Connection for Evaluation

1.2 AMC131M03EVM Board

The AMC131M03EVM board includes the following features:

- External signal source from differential pair headers
- Options to use external digital power supply
- Serial interface header for easy connection to the PHI controller
- Pin connections to monitor digital signals with a logic analyzer
- Onboard 8.192-MHz crystal oscillator, or external clock from PHI controller card

Copyright © 2023 Texas Instruments Incorporated

2 EVM Analog Interface

The AMC131M03EVM is designed for easy interfacing with analog sources. This section covers the details of the front-end circuit including jumper configuration for different input test signals and board connectors for signal sources.

2.1 ADC Analog Input Signal Path

Analog inputs to the EVM can be connected to either the terminal blocks or to the header pins associated with each ADC channel. The headers for each channel allow the user to configure the inputs differentially depending on the signal to be measured. The screw terminal blocks can interface directly with the leads of an external sensor input. Figure 2-1 shows the signal chain used for all three input channels on the EVM .

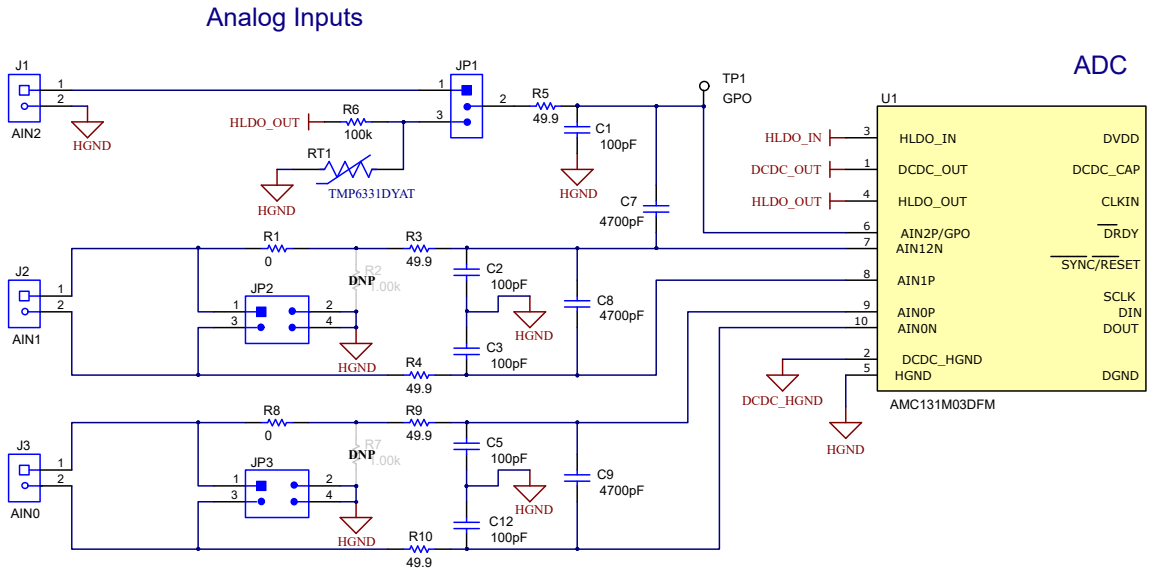


Figure 2-1. Analog Input (Schematic)

There are 3 analog input channels for the AMC131M03EVM: channel 0, 1, and 2. Signals can be applied to these channels via terminal blocks J3, J2, and J1, respectively.

Channel 0 (AIN0) and Channel 1 (AIN1) contain the same circuitry. This includes a terminal block to apply signals to AIN0P/N and AIN1P/N. These inputs can also be shorted to HGND via the provided jumpers on JP2 and JP3, respectively. Each channel also contains both common-mode and differential passive filters for antialiasing. If needed, one input on each channel can be divided down using the provided resistor divider footprints (this is unpopulated by default).

Channel 2 (AIN2) shares a negative channel input with Channel 1 (AIN12N). An external voltage can be applied to AIN2P by connecting to the terminal block, J1. This signal measured against AIN12N by configuring JP1 in the [1-2] position.

Another common use of Channel 2 is to measure the output of an external temperature sensor. The AMC131M03EVM provides an example temperature sensor circuit using the TMP6331, a 100-kΩ linear thermistor. The temperature sensor output can be selected using the [2-3] position on JP1.

2.2 ADC External Clock (CLKIN) Options

The AMC131M03 requires a continuous, free-running external controller clock at the CLKIN pin for normal operation. The onboard complementary metal oxide semiconductor (CMOS) crystal oscillator (Y1) provides the nominal 8.192-MHz clock frequency used in the high-resolution (HR) mode of the device. A D flip-flops (U3) divide the Y1 clock output to produce clock frequencies of 4.096 MHz to support the low-power (LP) mode.

Install a jumper in the appropriate position on the JP4 header to provide four selectable clock frequency options. An external clock frequency can also be provided to any odd-numbered pin on JP4 when the jumper is uninstalled. TI also recommends powering down Y1 by installing JP6 when providing an external clock. When using an external clock, ground must be shared between the external clock source and the EVM ground. The

Copyright © 2023 Texas Instruments Incorporated

external clock must adhere to the frequency and amplitude limits outlined in the AMC131M03 data sheet. Table 2-1 lists the JP4 jumper settings for the clock input selections.

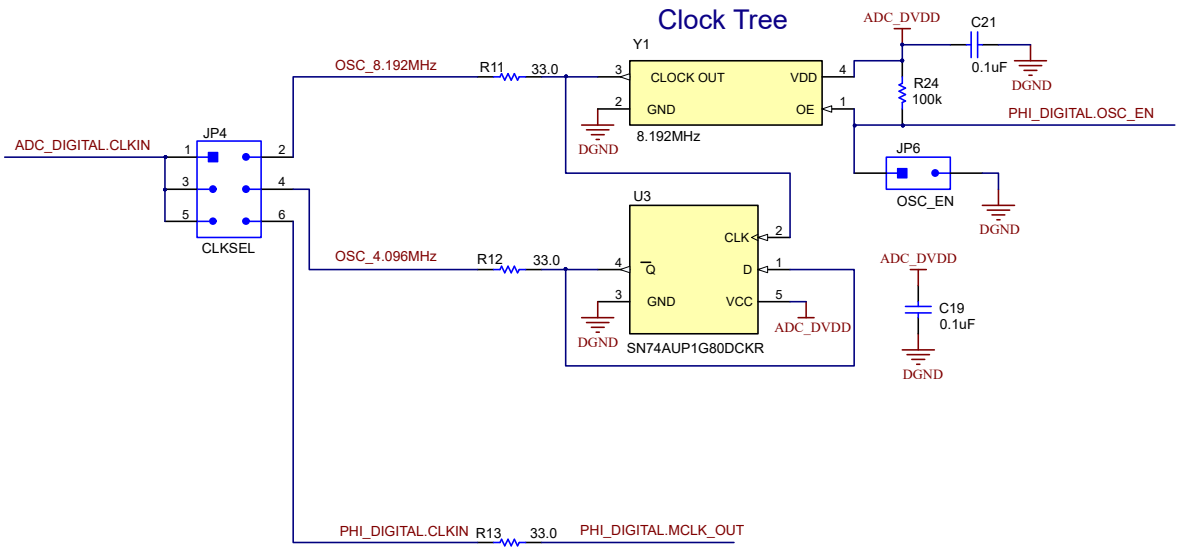


Figure 2-2. Clock Tree (Schematic)

Table 2-1. AMC131M03EVM CLKIN Options

JP4 Setting	CLKIN Source	CLKIN Frequency
1-2	Y1	8.192 MHz
3-4	U3	4.096 MHz
5-6	PHI	Configured in graphical user interface (GUI)
Open	External clock to JP4[5]	See data sheet for CLKIN range

Note

The current build of the GUI does not support the CLKIN signal generated by the PHI.

Copyright © 2023 Texas Instruments Incorporated

3 Digital Interface

As noted in Section 1, the EVM interfaces with the PHI and communicates with the computer over the USB. There are two devices on the EVM with which the PHI communicates: the AMC131M03 ADC (over SPI) and the EEPROM (over I^2C). The EEPROM comes pre-programmed with the information required to configure and initialize the AMC131M03EVM platform. When the hardware is initialized, the EEPROM is no longer used.

3.1 SPI Communication

The AMC131M03EVM supports limited interface modes as detailed in the AMC131M03 data sheet. The AMC131M03 uses a SPI-compatible interface to configure the device and retrieve conversion data. SPI communication on the AMC131M03 is performed in frames. Each SPI communication frame consists of several words. The word size is configurable as either 16 bits, 24 bits (default), or 32 bits by programming the WLENGTH[1:0] bits in the MODE register.

Additionally, the $\overline{\text{DRDY}}$ pin indicates when conversion data are available to be read by the controller. The DRDY_SEL[1:0] bits, DRDY_HIZ bit, and the DRDY_FMT bit in the MODE register control the behavior of the $\overline{\text{DRDY}}$ pin.

For this EVM, not all modes and functions for this SPI communication are supported. Functions not supported are disabled in the EVM GUI software. For more information about the SPI communication, see the AMC131M03 data sheet.

3.2 Connection to the PHI

The AMC131M03EVM board communicates with the PHI through a shrouded, 60-pin connector, J6. There are two round standoffs next to J6 with Phillips-head screws. To connect the PHI to the EVM, remove the screws, attach the PHI to the EVM, and replace the screws into the standoffs. The screws secure the EVM to the PHI and verifies the connection between the boards.

Table 3-1 lists the different PHI connection and their functions.

Table 3-1. PHI Connector Pin Functions

PHI Connector Pin Name	PHI Connector Pin	Function
DGND	J6[3]	Ground
OSC_EN	J6[6]	External oscilator enable
DIN	J6[18]	Serial data input for the AMC131M03
$\overline{\text{CS}}$	J6[22]	Chip select for the AMC131M03; active low
SCLK	J6[24]	Serial data clock for the AMC131M03
CAPCLK	J6[26]	Capture clock for the AMC131M03
CAPCLK	J6[28]	Capture clock for the AMC131M03
$\overline{\text{DRDY}}$	J6[30]	Data ready for the AMC131M03; active low
OSC_8.192MHz	J6[32]	Controller clock input for the AMC131M03
MCLK_OUT	J6[34]	Controller clock output for the AMC131M03
DOUT	J6[36]	Serial data output for the AMC131M03
$\overline{\text{SYNC}}$/ $\overline{\text{RESET}}$	J6[46]	Conversion synchronization or system reset for the AMC131M03; active low
EVM_WP	J6[49]	Write protection enable for the EEPROM
ADC_DVDD	J6[50]	Power-supply source for the AMC131M03
SDA	J6[56]	I^2C serial data for the EEPROM used to identify the EVM
SCL	J6[58]	I^2C serial clock for the EEPROM used to identify the EVM
EVM_ID_PWR	J6[59]	Power-supply source for the EEPROM used to identify the EVM
DGND	J6[60]	Ground

Copyright © 2023 Texas Instruments Incorporated

3.3 Digital Header

In addition to the PHI, the EVM has a header connected to the digital lines that can be used to connect a logic analyzer or oscilloscope. This placement allows for easy access to the digital communications. Header J5 is connected to the digital lines between the AMC131M03 and the PHI connector. Table 3-2 describes the digital header pins.

Table 3-2. Digital Header Pins

AMC131M03 Pin Name	Digital Header Pin
DIN	J5[1], J5[2]
$\overline{CS}$	J5[3], J5[4]
SCLK	J5[5], J5[6]
$\overline{DRDY}$	J5[7], J5[8]
DOUT	J5[9], J5[10]
$\overline{SYNC}$/ $\overline{RESET}$	J5[11], J5[12]
DGND	J5[13], J5[14]

Copyright © 2023 Texas Instruments Incorporated

4 Power Supplies

The PHI provides multiple power-supply options for the EVM, derived from the USB supply of the computer.

The EEPROM on the AMC131M03EVM uses a 3.3-V power supply generated directly by the PHI. The low-side analog and digital supply (DVDD) of the ADC uses a 3.3-V power supply provided directly by a low-dropout (LDO) regulator on the PHI.

The power supply for each active component on the EVM is bypassed with a ceramic capacitor placed close to that component. Additionally, the EVM layout uses thick traces or large copper fill areas, where possible, between bypass capacitors and their loads to minimize inductance along the load current path.

As mentioned previously in Section 1, power to the EVM is supplied by the PHI through connector J6. For information about PHI pins and the power connections, see Table 3-1.

With modifications, the user can use external supplies for the low-side analog and digital supply (DVDD) of the ADC. DVDD can be driven externally from the terminal block J4.

Copyright © 2023 Texas Instruments Incorporated

5 AMC131M03EVM Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for properly operating the AMC131M03EVM.

5.1 Default Jumper Settings

After unpacking, the EVM is already configured with the default jumper settings. Figure 5-1 shows the locations for the default jumpers.

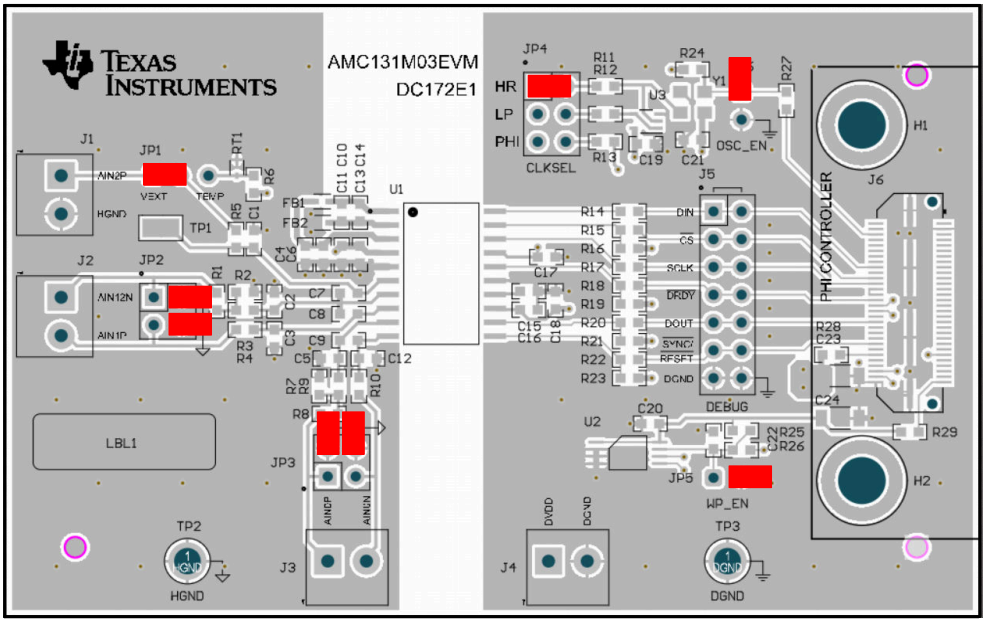


Figure 5-1. AMC131M03EVM Jumper Default Settings

The default position of the JP4 jumper is across [1-2] at the top. JP4 sets the onboard oscillator frequency to 8.192 MHz, used for the AMC131M03 in high-resolution mode. The default connection for JP1 is to the left [1-2], so that the channel AIN2P of the AMC131M03 is used to convert the signal from the J1 terminal block.

The default settings, as listed in Table 5-1, includes no jumpers installed at JP5, JP6. When installed, JP5 enables the EEPROM for write, and JP6 disables the onboard oscillator.

Table 5-1. Default Settings

Jumper	Position	Function
JP1	[1-2]	Selects input for AIN2P of the ADC
JP2	Not installed	Ground connection for input
JP3	Not installed	Ground connection for input
JP4	[1-2]	Oscillator frequency select, 8.192MHz
JP5	Not installed	Disables write for EEPROM
JP6	Not installed	Disables on-board oscillator

Copyright © 2023 Texas Instruments Incorporated

5.2 EVM Graphical User Interface (GUI) Software Installation

Download the latest version of the EVM GUI installer from the *Tools and Software* folder of the AMC131M03EVM and run the GUI installer to install the EVM GUI software on your computer.

> **CAUTION**
> Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message can appear or the installer. The .exe file can be deleted.

Accept the license agreements and follow the on-screen instructions shown in Figure 5-2 to complete the installation.

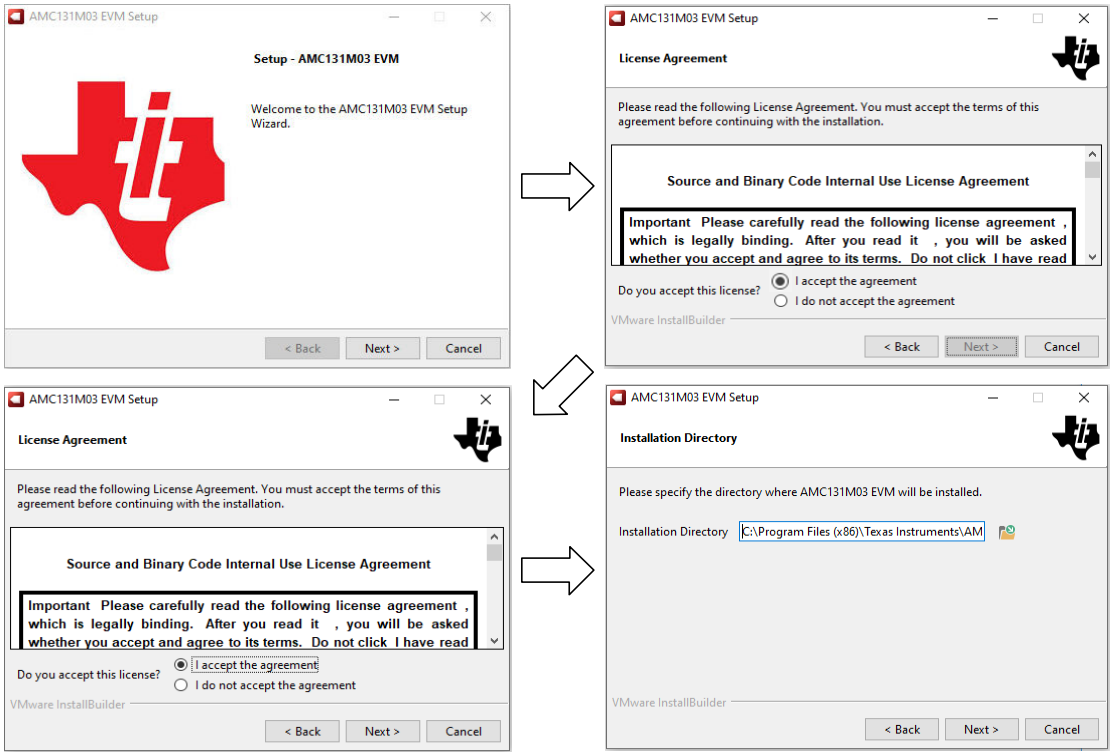


Figure 5-2. AMC131M03 Software Installation Prompts

As a part of the AMC131M03EVM GUI installation, a prompt with a Device Driver Installation (as shown in Figure 5-3) appears on the screen. Click *Next* to proceed.

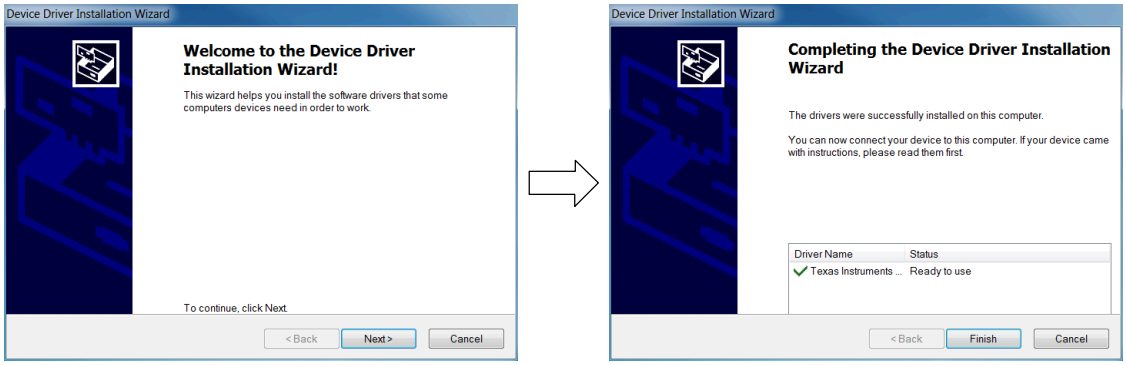


Figure 5-3. Device Driver Installation Wizard Prompts

Copyright © 2023 Texas Instruments Incorporated

Note

A notice can appear on the screen stating that Windows cannot verify the publisher of this driver software. Select *Install this driver software anyway*.

The AMC131M03EVM requires the LabVIEW® run-time engine and can prompt for the installation of this software, as shown in Figure 5-4, if not already installed.

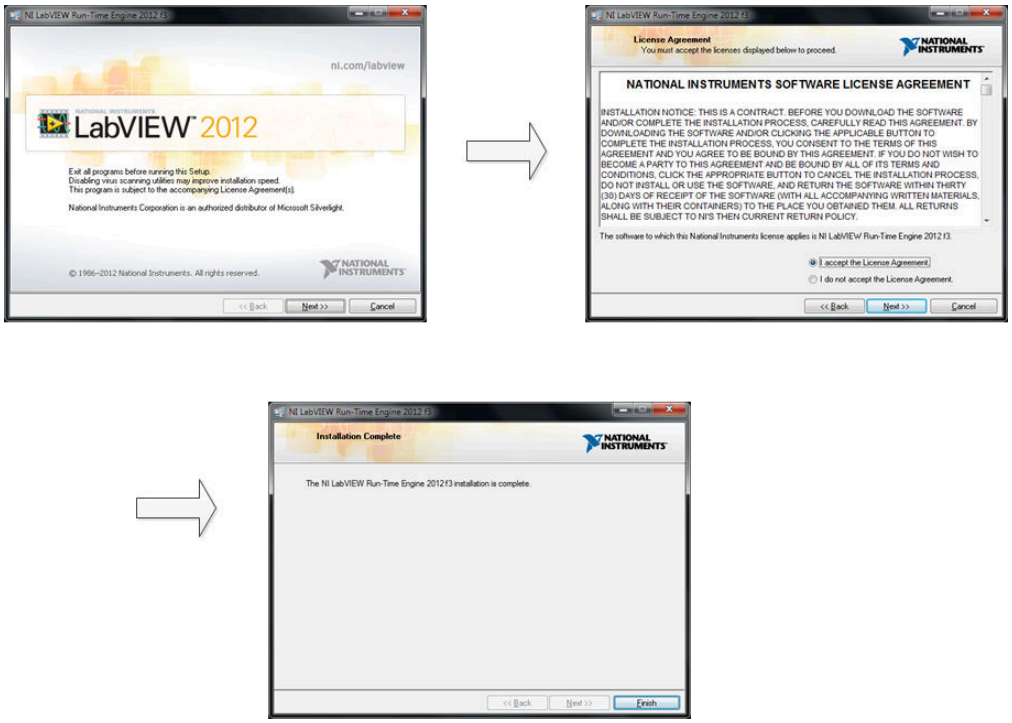


Figure 5-4. LabVIEW Run-Time Engine Installation

Verify that *C:\Program Files (x86)\Texas Instruments\AMC131M03EVM* is as shown in Figure 5-5 after these installations.

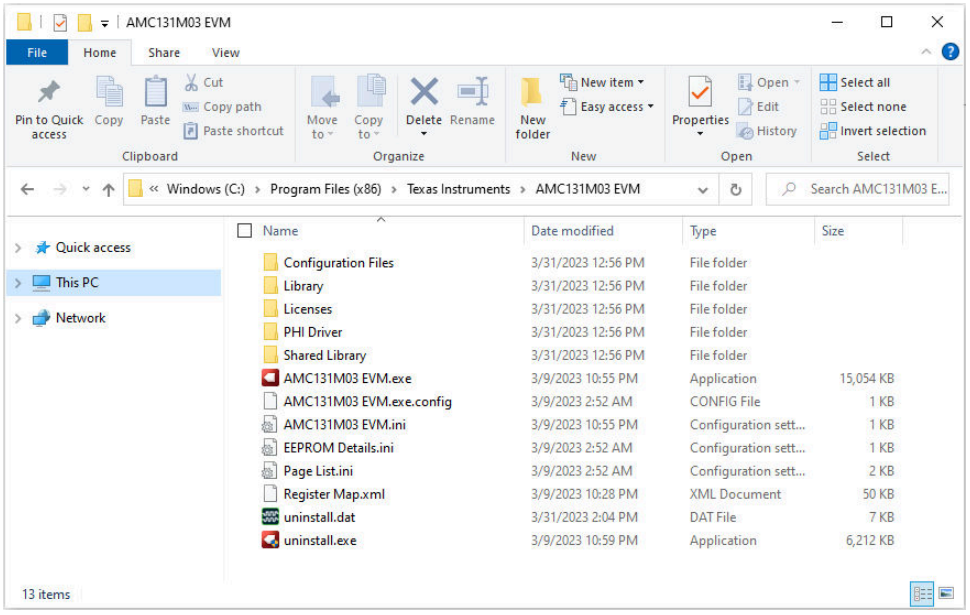


Figure 5-5. AMC131M03EVM GUI Folder Post-Installation

Copyright © 2023 Texas Instruments Incorporated

6 AMC131M03EVM Operation

The following instructions are a step-by-step guide to connecting the AMC131M03EVM to the computer and evaluating the performance of the AMC131M03:

1. Connect the AMC131M03EVM to the PHI. Install the two screws as indicated in Figure 6-1.
2. Use the provided USB cable to connect the PHI to the computer.
   - LED D5 on the PHI lights up, indicating that the PHI is powered up
   - LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC; Figure 6-1 shows the resulting LED indicators

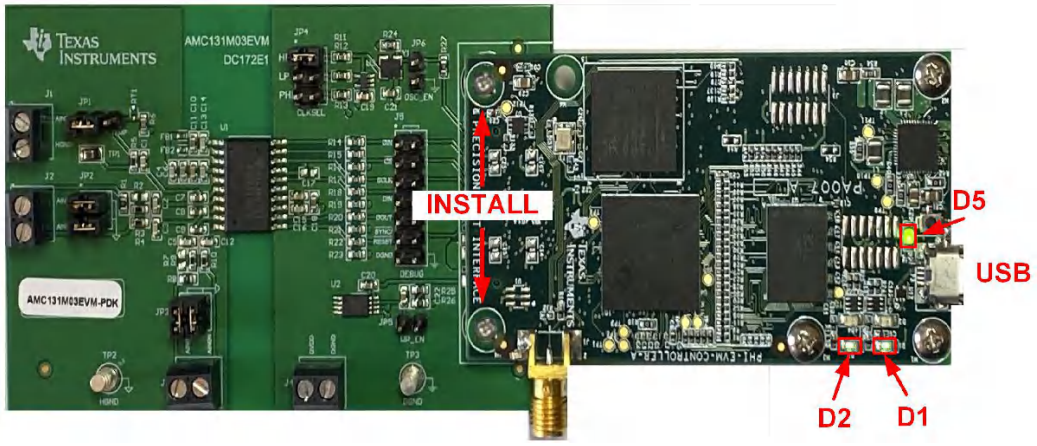


Figure 6-1. AMC131M03EVM Hardware Setup and LED Indicators

3. Figure 6-2 shows how to launch the AMC131M03EVM GUI software.

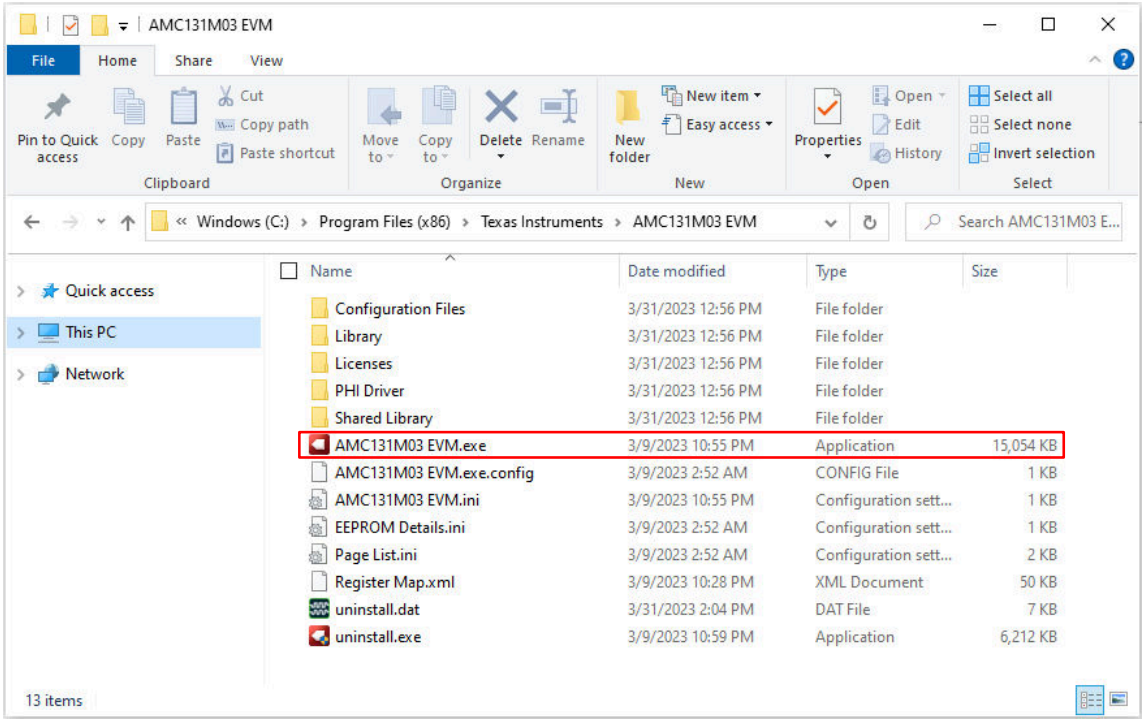


Figure 6-2. Launch the EVM GUI Software

Copyright © 2023 Texas Instruments Incorporated

6.1 EVM GUI Global Settings for ADC Control

Although the EVM GUI does not allow direct access to the levels and timing configuration of the ADC digital interface, the EVM GUI does give users high-level control over virtually all functions of the AMC131M03 including interface modes, sampling rate, and number of samples to be captured. Figure 6-3 identifies the input parameters of the GUI (as well as their default values) through which the various functions of the AMC131M03 can be exercised.

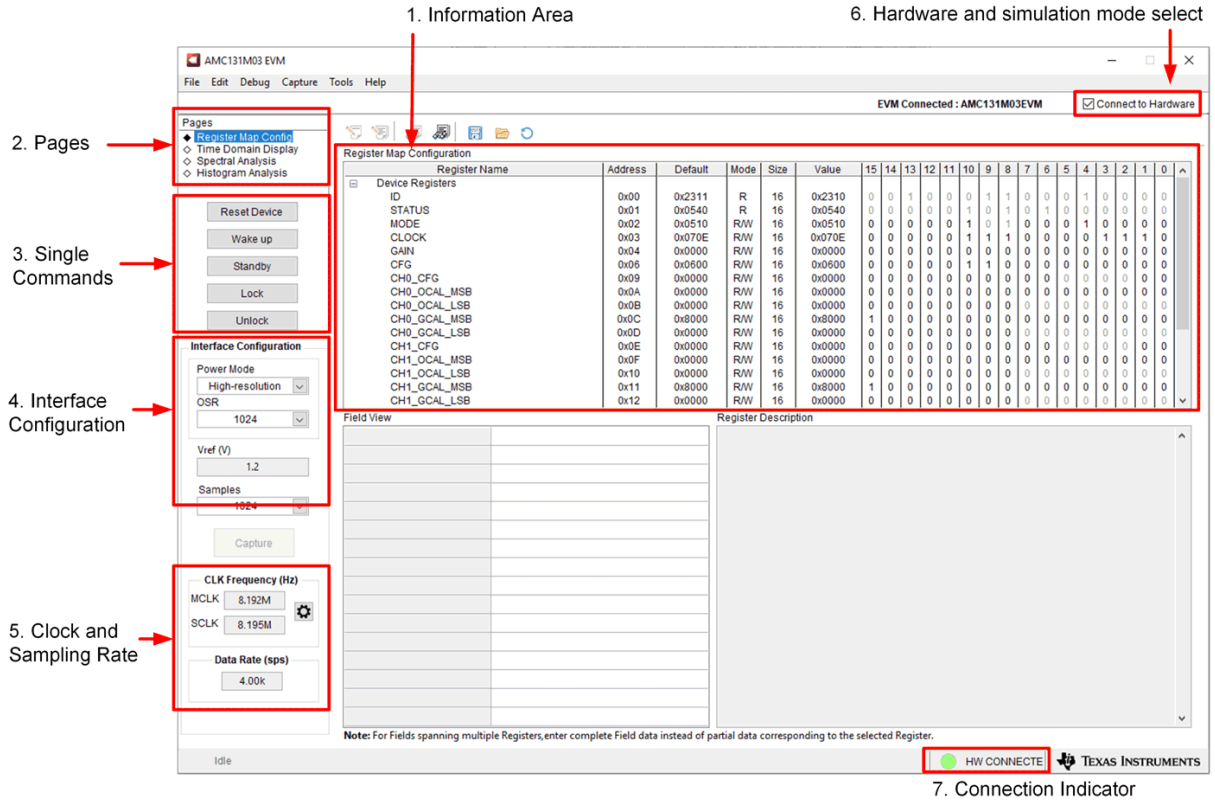


Figure 6-3. EVM GUI Global Input Parameters

There are four pages available in the AMC131M03EVM GUI. The information area displays the results of each of the pages. Each of these pages display a different control or measurement of the device. The Register Map Config page is used to read and write to the registers of the device. The Time Domain Display page is used to collect a set of data from the device and display the result. The Spectral Analysis page can determine the FFT of the collected data, and the Histogram Analysis page shows a histogram of the collected data and displays basic statistics of the result.

The Single Commands section allows for direct control of the device for five basic functions. First the *Reset Device* button sends a signal to the SYNC/RESET pin to reset the device. The *Standby* button puts the device into a low-power state in which all channels are disabled, and the reference and other non-essential circuitry are powered down. The *Wake up* button wakes the device from standby to convert mode. The *Lock* button lock the interface such that only the NULL, UNLOCK, and RREG commands are valid. The *Unlock* button unlocks the interface.

The Interface Configuration options in this pane allows the user to choose from different frame word sizes available on the AMC131M03. This section also sets the data rate by setting the oversampling ratio (OSR) in the ADC. Finally, this section can be used to set the power modes in the registers. The AMC131M03 can be set to high-resolution and low power modes in conjunction with the jumper settings of JP4 for the CLKIN pin, as outlined in Table 2-1. This information is also discussed in Section 2.2.

The Clock and Data Rate section allows the user to select the CLK source and SCLK source, and change the SCLK frequency (in Hz). These configurations can be implemented by checking the clock setting button in the CLK Frequency area and changing the dropdown as shown in Figure 6-4 . The clock source selection in the

Copyright © 2023 Texas Instruments Incorporated

Clock Settings must match the jumper installed on JP4 on the AMC131M03EVM. Select *Custom* if an external CLKIN clock is provided directly to JP4[5].

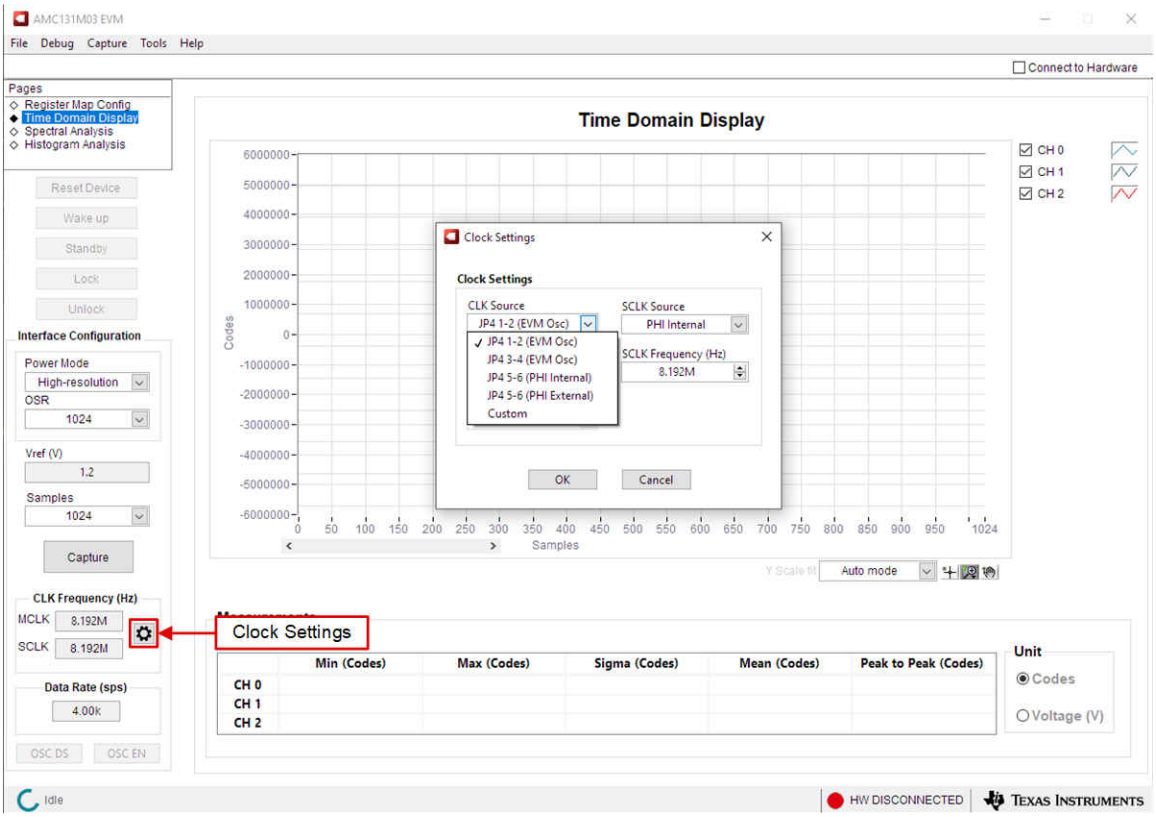


Figure 6-4. Clock Setting Dialog

The GUI tries to match this frequency as closely as possible by changing the PHI PLL settings, but the achievable frequency can differ from the target value entered. This section also displays the data rate of the ADC as controlled by the OSR configuration.

The GUI is switched between hardware mode and simulation mode by checking and unchecking the *Connected to Hardware* box in the top right area of the screen at any time.

Copyright © 2023 Texas Instruments Incorporated

6.2 Register Map Configuration Tool

The register map configuration tool allows the user to view and modify the registers of the AMC131M03. This tool can be selected, as indicated in Figure 6-5, by clicking on the *Register Map Config* button at the Pages section of the left pane. On power-up, the values on this page correspond to the ADC default register settings with the DC/DC converter enabled. The register values can be edited by:

1. Double-clicking the corresponding Value field and entering the desired hexadecimal register setting.
2. Choosing the desired setting for each bit field in the Field View below the register map.
3. Clicking each individual bit to toggle the current value.

Each of the three actions above immediately executes a WREG (“register-write”) command followed by a RREG (“register-read”) command to confirm the register setting was written correctly.

If interface mode settings are affected by the change in register values, then this change reflects on the left pane immediately. The changes in the register value reflect on the AMC131M03 device on the AMC131M03EVM based on the Update Mode selection, as described in Section 6.1.

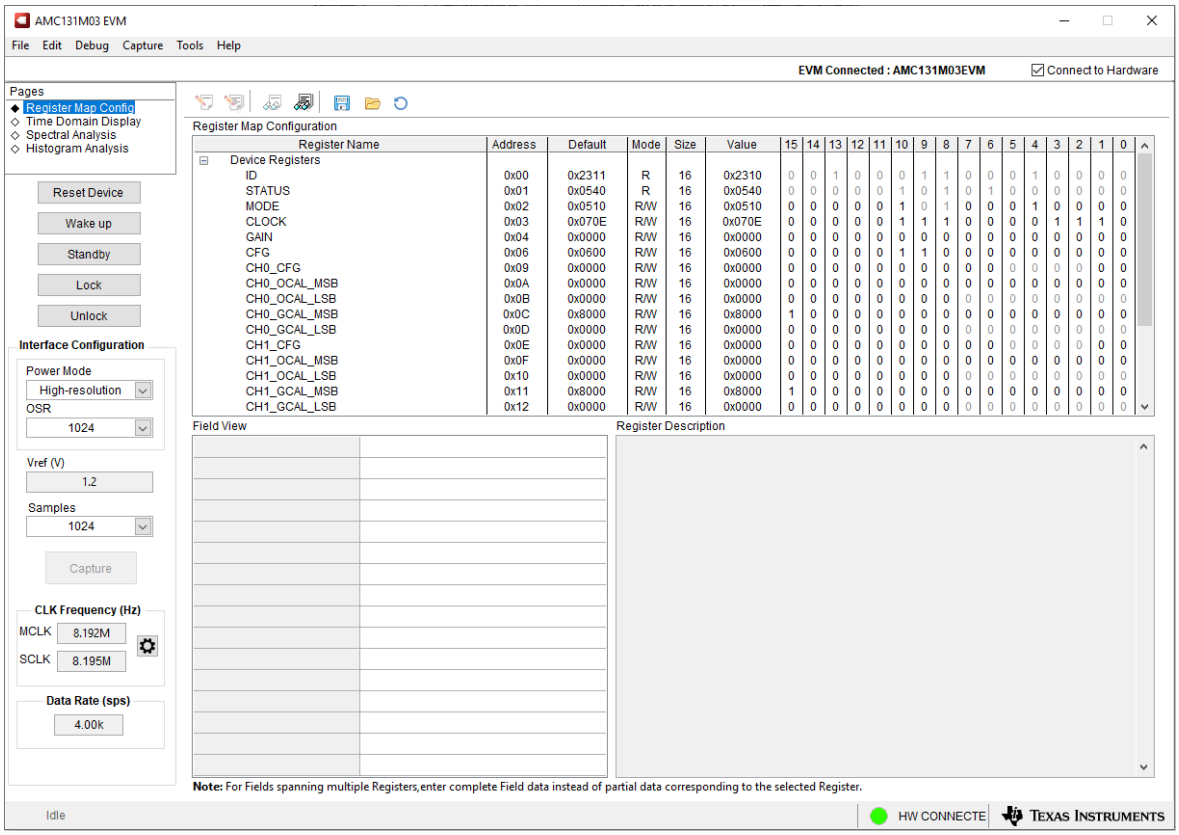


Figure 6-5. Register Map Configuration

Section 6.3 through Section 6.5 describe the data collection and analysis features of the AMC131M03EVM GUI.

Copyright © 2023 Texas Instruments Incorporated

6.3 Time Domain Display Tool

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits.

The user can trigger a capture of the data of the selected number of samples from the AMC131M03EVM, as per the current interface mode settings indicated in Figure 6-6 by using the *Capture* button. The sample indices are on the x-axis and the y-axes showing the corresponding output codes or the equivalent analog voltages based on the specified reference voltage. The code or voltage unit can be selected in the botom right Unit area at any time. Switching pages to any of the Analysis tools described in the subsequent sections causes calculations to be performed on the same set of data.

Figure 6-6. Time Domain Display Tool Options

Copyright © 2023 Texas Instruments Incorporated

6.4 Spectral Analysis Tool

The spectral analysis tool, shown in Figure 6-7, is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the AMC131M03 ADC through single-tone sinusoidal signal FFT analysis using the *7-term Blackman-Harris* window setting.

Figure 6-7. Spectral Analysis Tool

The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The *7-Term Blackman Harris* window is the default option and has sufficient dynamic range to resolve the frequency components up to a 24-bit ADC. The *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

Copyright © 2023 Texas Instruments Incorporated

6.5 Histogram Tool

Noise degrades ADC resolution and the histogram tool can be used to estimate effective resolution, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output from sources, such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a DC input applied to a given channel.

As shown in Figure 6-8, the histogram corresponding to a DC input is displayed on clicking the *Capture* button.

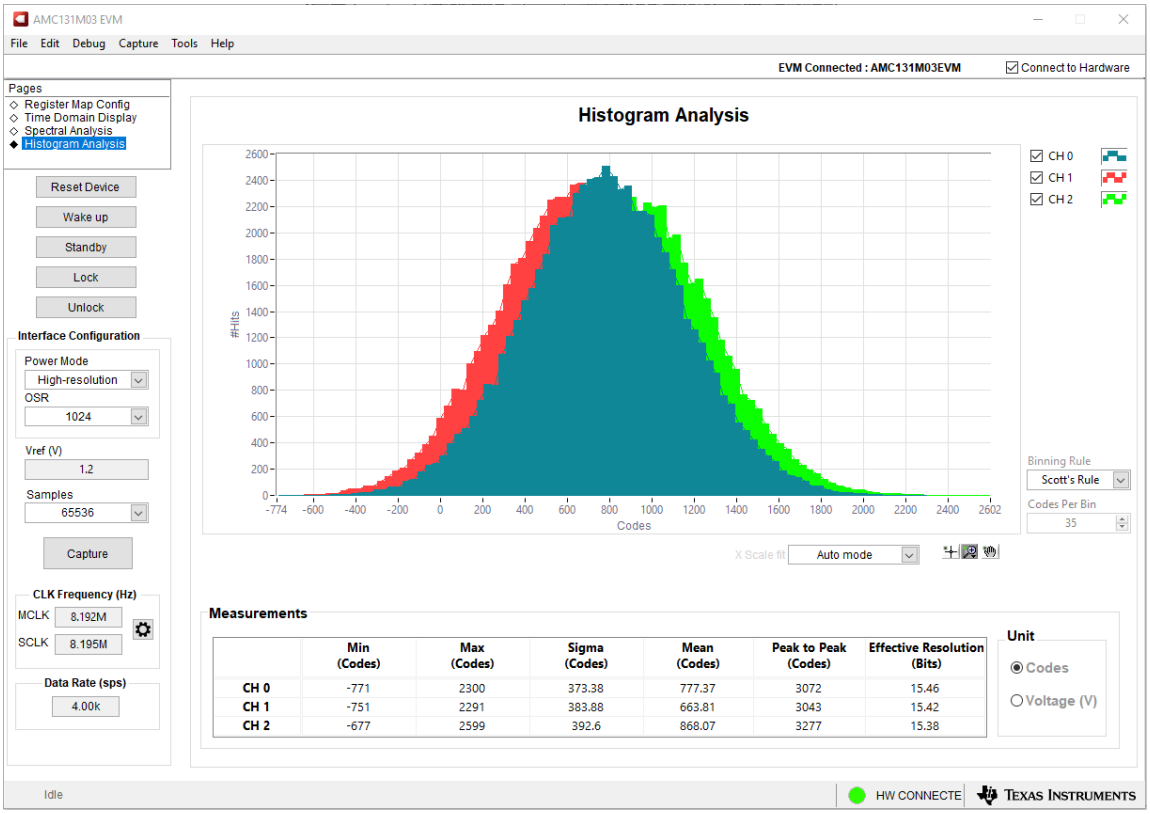


Figure 6-8. Histogram Analysis Tool

Copyright © 2023 Texas Instruments Incorporated

7 AMC131M03EVM Bill of Materials, PCB Layout, and Schematic

7.1 PCB Layout

Figure 7-1 through Figure 7-6 illustrate the AMC131M03EVM PCB layout.

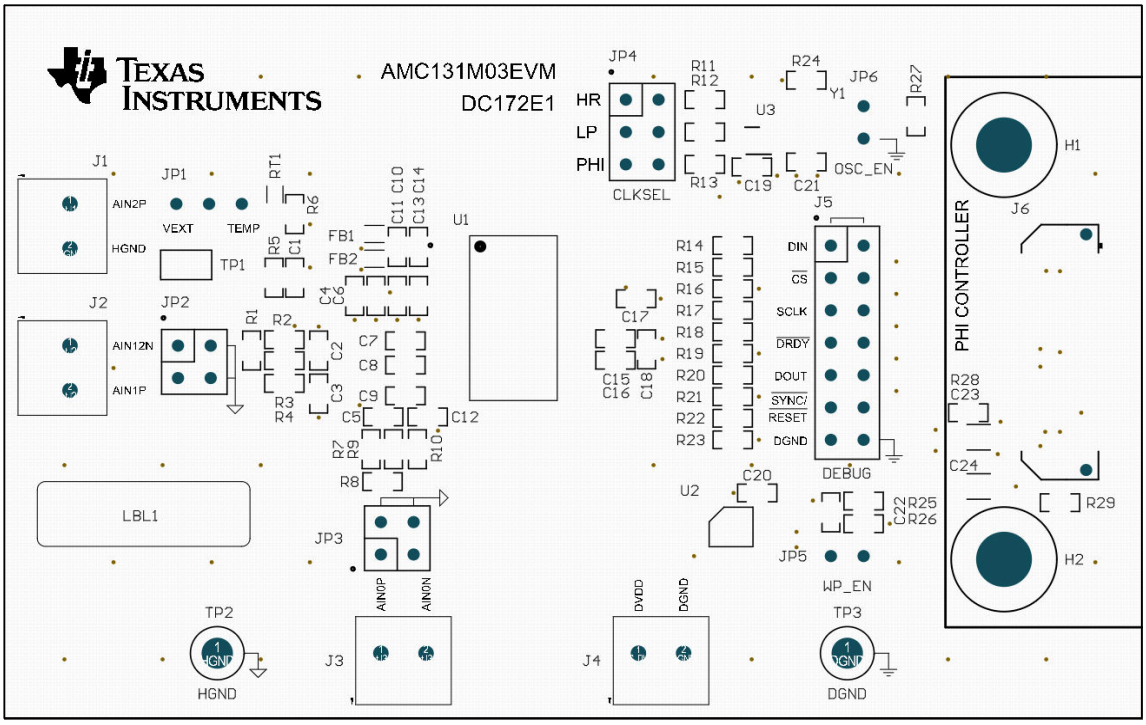


Figure 7-1. Top Silkscreen

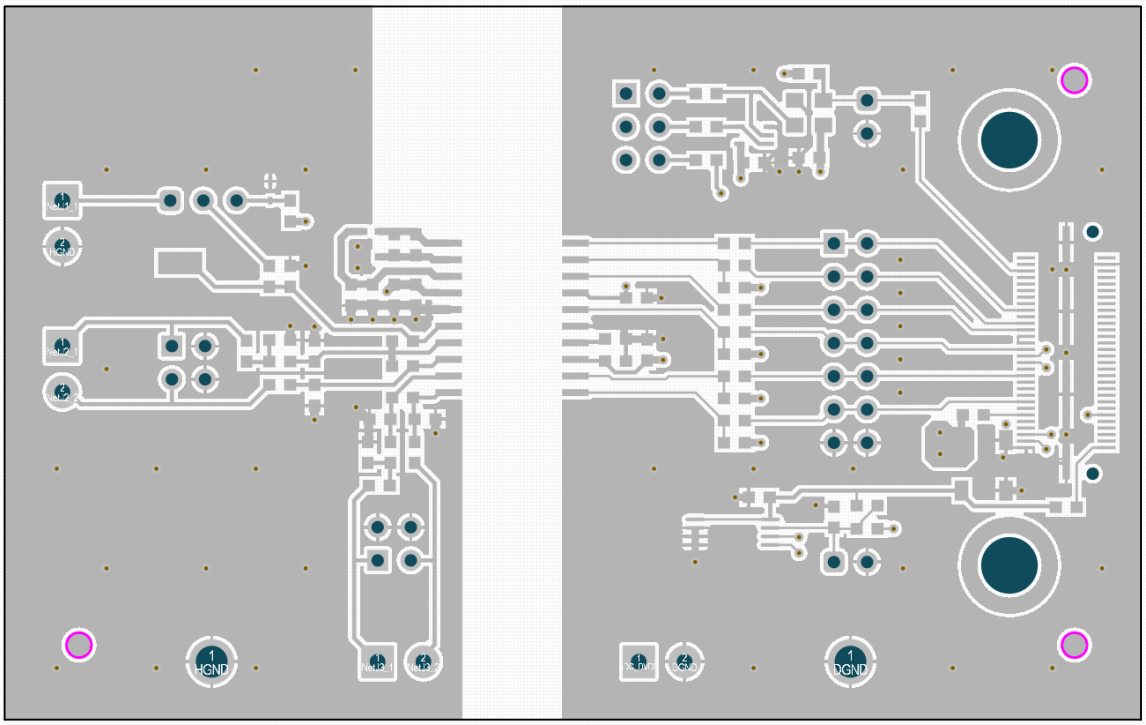


Figure 7-2. Top Layer

Copyright © 2023 Texas Instruments Incorporated

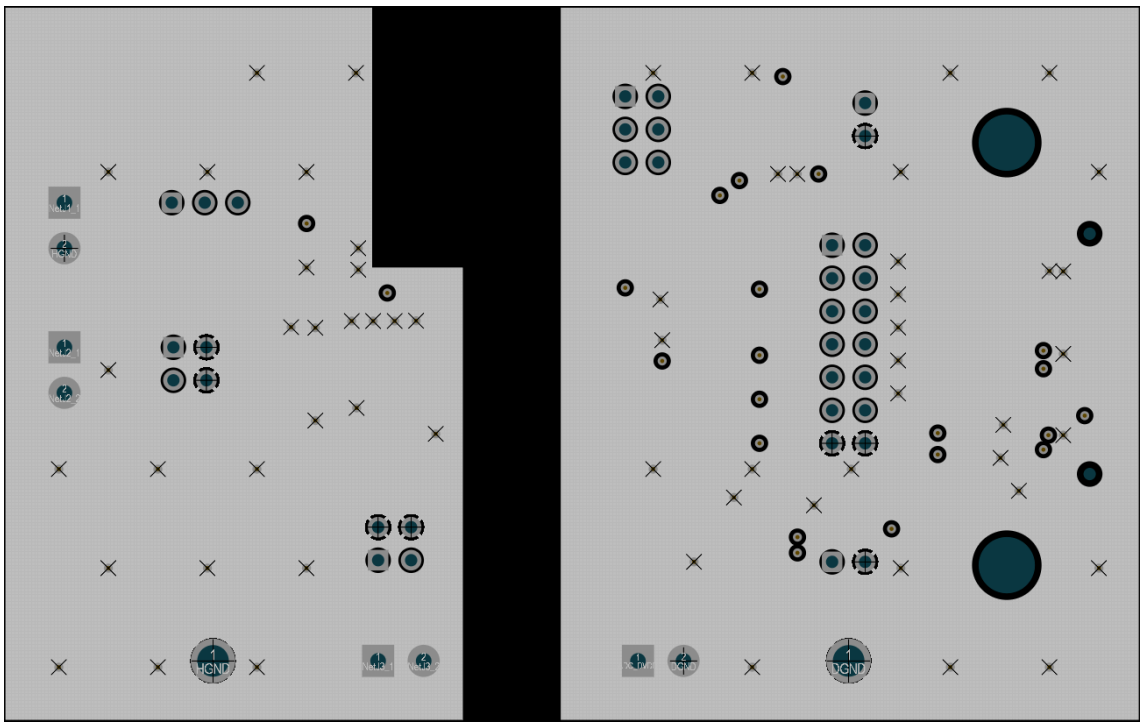


Figure 7-3. Ground Layer - Internal

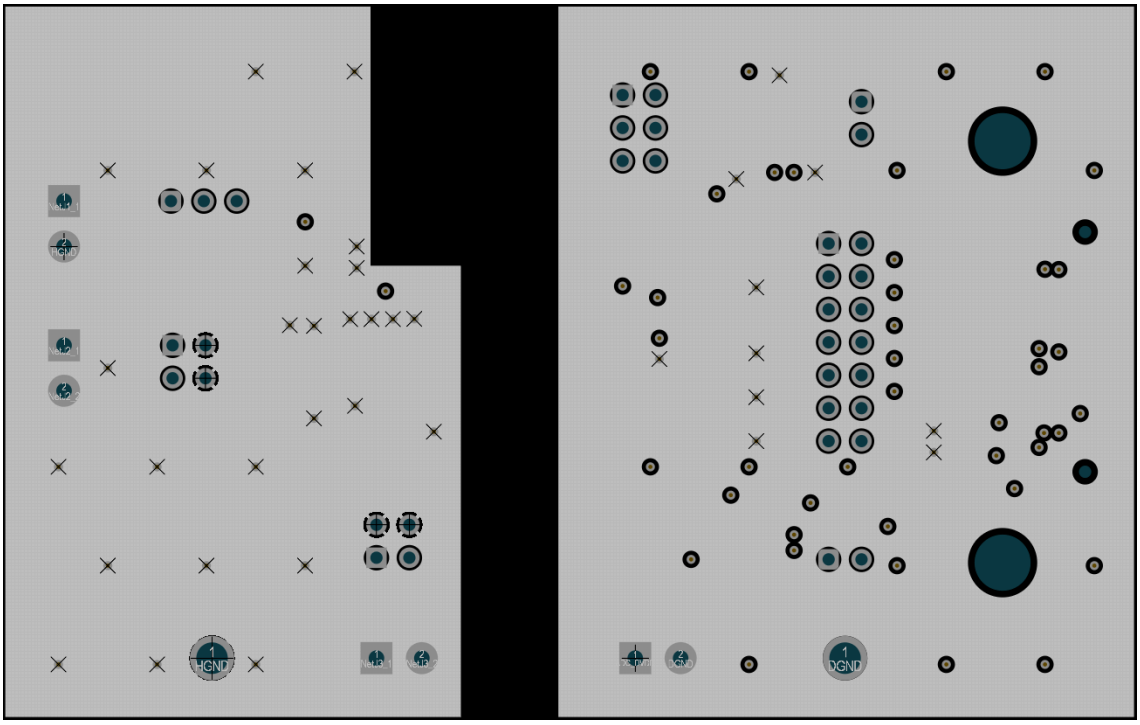


Figure 7-4. Power Layer - Internal

Copyright © 2023 Texas Instruments Incorporated

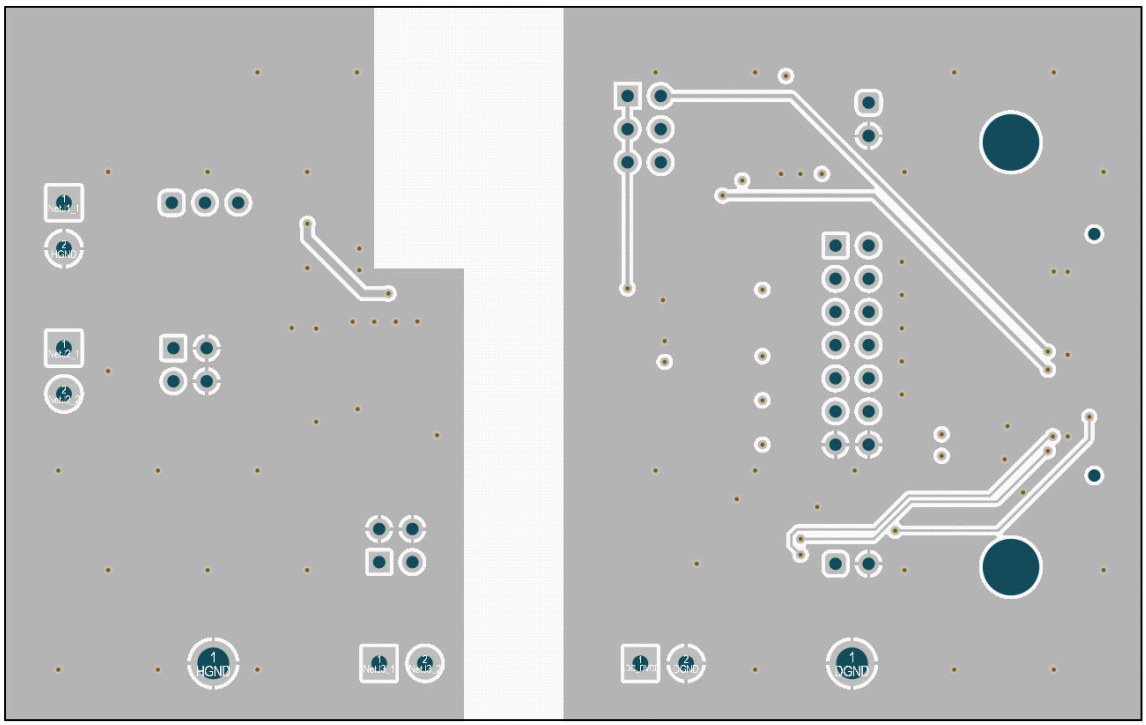


Figure 7-5. Bottom Layer

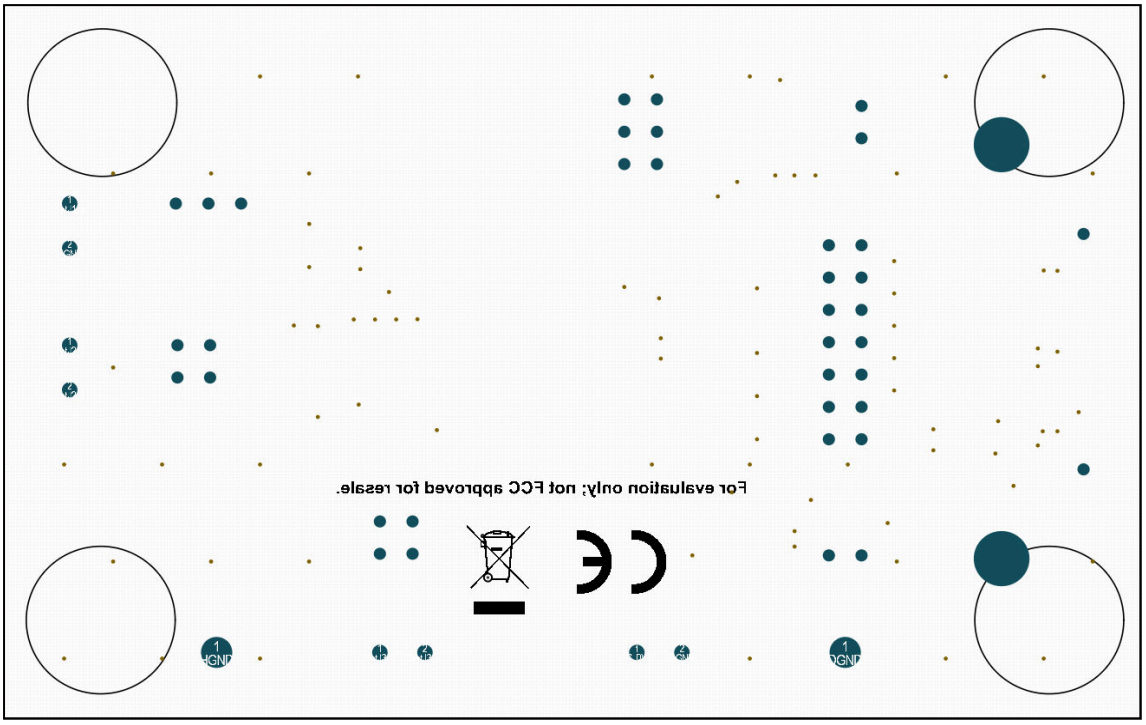


Figure 7-6. Bottom Silkscreen

Copyright © 2023 Texas Instruments Incorporated

7.2 Schematics

Figure 7-7 illustrates the AMC131M03EVM schematics.

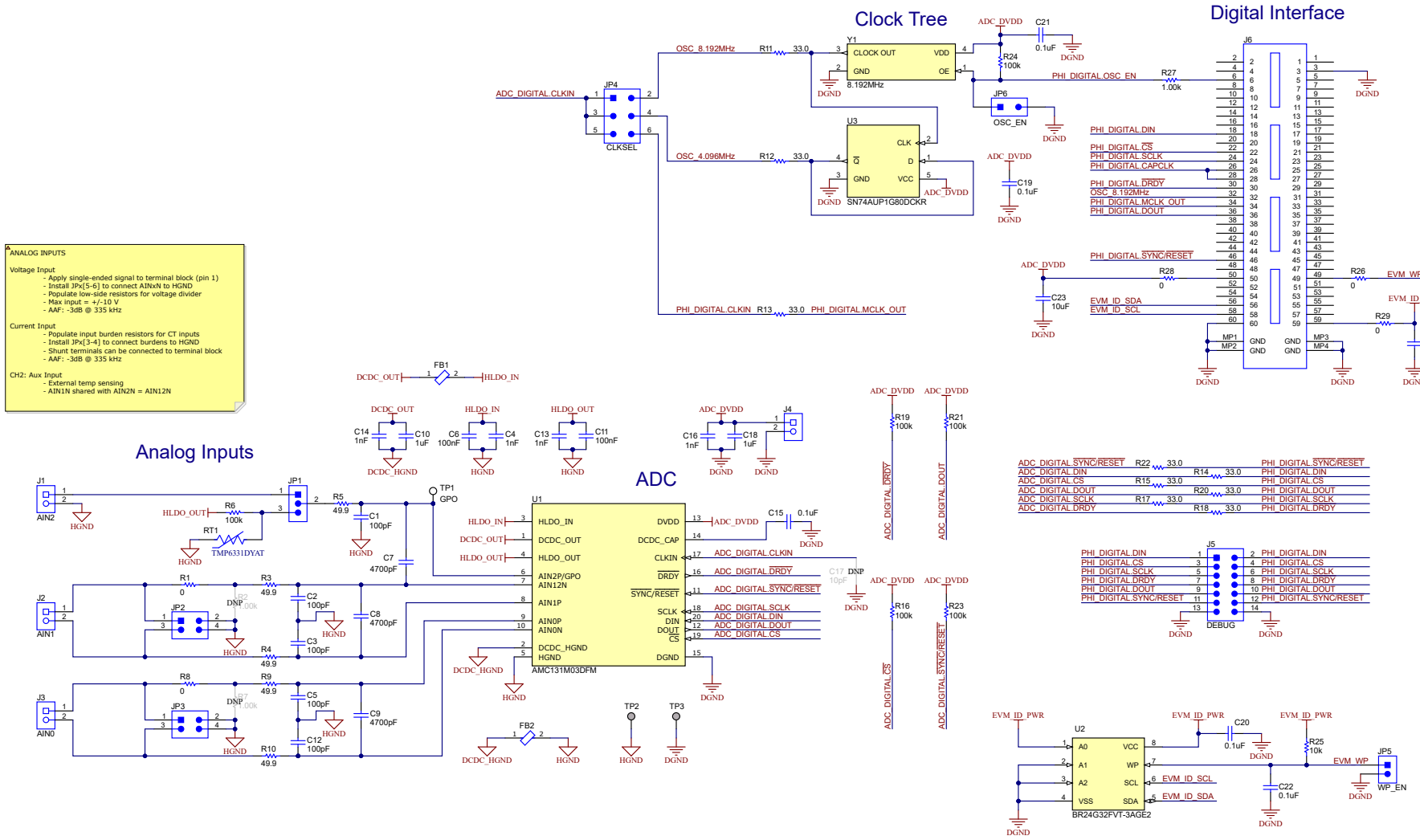


Figure 7-7. AMC131M03EVM Main Schematic

Copyright © 2023 Texas Instruments Incorporated

7.3 Bill of Materials

Section 7.3 lists the AMC131M03EVM bill of materials.

Table 7-1. AMC131M03EVM Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C1, C2, C3, C5, C12	5	100 pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	603	8.85012E+11	Wurth Elektronik
C4, C13, C14, C16	4	1000 pF	CAP, CERM, 1000 pF, 50 V, +/- 10%, X7R, 0603	603	C0603C102K5RACTU	Kemet
C6, C11, C15	3	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	603	C1608X7R1H104K080AA	TDK
C7, C8, C9	3	4700 pF	CAP, CERM, 4700 pF, 100 V, +/- 5%, C0G/NP0, 0603	603	C0603C472J1GAC7867	Kemet
C10, C18	2	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	603	C0603C105K3RACTU	Kemet
C17	1	10 pF	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0603	603	C0603C100J5GACTU	Kemet
C19, C20, C21, C22	4	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	603	C0603C104J3RAC	Kemet
C23, C24	2	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7R, 1206_190	1206_190	C1206C106K3RACTU	Kemet
FB1, FB2	2		1.8 kOhms @ 100 MHz 1 Power, Signal Line Ferrite Bead 0402 (1005 Metric) 210 mA 2.1Ohm	402	74269244182	Wurth Electronics
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2	2		ROUND STANDOFF M3 STEEL 5 MM	ROUND STANDOFF M3 STEEL 5 MM	9774050360R	Wurth Elektronik
H2, H4	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL
H3, H4, H5, H6	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M

Copyright © 2023 Texas Instruments Incorporated

Table 7-1. AMC131M03EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
H8	1		Cable, USB-A to micro USB-B, 1 m - Kitting item		102-1092-BL-00100	CnC Tech
H9	1		PHI-EVM Controller Kitting item Edge# 6591636		PA007	Texas Instruments
J1, J2, J3, J4	4		Terminal Block, 3.5mm Pitch, 2x1, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
J5	1		Header, 100mil, 7x2, Gold, TH	7x2 Header	TSW-107-07-G-D	Samtec
J6	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A	Samtec
JP1	1		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
JP2, JP3	2		Header, 100mil, 2x2, Gold, TH	2x2 Header	TSW-102-07-G-D	Samtec
JP4	1		Header, 100mil, 3x2, Gold, TH	3x2 Header	TSW-103-07-G-D	Samtec
JP5, JP6	2		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
R1, R8, R26, R28, R29	5	0	RES, 0, 5%, 0.1 W, 0603	603	RC0603JR-070RL	Yageo
R3, R4, R5, R9, R10	5	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW060349R9FKEA	Vishay-Dale
R6, R16, R19, R21, R23, R24	6	100k	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW0603100KFKEA	Vishay-Dale
R11, R12, R13, R14, R15, R17, R18, R20, R22	9	33	RES, 33.0, 1%, 0.1 W, 0603	603	RC0603FR-0733RL	Yageo

Copyright © 2023 Texas Instruments Incorporated

Table 7-1. AMC131M03EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R25	1	10k	RES, 10 k, 5%, 0.1 W, 0603	603	RC1608J103CS	Samsung Electro-Mechanics
R27	1	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW06031K00FKEA	Vishay-Dale
RT1	1	100k	±1% tolerance 100 kΩ linear thermistor available in an 0402 package 2-SOT-5X3 -40 to 150	SOD523	TMP6331DYAT	Texas Instruments
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6	6	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1	1		Test Point, Miniature, SMT	Testpoint_Keystone_Miniature	5015	Keystone
TP2, TP3	2		Terminal, Turret, TH, Triple	Keystone1598-2	1598-2	Keystone
U1	1		3-Channel, Simultaneously-Sampling, 24-Bit, Reinforced Isolated DeltaSigma ADC With Integrated DC/DC Converter	SOIC20	AMC131M03DFM	Texas Instruments
U2	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm
U3	1		Low-Power Single Postitive-Edge-Triggered D-Type Flip-Flop, DCK0005A, LARGE T&R	DCK0005A	SN74AUP1G80DCKR	Texas Instruments
Y1	1		Oscillator, 8.192 MHz, 15 pF, AEC-Q200 Grade 1, SMD	3.2x2.5mm	SIT8924BA-22-33E-8.192000G	SiTime

Copyright © 2023 Texas Instruments Incorporated

Table 7-1. AMC131M03EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R2, R7	0	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW06031K00FKEA	Vishay-Dale

Copyright © 2023 Texas Instruments Incorporated

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated