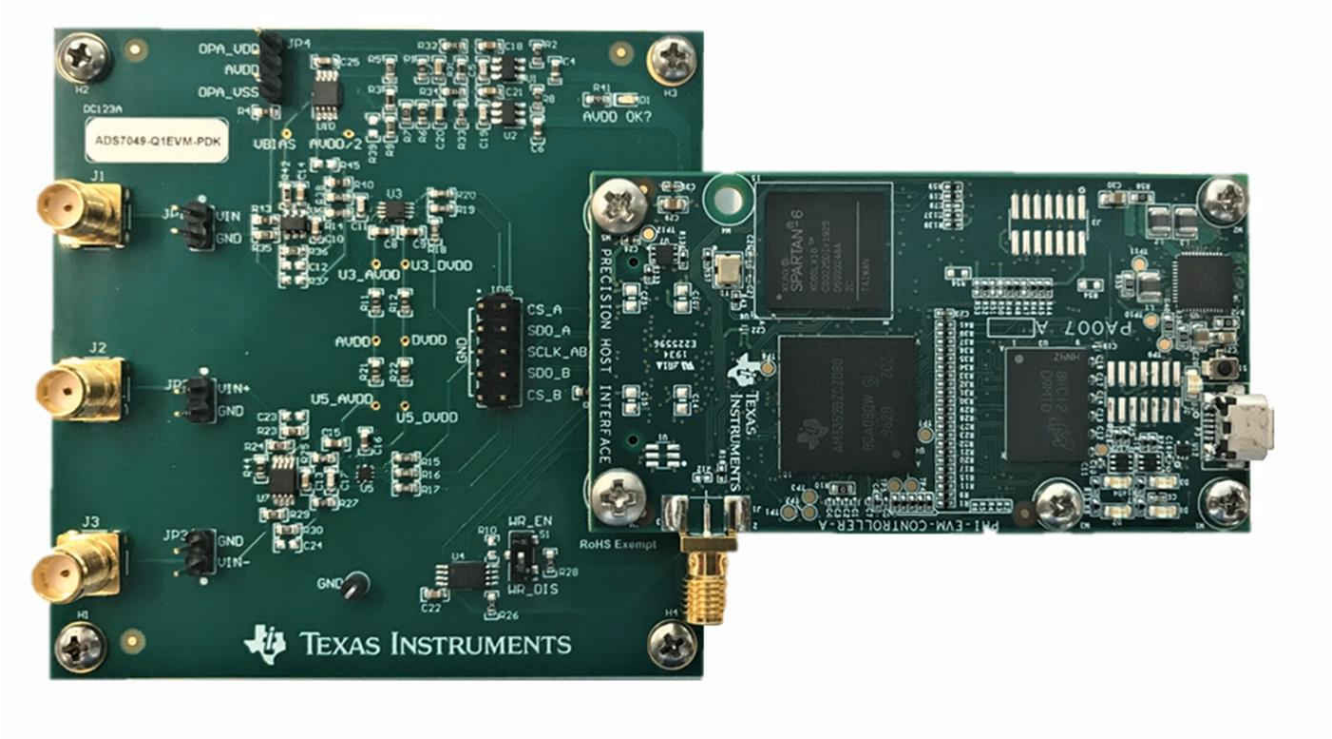
User's Guide

ADS7042EVM-PDK, ADS7049-Q1EVM-PDK, and ADS7057EVM-PDK Evaluation Module

ABSTRACT

This user's guide describes the characteristics, operation, and use of the ADS7042EVM-PDK, ADS7049-Q1EVM-PDK, and ADS7057EVM-PDK evaluation modules (EVM), referred to collectively as the *ADS704X-5XEVM-PDK*. Each kit functions as an evaluation platform for two different low-power, small-size, general-purpose successive approximation register (SAR) analog-to-digital converters (ADCs). These ADCs include the 12-bit, 1-MSPS, single-ended input ADS7042, the 12-bit, 2-MSPS, single-ended ADS7049-Q1, the 12-bit, 3-MSPS, differential input ADS7047, and the 14-bit, 2.5-MSPS, differential input ADS7057. Moreover, unique EVM design enables evaluation of the entire family of ADS704x and ADS705x devices through minor modifications. Finally, this EVM platform eases device analysis using hardware, software, and computer connectivity through the universal serial bus (USB) interface.

This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with any EVM (ADS7042EVM-PDK, ADS7049-Q1EVM-PDK, or ADS7057EVM-PDK), unless otherwise noted.



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1 ADS704X-5XEVM-PDK Overview

The ADS704X-5XEVM-PDK is a platform for evaluating the performance of the ADS704x and ADS705x family of ADCs. The ADS704X-5XEVM-PDK includes the following features:

- ADS704X-5XEVM for diagnostic testing and accurate performance evaluation of each ADC on the board
- USB powered—no external power supply is required
- A precision host interface (PHI) controller that provides a convenient communication interface to each ADC over USB 2.0 (or higher) for power delivery as well as digital input and output
- Microsoft® Windows® 8 and Windows® 10 operating systems
- Easy-to-use evaluation software for 64-bit Microsoft® Windows®
- A software suite that includes a graphical user interface (GUI) and tools for data capture, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file for post-processing

The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with each ADC
- Supplies power to all active circuitry on the ADS704X-5XEVM board

Each ADS704X-5XEVM board includes the peripheral analog circuits and components required to extract optimum performance from the ADC. Moreover, each ADS704X-5XEVM includes two complete ADC signal chains: one that supports a single-ended input ADC (see Section 2.1.1), and another that supports a differential input ADC (see Section 2.1.2). Table 1-1 defines which ADCs are populated by default on each EVM.

Table 1-1. Default ADCs Populated on Each EVM Variant

EVM Name	Single-Ended ADC (U3)	Differential ADC (U5)
ADS7042EVM-PDK	ADS7042	ADS7057
ADS7049-Q1EVM-PDK	ADS7049-Q1	ADS7047
ADS7057EVM-PDK	ADS7042	ADS7057

Additionally, the ADS704X-5XEVM includes the following features:

- External signal source from subminiature version A (SMA) connectors or header pins
- Option to use external power supplies
- Serial interface header for easy connection to the PHI controller
- Pin connections to monitor digital signals with a logic analyzer
- Two ultra-low noise, low-dropout (LDO) regulators for excellent single-supply regulation of all analog circuits
- Accommodates all package options for 14 different ADCs using four different device footprints, as per Table 1-2

Table 1-2. ADCs Supported by the ADS704X-5XEVM

Supported ADC	Populated on EVM?	Input Type	Package Options (Designator)
ADS7040	n/a	Single-ended	X2QFN (U8), VSSOP (U3)
ADS7041	n/a	Single-ended	X2QFN (U8), VSSOP (U3)
ADS7042	ADS7042EVM-PDK, ADS7057EVM-PDK	Single-ended	X2QFN (U8), VSSOP (U3)
ADS7043	n/a	Pseudo-differential	X2QFN (U8), VSSOP (U3)
ADS7044	n/a	Differential	X2QFN (U5), VSSOP (U9)
ADS7046	n/a	Single-ended	X2QFN (U8)
ADS7047	ADS7049-Q1EVM-PDK	Differential	X2QFN (U5)
ADS7052	n/a	Single-ended	X2QFN (U8)
ADS7054	n/a	Differential	X2QFN (U5)
ADS7056	n/a	Single-ended	X2QFN (U8)
ADS7057	ADS7042EVM-PDK, ADS7057EVM-PDK	Differential	X2QFN (U5)
ADS7029-Q1	n/a	Single-ended	VSSOP (U3)
ADS7039-Q1	n/a	Single-ended	VSSOP (U3)
ADS7049-Q1	ADS7049-Q1EVM-PDK	Single-ended	VSSOP (U3)

2 Introduction to the ADS704X-5XEVM

Each ADS704X-5XEVM board includes the peripheral analog circuits and components required to extract optimum performance from each ADC signal chain. Important portions of the EVM are highlighted in Figure 2-1, and described in the subsequent sections.

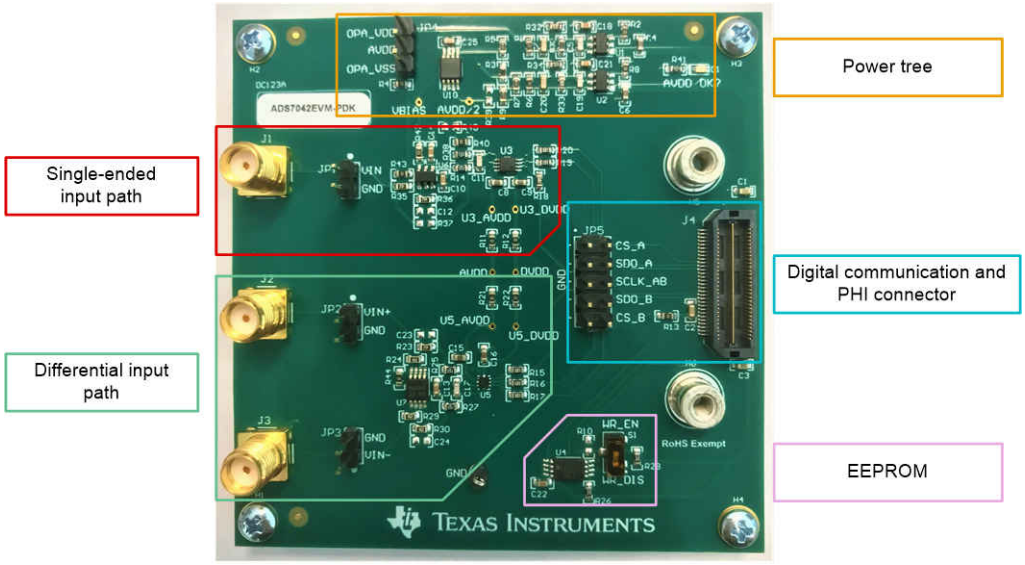

Figure 2-1. Important Subsections of the ADS704X-5XEVM

2.1 Analog Inputs

As shown in Figure 2-1, the ADS704X-5XEVM has two analog input paths: a single-ended input path highlighted in red, and a differential input path highlighted in green. SMA connectors and headers are included on each path to connect external signals. These signals feed into a driver amplifier and then to one of two ADC footprints, where the digital output is supplied to the PHI via J4.

2.1.1 Single-Ended Input Path

The single-ended input path consists of an inverting driver amplifier, an RC circuit, and two ADC footprints. Figure 2-2 shows the single-ended input path schematic.

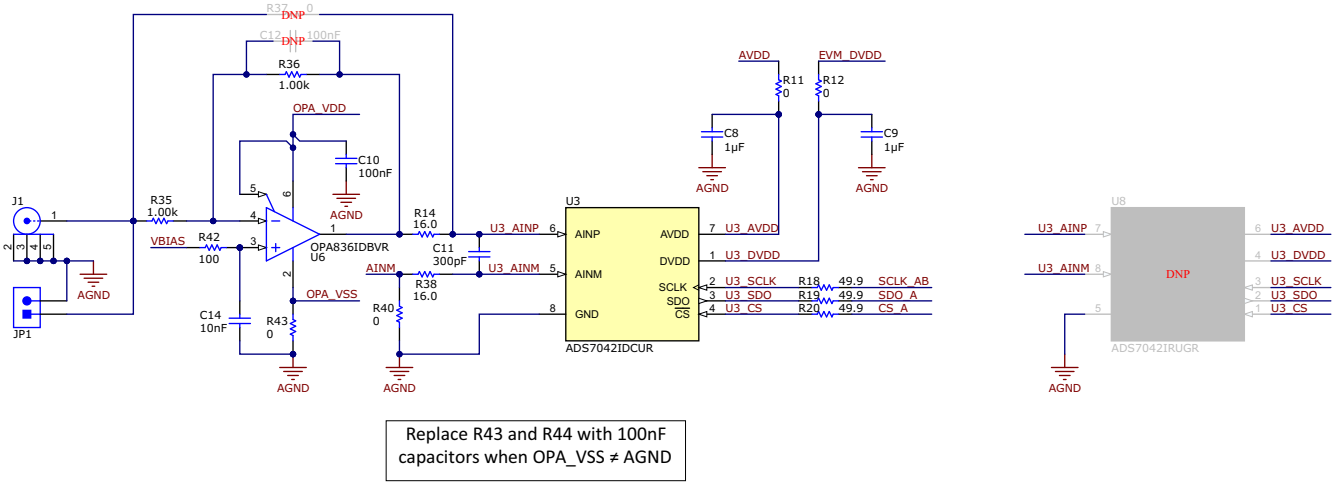

Figure 2-2. Single-Ended Input Path on the ADS704X-5XEVM

Signals connected to the single-ended input path are applied to an inverting amplifier whose common-mode voltage is set by VBIAS. The output of the amplifier connects to an RC filter (R14, R38, and C11) that then connects to the ADC input. A compensation capacitor can be added to the amplifier feedback loop via C12, but is not required for good performance. The amplifier power supplies are connected by default to the OPA_VDD and OPA_VSS supplies. Section 2.2 explains how to modify the EVM to use external supplies. If desired, the amplifier can be bypassed by populating R37 with a 0-Ω resistor and removing R14 and R35.

Figure 2-2 also depicts all connections to the ADC (U3). Each power-supply connection has a 1-µF decoupling capacitor. The supply connections also have a series 0-Ω resistor that can be removed for the purpose of making external current measurements. Moreover, each digital input has a 49.9-Ω series resistor. These resistors smooth the edges of the digital signals to minimize overshoot and ringing.

Finally, Figure 2-2 identifies a do-not-populate (DNP) component in U8. This ADC footprint is on the bottom of the board and can be used to evaluate any single-ended ADC in an X2QFN package listed in Table 1-2. However, ensure that any device in U3 is cleanly removed before soldering a device in U8. Section 4.6 explains how to use the ADS704X-5XEVM GUI to update the EEPROM when the ADC is replaced.

2.1.2 Differential Input Path

The differential input path consists of a differential driver amplifier, an RC circuit, and two ADC footprints. Figure 2-3 shows the differential input path schematic.

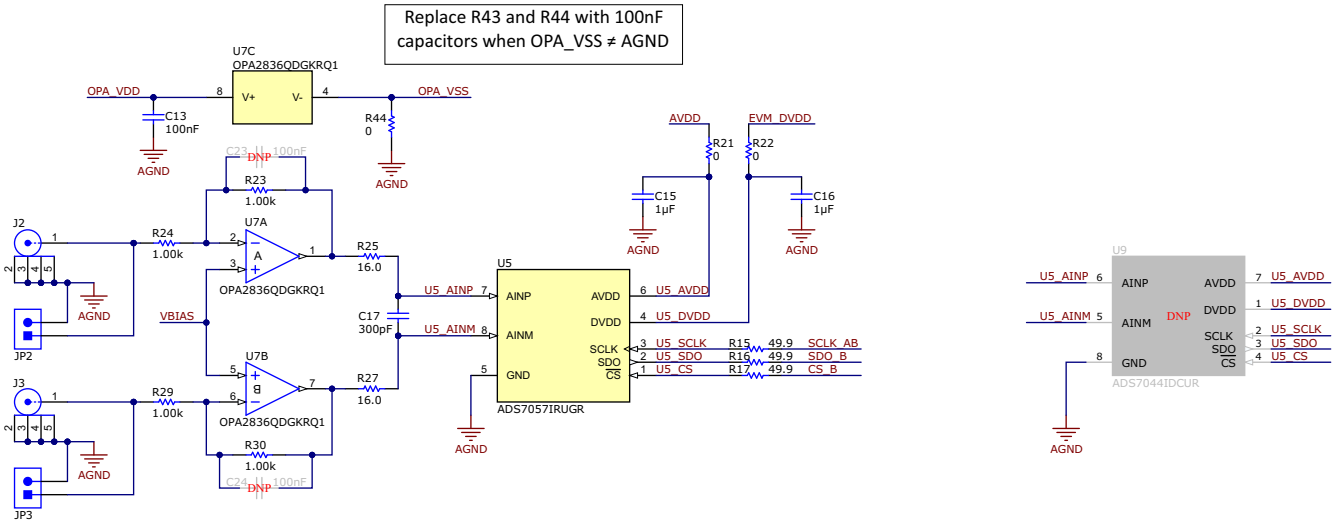

Figure 2-3. Differential Input Path on the ADS704X-5XEVM

Signals connected to the differential input path are applied to a differential amplifier in an inverting configuration whose common-mode voltage is set by VBIAS. The output of the amplifier connects to an RC filter (R25, R27, and C17) that then connects to the ADC input. Each amplifier feedback loop has an option for a compensation capacitor via C23 or C24, but these capacitors are not required for good performance. The amplifier power supplies are connected by default to the OPA_VDD and OPA_VSS supplies. Section 2.2 explains how to modify the EVM to use external supplies.

Figure 2-3 also shows all connections to the ADC (U5). Each power-supply connection has a 1-µF decoupling capacitor. The supply connections also have a series 0-Ω resistor that can be removed for the purpose of making external current measurements. Moreover, each digital input has a 49.9-Ω series resistor. These resistors smooth the edges of the digital signals to minimize overshoot and ringing.

Finally, Figure 2-3 identifies a do-not-populate (DNP) component in U9. This ADC footprint is on the bottom of the board and can be used to evaluate any differential ADC in a VSSOP package in Table 1-2. However, ensure that any device in U5 is cleanly removed before soldering a device in U9. Section 4.6 explains how to use the ADS704X-5XEVM GUI to update the EEPROM when the ADC is replaced.

2.2 Power Supplies

The default state of the EVM has all power supplies derived from the USB power and delivered by the PHI controller. The 3.3-V ADC digital supply voltage (DVDD) is provided by the PHI via pin 50 on J4 (see Figure 2-7). The PHI also provides a regulated 5.5-V power rail that feeds into two LDOs on the EVM. These LDOs generate a low-noise, 3.6-V (nominal) supply voltage for the amplifier (OPA_VDD) and a low-noise, 3.3-V (nominal) analog supply voltage for the ADC (AVDD). Figure 2-4 shows the two LDO circuits used on the ADS704X-5XEVM.

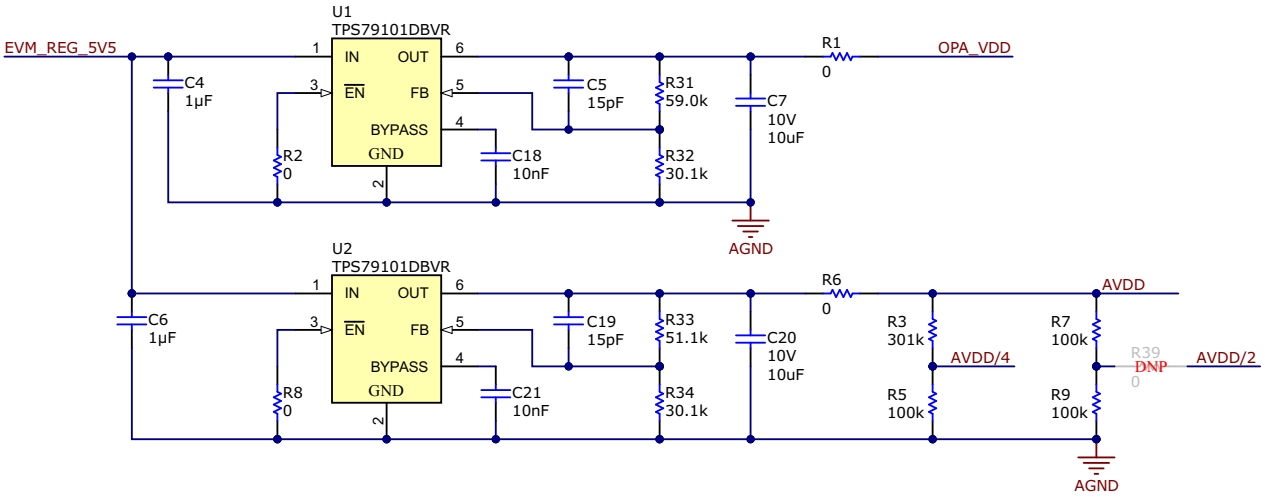

Figure 2-4. Power Tree on the ADS704X-5XEVM

In Figure 2-4, the top LDO (U1) has an adjustable output set by resistors R31 and R32 while the bottom LDO (U2) has an adjustable output set by resistors R33 and R34. Modify these resistor values if a different OPA_VDD or AVDD voltage is desired. Ensure that the input, absolute, and common-mode voltage limitations for all components are within data sheet limits when modifying the power supplies. See the LDO data sheet for more information on how to choose resistor values for a specific output voltage.

If external power supplies are desired, remove resistors R1 and R6 in Figure 2-4 to disconnect both LDOs from the power-supply circuit. Connector JP4 in Figure 2-5 can then be used to provide direct power to OPA_VDD, AVDD, and OPA_VSS.

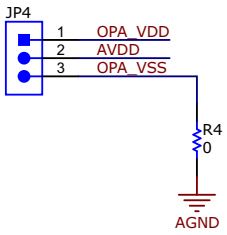

Figure 2-5. External Power-Supply Header on the ADS704X-5XEVM

If OPA_VSS is connected to any voltage other than AGND, remove R4 in Figure 2-5 and replace R43 and R44 per the instructions in Figure 2-2. Another important consideration if OPA_VSS is modified is that the V– input (pin 4) on the buffer amplifier in Figure 2-6 is hard-wired to AGND and is therefore unaffected when the voltage on OPA_VSS is changed.

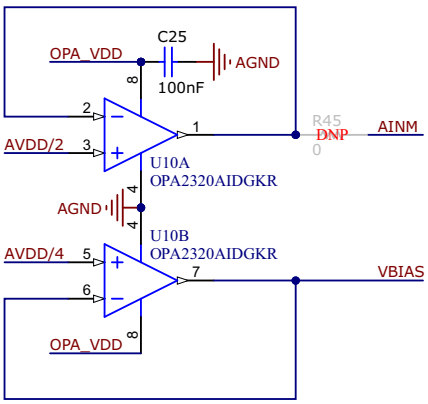

Figure 2-6. Buffer Amplifier Circuit on the ADS704X-5XEVM

The buffer amplifier in Figure 2-6 prevents the AVDD/4 resistor divider (R3 and R5) from loading the amplifier inputs and the AVDD/2 resistor divider (R7 and R9) from loading the ADC inputs (see Figure 2-4). As per Section 2.1.1, VBIAS sets the driver amplifier common-mode voltage for both signal paths. AINM is only required if U3 or U5 in Figure 2-2 is populated with the ADS7043. This specific ADC has a pseudo-differential input that requires the AINM pin to be set to AVDD / 2 ±100 mV.

When the ADS7043 is used on the ADS704X-5XEVM:

- Populate R39 in Figure 2-4 with a 0-Ω resistor
- Populate R45 in Figure 2-6 with a 0-Ω resistor
- Depopulate R40 in Figure 2-2

2.3 Digital Interface and Communication

The EVM interfaces with the PHI and communicates with the computer over the USB. There are three devices on the EVM with which the PHI communicates: the two ADCs (over SPI) and the EEPROM (over I^2C). The EEPROM comes preprogrammed with the information required to configure and initialize each ADC populated by default on the ADS704X-5XEVM. Therefore, communication with the EEPROM is only required if the user removes and replaces one of the default ADCs. See Section 2.4 for more information.

All ADCs supported by the ADS704X-5XEVM use SPI serial communication in mode 1 (CPOL = 0, CPHA = 1). The ADS704X-5XEVM offers 49.9-Ω resistors between the SPI signals to aid with signal integrity (see Figure 2-2) because the serial clock (SCLK) frequency can be as fast as 60 MHz. Typically, in high-speed SPI communication, fast signal edges can cause overshoot; these 49.9-Ω resistors slow down the signal edges to minimize signal overshoot. JP5 provides test points to measure the digital signals, as illustrated in Figure 2-7.

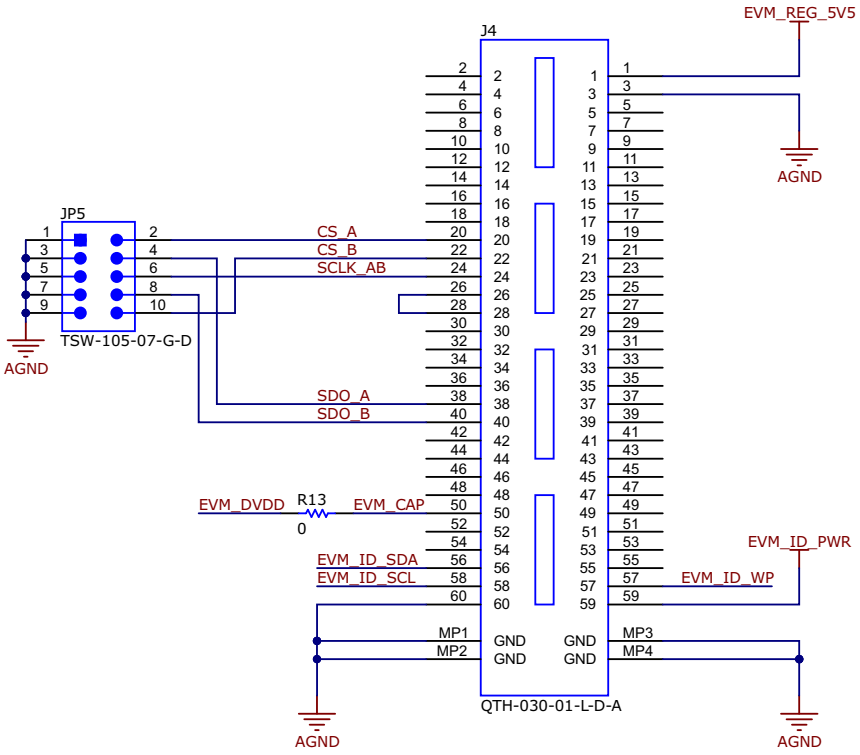

Figure 2-7. Digital Communication and PHI Connector on the ADS704X-5XEVM

2.4 I²C Bus for Onboard EEPROM

The circuit shown in Figure 2-8 is used with the PHI board to identify the specific ADCs populated on the EVM and enable the correct GUI settings. The user does not need to modify or interact with this circuit during EVM operation. As a result, switch S1 is set by default to enable the EEPROM write protect and must not be altered unless the ADC is modified as per Section 2.1.1 or Section 2.1.2. Update the EEPROM when the ADC is replaced using the ADS704X-5XEVM GUI, as per Section 4.6.

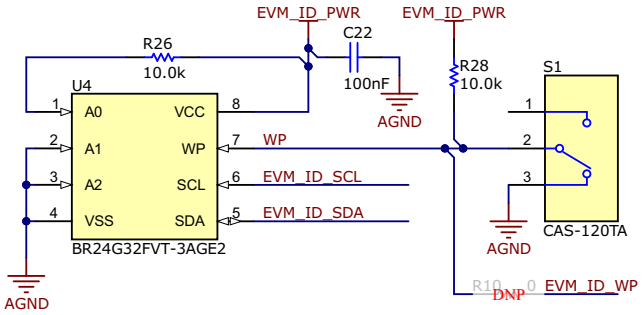

Figure 2-8. EEPROM Circuit on the ADS704X-5XEVM

3 ADS704X-5XEVM Software Installation

Download the latest version of the EVM GUI installer from the *Order & Start Development* section of the ADS7042EVM-PDK, ADS7049-Q1EVM-PDK, or ADS7057EVM-PDK tool folder. Run the GUI installer to install the EVM GUI software on your computer.

Note

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message may appear or the *installer.exe* file may be deleted.

As shown in Figure 3-1, accept the license agreements and follow the on-screen instructions to complete the installation.

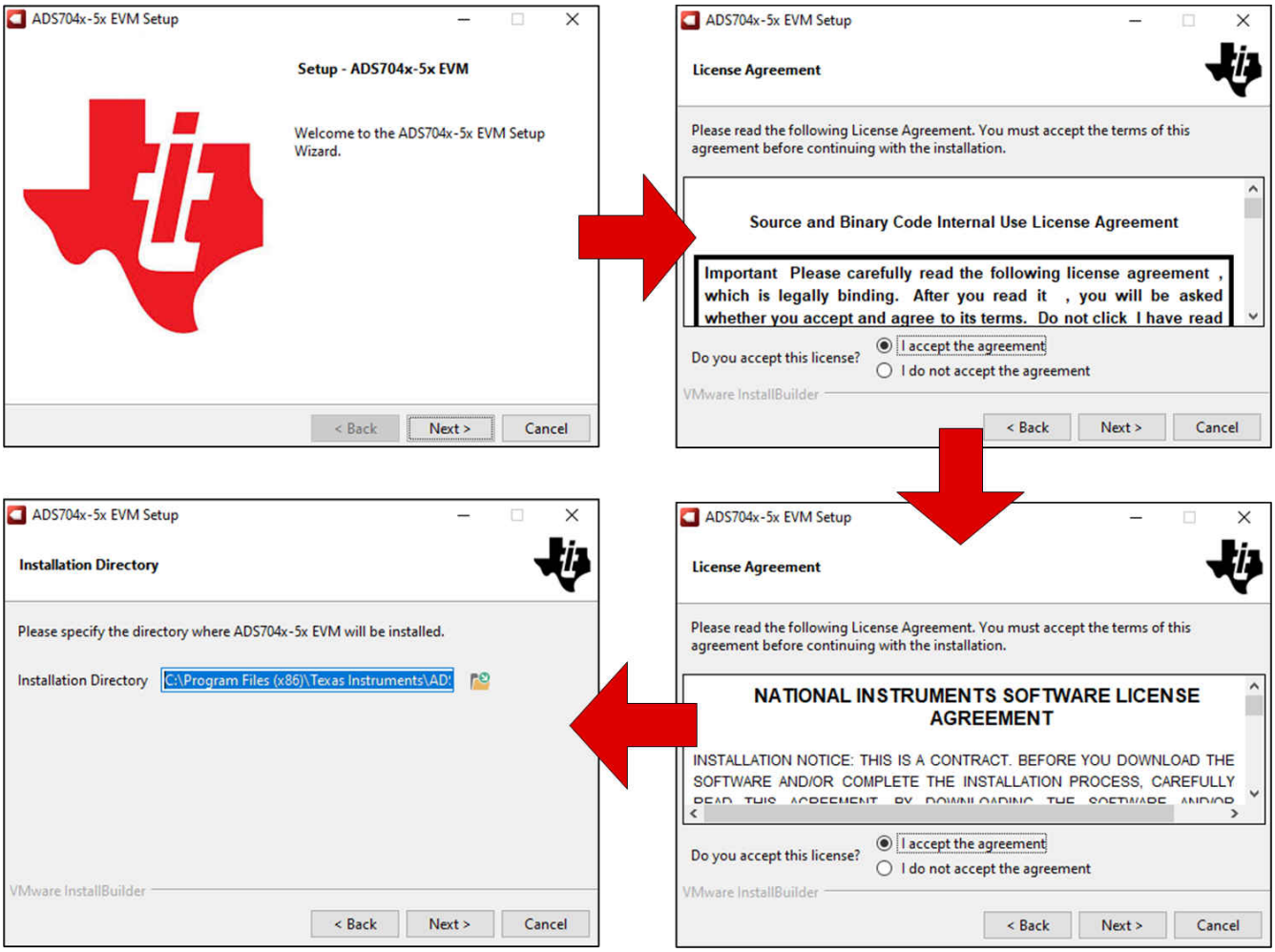

Figure 3-1. Software Installation and Prompts

As part of the ADS704X-5XEVM GUI installation, a prompt with a *Device Driver Installation* appears on the screen, as shown in Figure 3-2. Click *Next* to proceed.

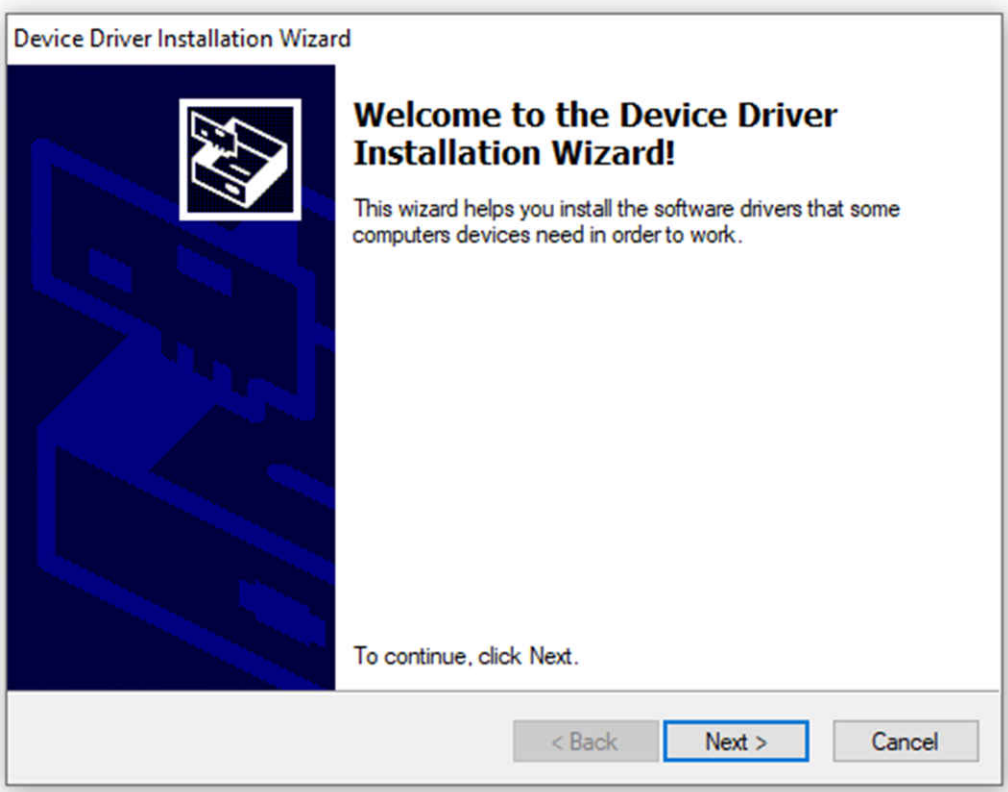

Figure 3-2. Device Driver Installation

The ADS704X-5XEVM requires the LabVIEW™ run-time engine and may prompt for the installation of this software, as shown in Figure 3-3, if not already installed.

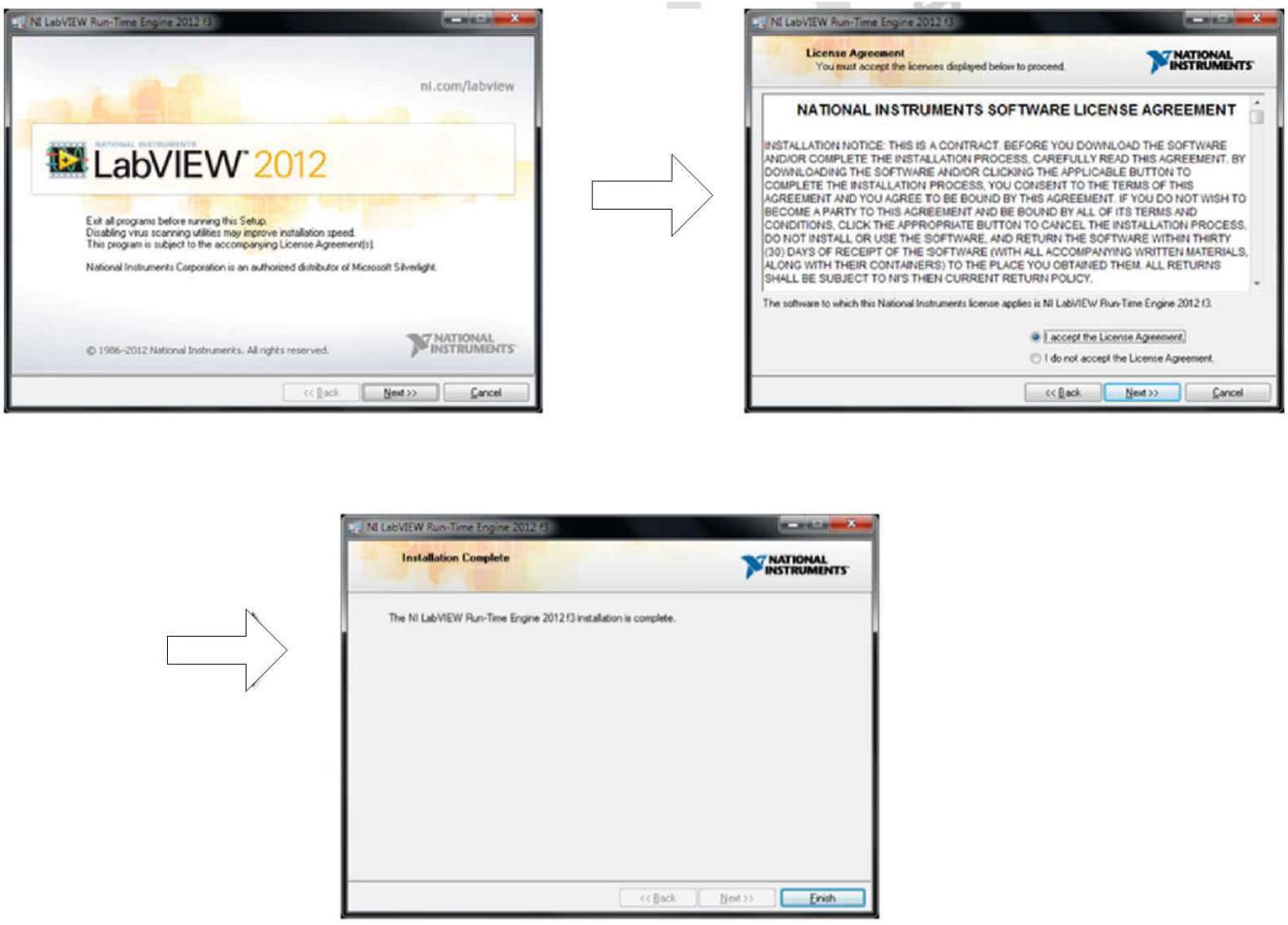

Figure 3-3. LabVIEW™ Run-Time Engine Installation

4 EVM Operation

4.1 Connecting the Hardware

After installing the software, connect the EVM as shown in Figure 4-1:

1. Physically connect P2 of the PHI to J4 of the ADS704X-5XEVM. Install the screws to ensure a robust connection
2. Connect the USB cable from the PHI to the computer first:
   a. LED D5 on the PHI lights up, indicating that the PHI is powered
   b. LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC; Figure 4-1 shows the resulting LED indicators
3. Start the software GUI. The LEDs blink slowly as the FPGA firmware is loaded on the PHI. This loading takes a few seconds and then the AVDD and DVDD power supplies turn on. LED D1 on the ADS704X-5XEVM (as shown in Figure 4-1) illuminates green to indicate that AVDD is being supplied to the EVM
4. Connect the signal generator. The input range varies for the different ADCs, but is typically 0 V to AVDD for single-ended devices or –AVDD to +AVDD for differential devices. Check the specific ADC data sheet for more information about allowable input ranges. In any case, adjust the input signal to just below full-scale range to avoid clipping
   a. Texas Instruments offers the PSIEVM as a precision signal generator if such a source is otherwise unavailable to the user. The PSIEVM can be used to generate clean sinusoidal input signals for the ADS704X-5XEVM to verify AC performance specifications.

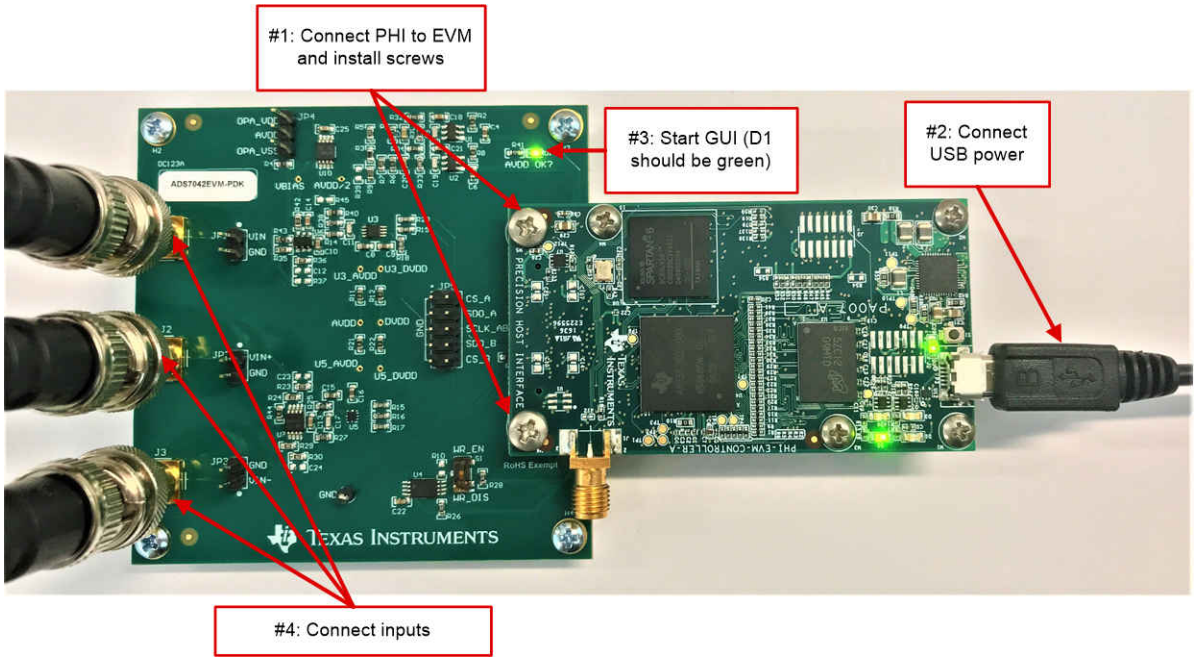

Figure 4-1. Hardware Connections on the ADS704X-5XEVM

4.2 EVM GUI Global Settings for ADC Control

Figure 4-2 shows the default screen when the GUI is started. The GUI defaults to the *Time Domain Display*, though other options are available in the *Pages* control box. When the GUI connects successfully, *HW Connected* shows in green in the bottom ribbon and the specific devices included on the EVM are identified in the upper right. In this case, ADS7049-Q1 and ADS7047 are included on the EVM represented by Figure 4-2.

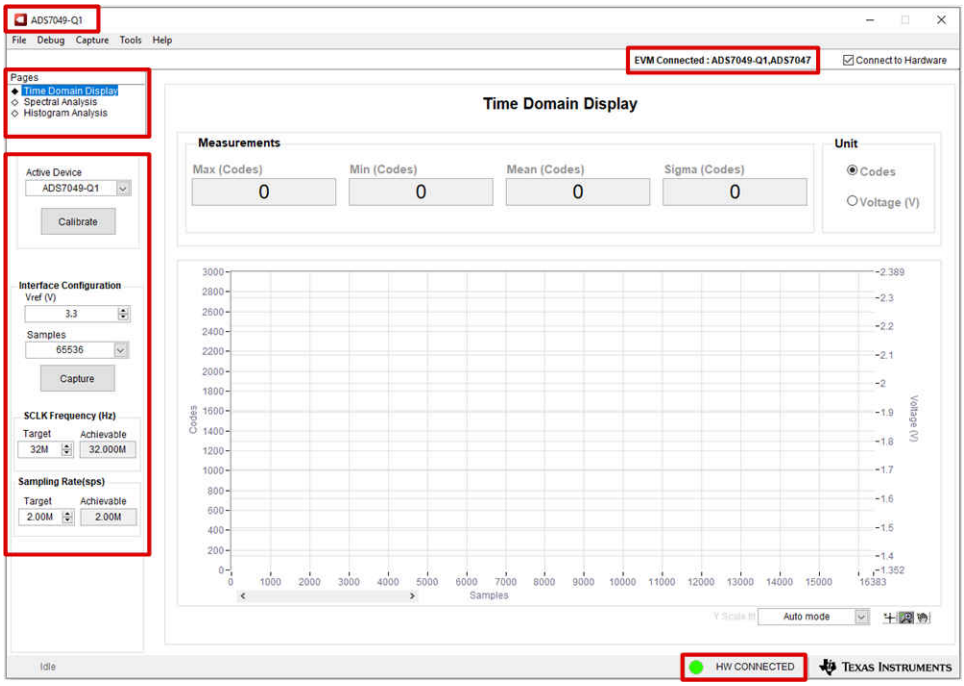

Figure 4-2. ADS704X-5XEVM GUI Overview

The EVM global controls are located on the left-hand side of the GUI and are as follows:

- *Active Device* (also shown in the upper left corner of the GUI)
- *VREF* (only valid if AVDD is modified from the default value as per Section 2.2, otherwise leave this value set to 3.3 V)
- *Samples*
- *SCLK Frequency*
- *Sampling Rate*

4.3 Time Domain Display

The *Time Domain Display* tool visualizes the ADC response to a given input signal. This tool is useful for both studying the behavior of and debugging any gross problems with the ADC or drive circuits, such as waveform clipping.

Trigger a data capture of the selected number of samples by using the *Capture* button highlighted in Figure 4-3. The GUI plots a waveform based on the input signal. The waveform is plotted by *Samples* on the x-axis against *Codes* and *Voltage* on the left and right y-axes, respectively. *Voltage* is relative to the specified reference voltage, which for all devices in Table 1-2 is just the AVDD voltage. Switching *Pages* to any of the analysis tools described in the subsequent sections causes calculations to be performed on the same set of data.

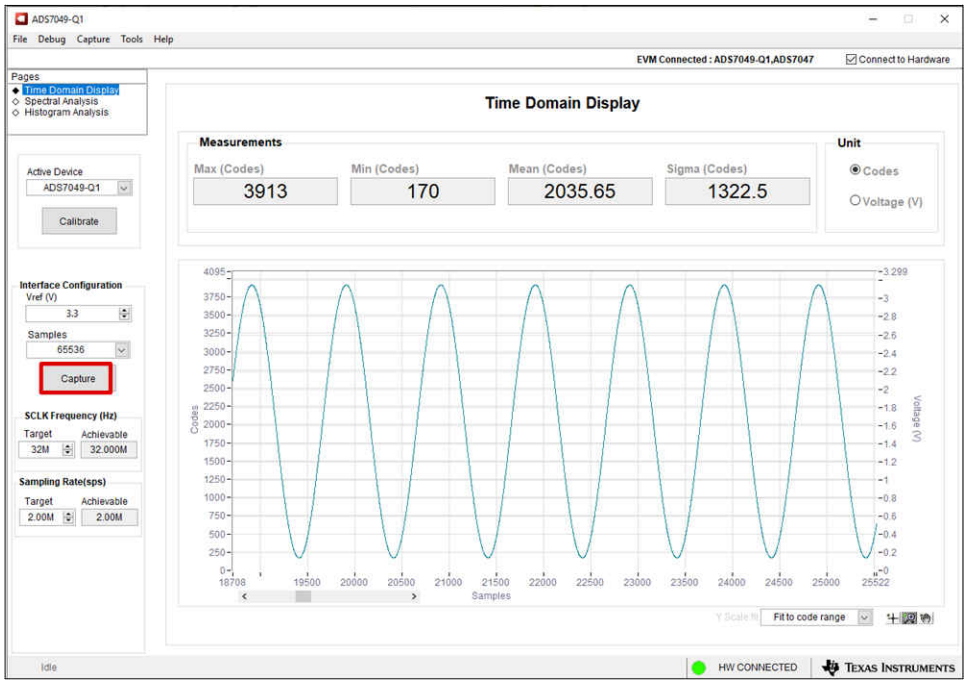

Figure 4-3. Time Domain Display in the ADS704X-5XEVM GUI

4.4 Spectral Analysis

The *Spectral Analysis* tool shown in Figure 4-4 is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-Term Blackman-Harris window is the default option and has sufficient dynamic range to resolve the frequency components of all ADCs included in Table 1-2. The *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

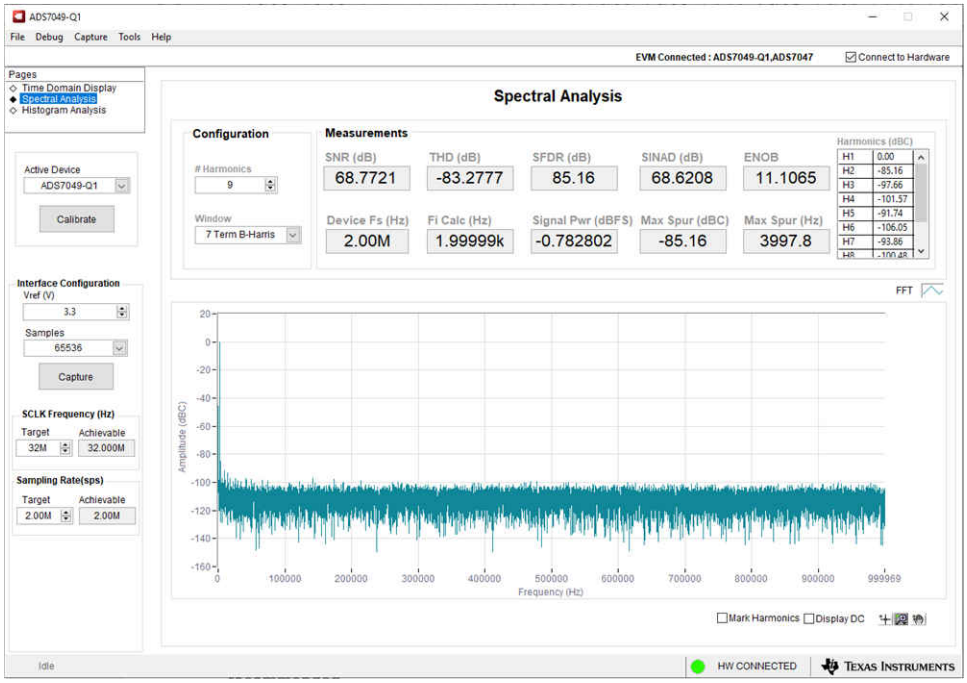

Figure 4-4. Spectral Analysis in the ADS704X-5XEVM GUI

As noted in step 4.a in Section 4.1, Texas Instruments offers the PSIEVM as a precision signal generator if such a source is otherwise unavailable to the user. The PSIEVM can be used to generate clean sinusoidal input signals for the ADS704X-5XEVM to verify AC performance specifications.

4.5 Histogram Analysis

Noise degrades ADC resolution and the *Histogram Analysis* tool can be used to visualize the ADC noise performance. Noise couples to the ADC output from sources such as the input drive circuits, the ADC power supply, and the ADC itself. The cumulative effect of this noise is reflected in the standard deviation of the ADC output code histogram obtained by performing multiple conversions of a DC input. As shown in Figure 4-5, click the *Capture* button to display a histogram corresponding to a DC input.

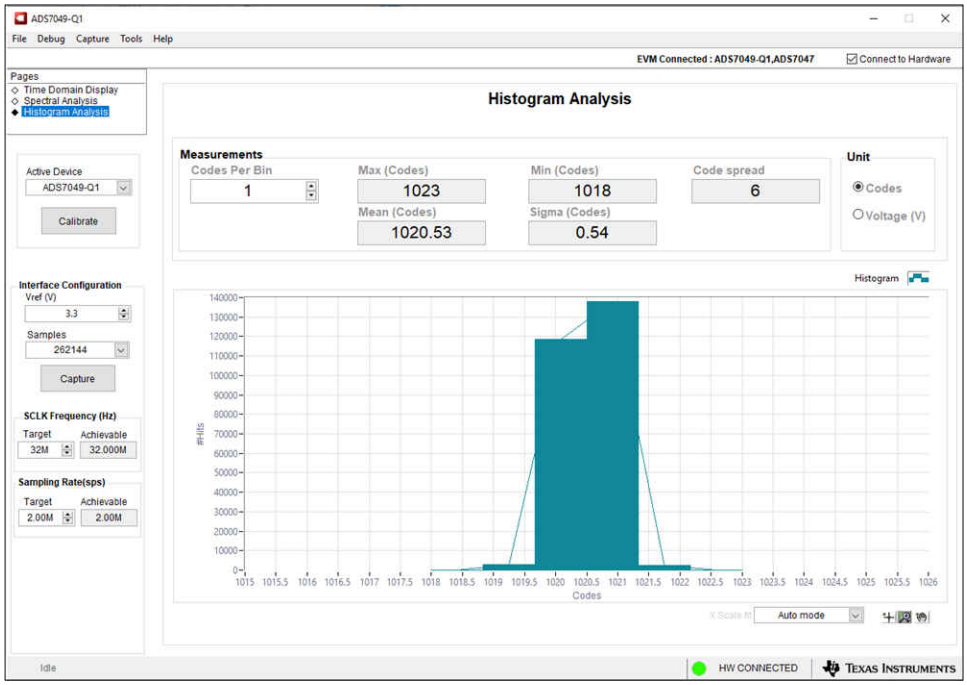

Figure 4-5. Histogram Analysis in the ADS704X-5XEVM GUI

4.6 Updating EEPROM After ADC Replacement

As discussed in Section 1, the ADS704X-5XEVM can support operation of the 14 different ADCs shown in Table 1-2. See Section 2.1.1 for information about the required hardware modifications for replacing a single-ended input ADC and Section 2.1.2 for information about the required hardware modifications for replacing a differential input ADC.

When the hardware modifications are complete, update the EEPROM so the GUI reflects the newly installed devices on the EVM. Follow these steps to update the EEPROM from the ADS704X-5XEVM GUI:

1. Set switch S1 to write enable by pushing the switch closest to the *WR_EN* silkscreen text (see Figure 2-1)
2. Navigate to *Tools* → *Load EEPROM* in the menu at the top left of the GUI
3. In the pop-up window illustrated in Figure 4-6, select the appropriate device for both ADC A (U3 or U8) and ADC B (U5 or U9)
   a. ADC A corresponds to the single-ended input path and ADC B corresponds to the differential input path
4. Click the *Load EEPROM* button in the pop-up window
5. Verify the EEPROM loaded correctly by reviewing the ADC name in the upper left corner of the GUI, the supported devices in the upper right of the GUI, and the *Active Device* drop-down menu (see Figure 4-7)
   a. In this example, ADC A was changed from ADS7049-Q1 to ADS7040 and ADC B was changed from ADS7047 to ADS7044
6. Set switch S1 to write disable by pushing the switch closest to the *WR_DIS* silkscreen text (see Figure 2-1)

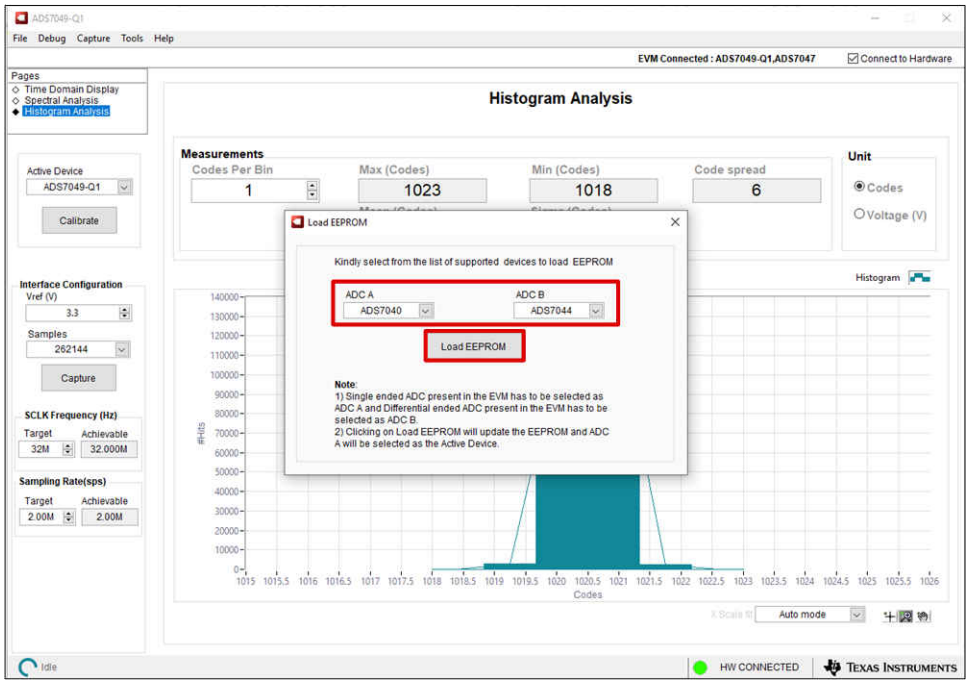

Figure 4-6. Selecting the ADCs and Loading the EEPROM

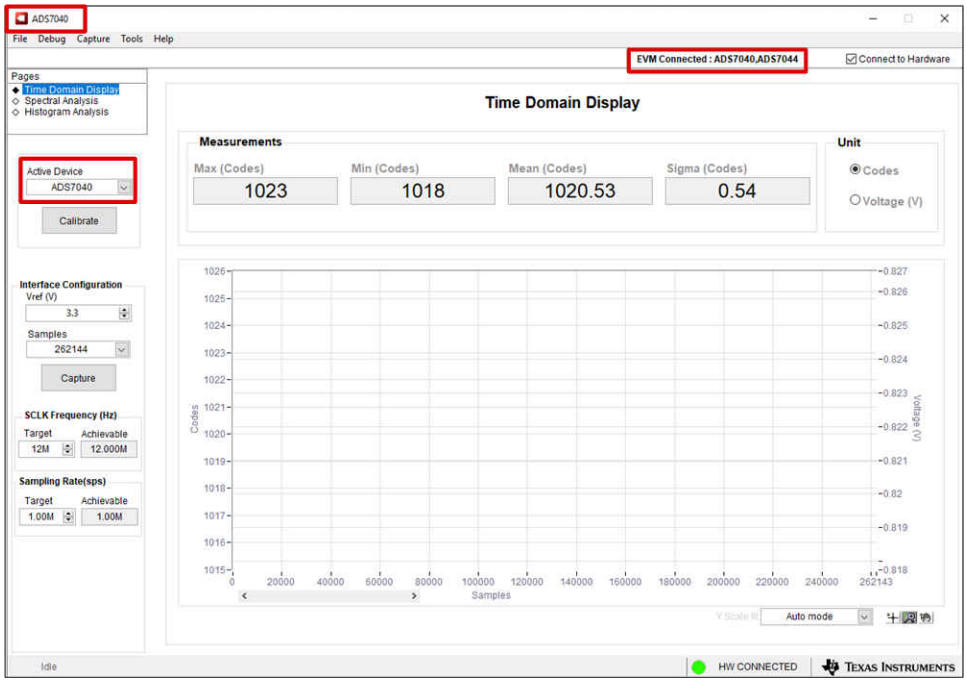

Figure 4-7. GUI Main Screen After EEPROM is Updated Successfully

5 Bill of Materials, Layout, and Schematic

This section contains the ADS704X-5XEVM bill of materials, PCB layout, and the EVM schematic.

5.1 Bill of Materials

Table 5-1 lists the bill of materials (BOM) for the ADS704X-5XEVM.

Table 5-1. Bill of Materials

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
!PCB	1		Printed Circuit Board		DC123	Any
!PCB2	1		PHI-EVM-CONTROLLER	N/A	PA007A	Any
@H1, @H2, @H3, @H4	4		Hex Standoff, #4-40, Aluminum, 1/4"	1/4 inch Aluminum Hex Standoff	1891	Keystone
@H5, @H6	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL
C1, C2, C3, C7, C20	5	10uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0603	0603	GRM188R61A106ME69D	MuRata
C4, C6, C8, C9, C15, C16	6	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet
C5, C19	2	15pF	CAP, CERM, 15 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	C0603C150J5GACTU	Kemet
C10, C13, C22, C25	4	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	0603	C0603C104J3RACTU	Kemet
C11, C17	2	300pF	CAP, CERM, 300 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H301JA01D	MuRata
C14, C18, C21	3	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 5%, X7R, 0603	0603	C0603C103J5RACTU	Kemet
D1	1	Green	LED, Green, SMD	1.6x0.8x0.8mm	LTST-C190GKT	Lite-On
H1, H2, H3, H4	4		MACHINE SCREW PAN PHILLIPS 4-40	Machine Screw, 4-40, 1/4 inch	PMSSS 440 0025 PH	B&F Fastener Supply
H5, H6	2		ROUND STANDOFF M3 STEEL 5MM	ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik
J1, J2, J3	3		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF
J4	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A	Samtec
JP1, JP2, JP3	3		Header, 100mil, 2x1, Gold, TH	Header, 2x1, 100mil	5-146261-1	TE Connectivity
JP4	1		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
JP5	1		Header, 100mil, 5x2, Gold, TH	5x2 Header	TSW-105-07-G-D	Samtec
LBL1	1			PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
R1, R2, R4, R6, R8, R11, R12, R13, R21, R22, R40, R43, R44	13	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
R3	1	301k	RES, 301 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD07301KL	Yageo America

Table 5-1. Bill of Materials (continued)

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
R5, R7, R9	3	100k	RES, 100 k, 0.1%, 0.063 W, 0603	0603	CPF0603B100KE	TE Connectivity
R14, R25, R27, R38	4	16.0	RES, 16.0, 0.1%, 0.1 W, 0603	0603	RT0603BRD0716RL	Yageo America
R15, R16, R17, R18, R19, R20	6	49.9	RES, 49.9, 1%, 0.1 W, 0603	0603	RC0603FR-0749R9L	Yageo
R23, R24, R29, R30, R35, R36	6	1.00k	RES, 1.00 k, 0.1%, 0.1 W, 0603	0603	RT0603BRB071KL	Yageo America
R26, R28	2	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R31	1	59.0k	RES, 59.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0759KL	Yageo
R32, R34	2	30.1k	RES, 30.1 k, 1%, 0.1 W, 0603	0603	RC0603FR-0730K1L	Yageo
R33	1	51.1k	RES, 51.1 k, 1%, 0.1 W, 0603	0603	RC0603FR-0751K1L	Yageo
R41	1	470	RES, 470, 5%, 0.1 W, 0603	0603	RC0603JR-07470RL	Yageo
R42	1	100	RES, 100, 0.1%, 0.1 W, 0603	0603	RT0603BRD07100RL	Yageo America
S1	1		Switch, Slide, SPDT 100mA, SMT	Switch, 5.4x2.5x2.5mm	CAS-120TA	Copal Electronics
TP1	1		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
U1, U2	2		Single Output High PSRR LDO, 100 mA, Adjustable 1.2 to 5.5 V Output, 2.7 to 5.5 V Input, 6-pin SOT-23 (DBV), -40 to 125 degC	DBV0006A	TPS79101DBVR	Texas Instruments
U3[1]	1		12-Bit 1MSPS Ultra-Low-Power Ultra-Small-Size SAR ADC With SPI Interface (VSSOP-8)	DCU0008A	ADS7042IDCUR	Texas Instruments
U4	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm
U5[2]	1		Ultra-Low Power, Ultra-Small Size, 14-Bit, High-Speed SAR ADC, RUG0008A (X2QFN-8)	RUG0008A	ADS7057IRUGR	Texas Instruments
U6	1		Very Low Power, Rail to Rail Out, Negative Rail In, VFB Operational Amplifier, 2.5 to 5.5 V, -40 to 125 degC, 6-pin SOT23 (DBV6)	DBV0006A	OPA836IDBVR	Texas Instruments
U7	1		Automotive, Dual, Very Low Power, Rail to Rail output, VFB Op Amp, DGK0008A (VSSOP-8)	DGK0008A	OPA2836QDGKRQ1	Texas Instruments
U10	1		Precision, Zero-Crossover, 20MHz, 0.9pA Ib, RRIO, CMOS Operational Amplifier (VSSOP-8)	DGK0008A	OPA2320AIDGKR	Texas Instruments
C12, C23, C24	0	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	0603	C0603C104J3RACTU	Kemet
R10, R37, R39, R45	0	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
U8	0		12-Bit, 1-MSPS, Ultra-Low-Power & Ultra-Small-Size SAR ADC with SPI Interface (X2QFN-8)	RUG0008A	ADS7042IRUGR	Texas Instruments
U9	0		Ultra-Low Power, Ultra-Small Size, 12-Bit, 1-MSPS, SAR ADC	VSSOP8	ADS7044IDCUR	Texas Instruments

1. ADS7049QDCURQ1 on the ADS7049-Q1EVM-PDK.
2. ADS7047IRUGR on the ADS7049-Q1EVM-PDK.

5.2 Layout

Figure 5-1 through Figure 5-7 show the layout for the ADS704X-5XEVM.

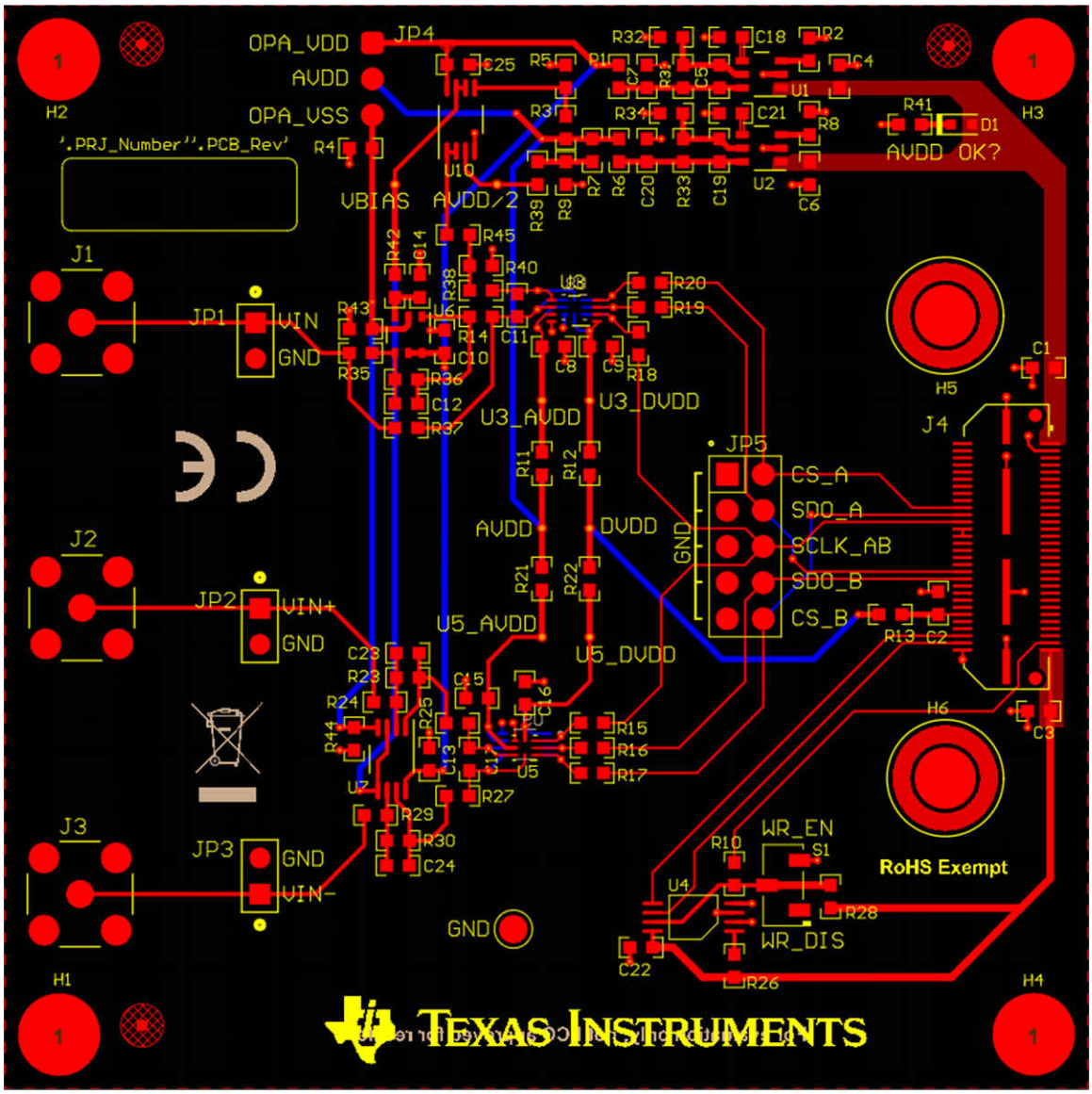

Figure 5-1. Composite PCB Layout

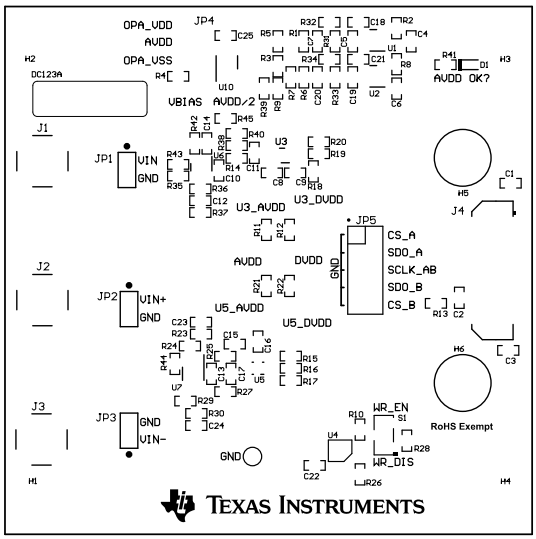

Figure 5-2. Top Overlay

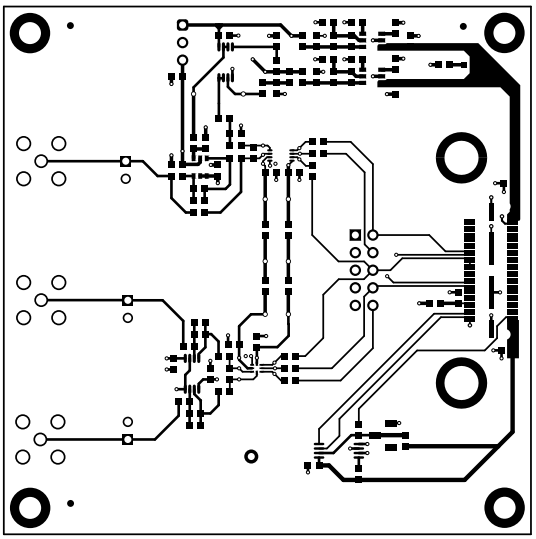

Figure 5-3. Top Layer

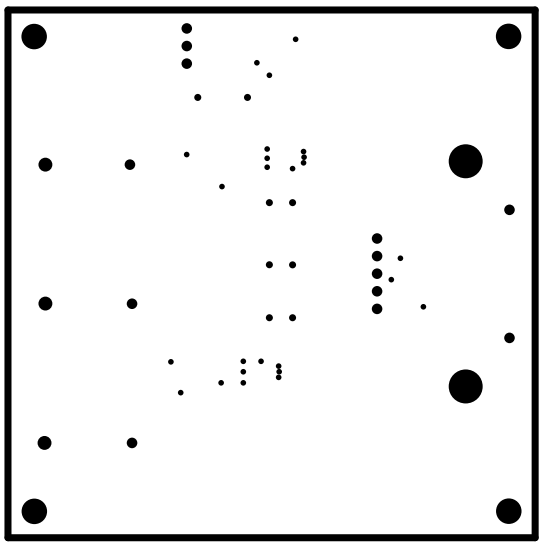

Figure 5-4. Inner Ground Plane 1

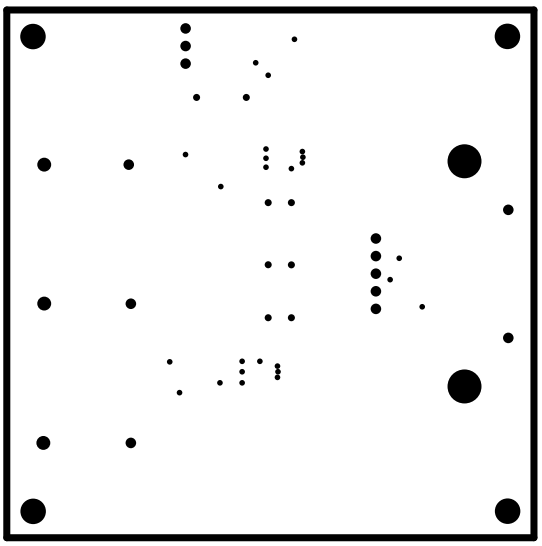

Figure 5-5. Inner Ground Plane 2

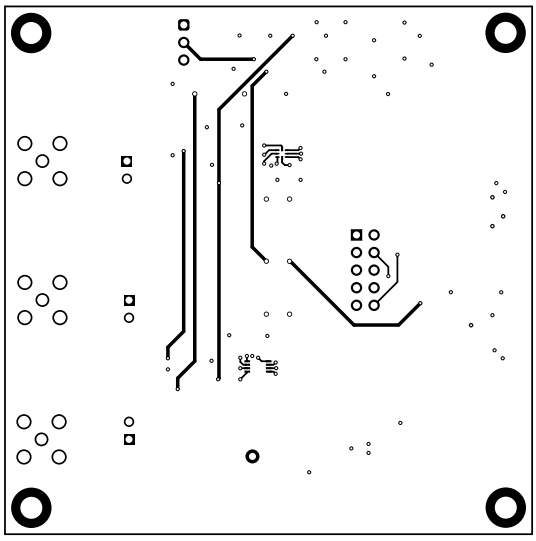

Figure 5-6. Bottom Layer

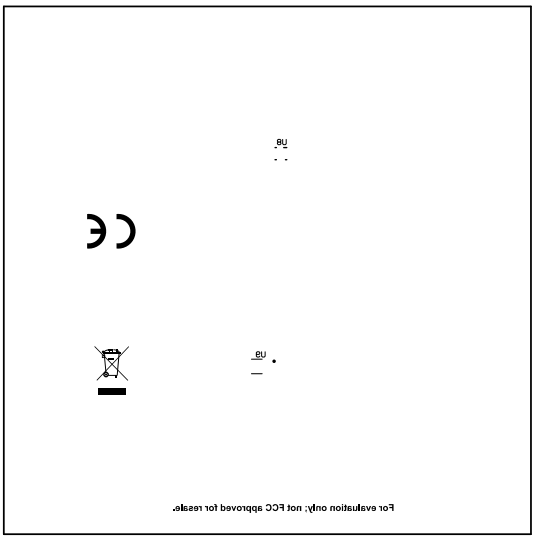

Figure 5-7. Bottom Overlay

5.3 Schematic

Figure 5-8 shows the schematic for the ADS704X-5XEVM.

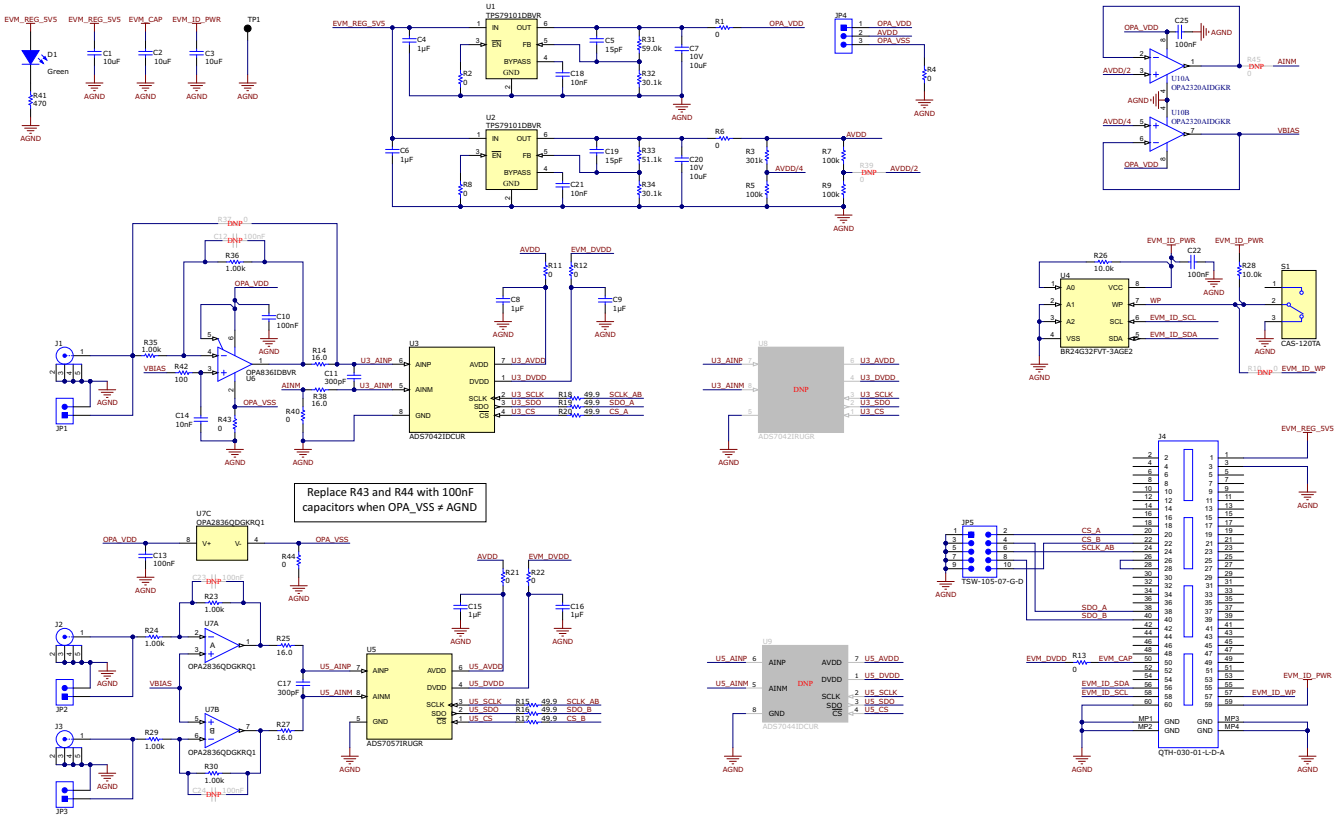

Figure 5-8. ADS704X-5XEVM Schematic

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2021) to Revision A (January 2022)	Page
• Changed first paragraph of *ADS704X-5XEVM Software Installation* section	10

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