EVM User's Guide: AFE7900EVM AFE7920EVM TSW14J58EVM

AFE79xx Evaluation Module

Description

The AFE79xx evaluation modules (EVMs) are evaluation boards used to evaluate the AFE79xx family of integrated RF Sampling transceivers from Texas Instruments. The AFE79xx devices support up to four-transmit, four-receive, and two feedback channels (4T4R2F) and integrates phase-locked loop (PLL) and voltage-controlled oscillator (VCO) for generating data converter clocks. The AFE79xx device integrates eight JESD204B-, JESD204C-compatible serializer/deserializer (SerDes) transceivers capable of running up to 29.5Gbps to transmit and receive digital data through the onboard FPGA mezzanine card (FMC) connector.

The EVM includes the LMK04828 clock generator to provide reference clocks and SYSREF to the analog front end (AFE) and capture card (field-programmable gate array, FPGA). The evaluation module (EVM) works off a single 5.5V input and includes complete power management circuitry. External clocking options include support for feeding the reference clock (for the on-chip PLL). The design interfaces with the TI pattern and capture card solution (TSW14J58), as well as many FPGA development kits.

Features

- Onboard FPGA mezzanine card (FMC) connector
- Includes complete power management circuitry
- Onboard clock generator to provide reference clocks and SYSREF
- Internal PLL/VCO to generate DAC/ADC clocks
- Optional external CLK at DAC or ADC rate
- SerDes data interface:
  - JESD204B and JESD204C compliant
  - 8 SerDes transceivers up to 29.5Gbps
  - 8b/10b and 64b/66b encoding
  - 12-bit, 16-bit, 24-bit, and 32-bit resolution
  - Subclass 1 multi-device synchronization

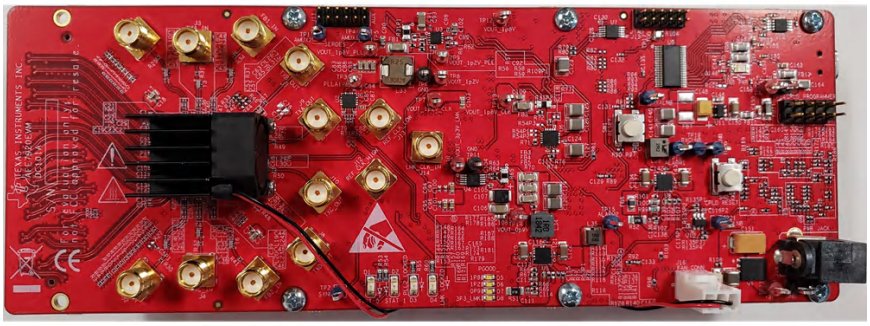

Figure 1-1. AFE79xxEVM Top View

1 EVM Overview

1.1 Caution and Warnings

	**WARNING** Moving parts. Do not touch the spinning disk or motor during operation.
	**WARNING** Hot surface. Contact can cause burns. Do not touch.

1.2 Introduction

The AFE79xxEVM includes a clocking and power method and runs off a single 5.5V supply. As shown in Figure 1-1, the RF inputs and outputs using miniature version A (SMA) connectors are on the top side of EVM. A reference clock (for example, 10MHz) to lock the onboard voltage-controlled crystal oscillator (VCXO) with the LMK04828, PLL-1 can be provided to the connector named LMK CLKIN (SMA J19).[1]

Figure 1-1 shows the bottom view of the AFE79xxEVM.

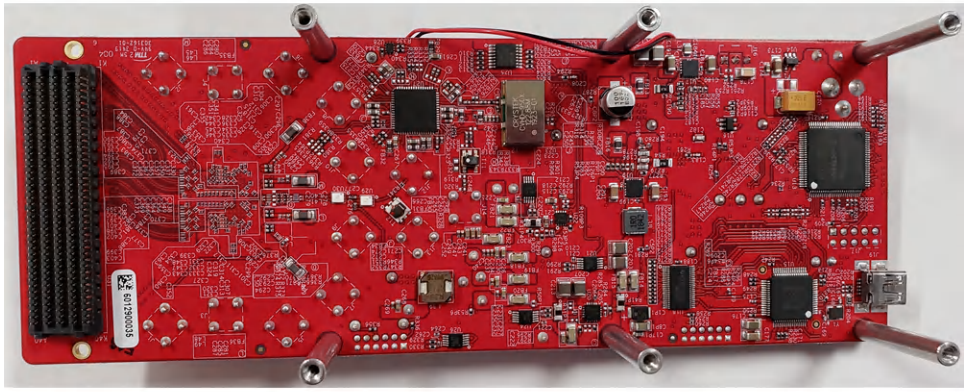

Figure 1-1. AFE79xxEVM Bottom View

Use SMA J12 (REF_CLK_HIGH) or SMA J13 (REF_CLK_LOW) to feed an external reference clock to lock the PLLs in the AFE79xx. The USB connector and the 5.5V connector are on the right side of the board.

Use the TSW14J58 capture card along with the AFE79xx EVM. TSW14J58 supports a SerDes speed of up to 29.5Gbps. Refer to Figure 1-2 for the typical connection between the TSW14J58 EVM and the AFE79xx EVM.

[1] Many typical lab equipments have 10MHz oscillator output to synchronize multiple lab systems. The onboard LMK04828 can accept the 10MHz from external lab equipment to verify synchronization and coherency of the data capture and generation to the AFE79xx EVM.

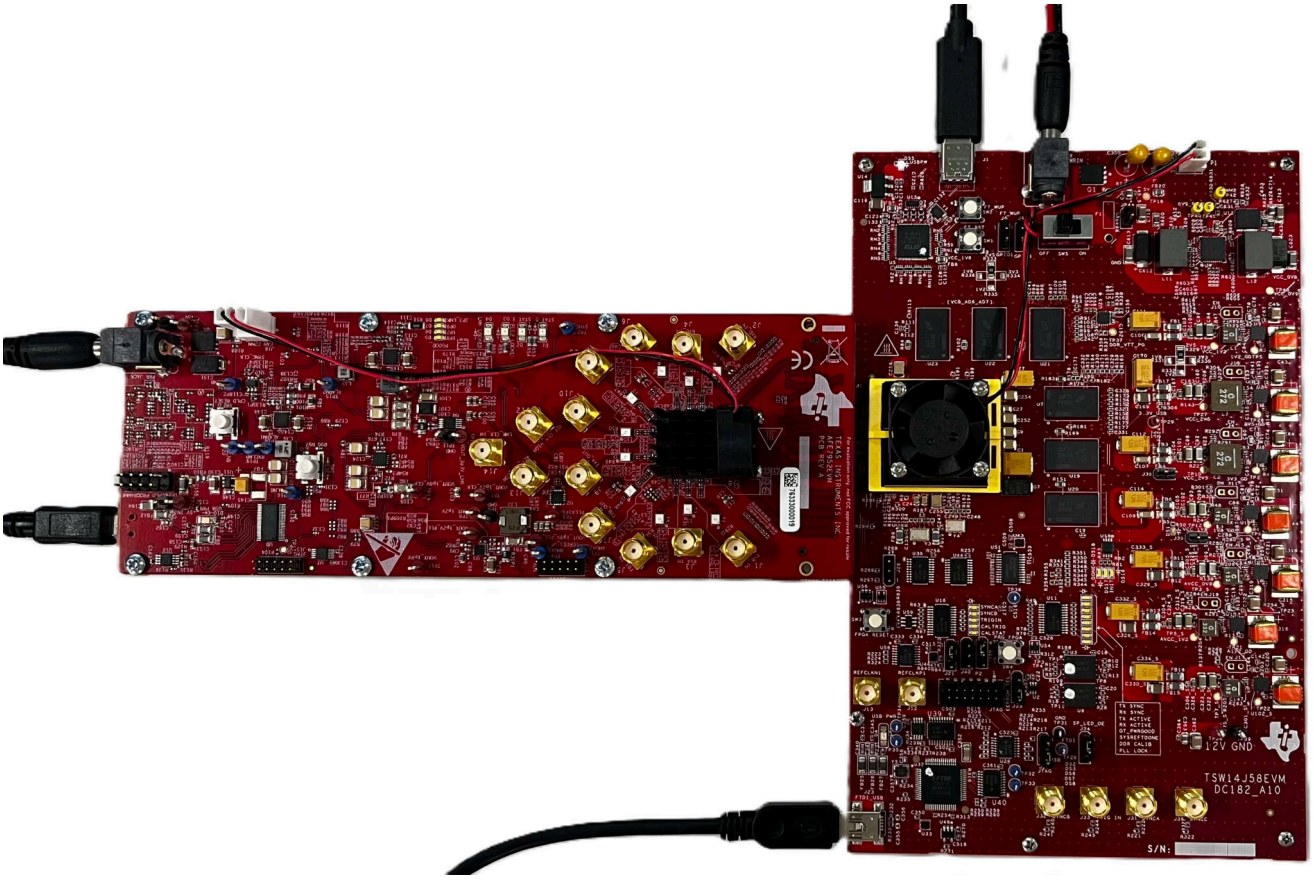

Figure 1-2. AFE79xxEVM and TSW14J58EVM Rev. A10

1.3 Kit Contents

Table 1-1 lists the components of the EVM kit. Contact the Texas Instruments Product Information Center if any components are missing. TI highly recommends that users check ti.com to verify that the latest versions of the related software is in use.

Table 1-1. Kit Contents

Item	Quantity
AFE79xx EVM	1
Mini USB cable	1
Power cable	1

1.4 Specifications

Click here for the device specifications.

1.5 Device Information

The AFE79xx is a family of high performance, wide bandwidth, multi-channel transceivers that integrate four RF sampling transmitter chains, four RF sampling receiver chains, and up to two RF sampling digitizing auxiliary chains (feedback paths). The high dynamic range of the transmitter and receiver chains allows the device to generate and receive 3G, 4G, and 5G signals from wireless base stations, while the wide bandwidth capability of the AFE79xx devices is designed for multi-band 4G and 5G base stations.

Each receiver chain includes a 25dB range DSA (Digital Step Attenuator), followed by a 3GSPS ADC (analog-to-digital converter). Each receiver channel has an analog peak power detector and various digital power detectors to assist an external or internal autonomous automatic gain controller, and RF overload detectors for device reliability protection. The single or dual digital down converters (DDC) provide up to 600MHz of combined signal

BW. In TDD mode, the receiver channel can be configured to dynamically switch between the traffic receiver (TDD RX) and wideband feedback receiver (TDD FB), with the capability of re-using the same analog input for both purposes.

Each transmitter chain includes a single or dual digital up converters (DUCs) supporting up to 1200MHz combined signal bandwidth. The output of the DUCs drives a 12GSPS DAC (digital to analog converter) with a mixed mode output option to enhance 2nd or 3rd Nyquist operation. The DAC output includes a variable gain amplifier (TX DSA) with 40dB range and 1dB analog and 0.125dB digital steps.

The feedback path includes an 25dB range DSA driving a 3GSPS RF sampling ADC, followed by a DDC with up to a 1200MHz bandwidth.

2 Hardware

Two bench power supplies are required to power the AFE79xxEVM and the TSW14J58 EVM. A PC to program the EVM and capture card is required. See Section 2.1 for more information. All lab equipment requirements (such as signal source, signal analyzer, and so forth) are left to the users' discretion.

Note

Typically, the bench power supply with rating of 5.5V powers the AFE79xx EVM. The nominal EVM power supply voltage is 5V. The additional 0.5V overhead is added to compensate for the power cable loss as the AFE79xx EVM and the TSW14J58 to be configured to full operating mode to accommodate the voltage drop associated with power cable loss.

2.1 Recommended Test Environment

- Power supply at 5.5V, 5A maximum for the AFE79xx EVM.
- Power supply at 5.5V, 5A maximum for the TSW14J58 EVM.
- A Windows PC™ that supports USB 3.0 for fast file transfer from ADC capture and DAC pattern loading.
- High-quality RF signal generator that supports RF frequency of interest for evaluation. The example set-up uses a Keysight™ PSG series of signal generator.
- High-quality RF spectrum analyzer that supports RF frequency of interest for evaluation. The example set-up uses Rohde & Schwarz™ FSQ®26 series of spectrum analyzer.

2.2 Required Hardware

- AFE79xx EVM
- TSW14J58 EVM
- 1 × USB 3.0 Micro-B cable (up to TSW14J58 REV A8) / USB Type-C® 3.0 cable (TSW14J58 REV A9+)
- 2 × USB Mini-B cable
- 2 power supply cables

2.3 Hardware Setup

2.3.1 AFE79xx EVM and TSW14J58 EVM Connections

1. Connect the FMC connector U31 of AFE79xx EVM to THE FMC connector J3 of TSW14J58 EVM.
2. With the power supply in powered-down mode, connect a 5.5V, 5A maximum power supply to J2 *+5V IN* connector of the TSW14J58EVM.
3. Connect a USB 3.0 cable from the PC to J1 connector of the TSW14J58 EVM.
4. Connect a USB Mini-B cable from the PC to FTDI_USB connector of the TSW14J58 EVM.
5. With the power supply in powered-down mode, connect the 5.5V, 5A maximum power supply to J18 connector of the AFE79xx EVM.
6. Connect a USB Mini-B cable from the PC to J19 connector of the AFE79xx EVM.
7. Optionally: Connect 10MHz of lab equipment reference to J14, LMK_CLK_IN connector.
8. Optionally: Choose the FPGA bitfile version by changing J35 jumper position.
   a. Default: For bitfile version 204B, check that the physical position of jumper J35 is covering pins 2 and 3 (the two pins positioned furthest from the FPGA fan).
   b. For bitfile version 204C, check that the physical position of jumper J35 is covering pins 1 and 2 (the two pins positioned nearest to the FPGA fan).
   c. The configuration steps in this guide assume the user is using bitfile version 204B.

Refer to Figure 1-2 for the typical connection between the TSW14J58 EVM and the AFE79xx EVM. TI recommends connecting the USBs directly to the PC, rather than a USB hub, and disconnect unnecessary USB devices from the PC. Other USB devices can potentially interfere with the ability of the PC to recognize the EVM USB handles.

After completing these steps, turn on the power supplies.

2.3.2 Power Supply Setup

1. Check that the D9 (PWR) LED is lit up. The power supply draws approximately 550mA to 650mA.

2. Check that the D10 (USB_PWR) LED is lit up. The LED light strength depends on the USB cable length. If the LED is not lit up, use a shorter USB cable. TI tested three-foot USB cables in this setup.
3. The power supply sequencer on the AFE79xx EVM has power status for each rail. If the power good (PGOOD) is in logic HI, the corresponding power supply rail is powered correctly. The respective LEDs light up. Check the following LEDs to verify that there is light.
   - D5 (1P8) LED
   - D6 (1P2) LED
   - D7 (0p9) LED
   - D8 (3p3_LMK) LED

3 Software

3.1 Required Software

The software used to configure the AFE79xxEVM is called *Latte*. The latest version of Latte is available for download from TI's Secure Resources website. The installer file is called *TI-AFE79xx-Latte_V2p5.exe.*

3.1.1 Software Installation Sequence

1. Install *TI-AFE79xx-Latte_V2p5.exe*, or latest version. Once the software is installed, launch the software from the AFE79xx Startup window from the Start Menu, or by selecting the AFE79xx icon in Desktop. Initializing the software takes up to 2 minutes.
2. Note the directory to which the Latte software is installed.

Note

The Default Latte Software Directory is in:

C:\Users\"User ID"\Documents\Texas Instruments\Latte

Replace the *"User ID"* with the proper Windows login ID.

3.2 Latte Overview

1. After fully initializing the software, launch the Latte GUI from the desktop shortcut or by selecting *All Programs* then selecting *Texas Instruments*.

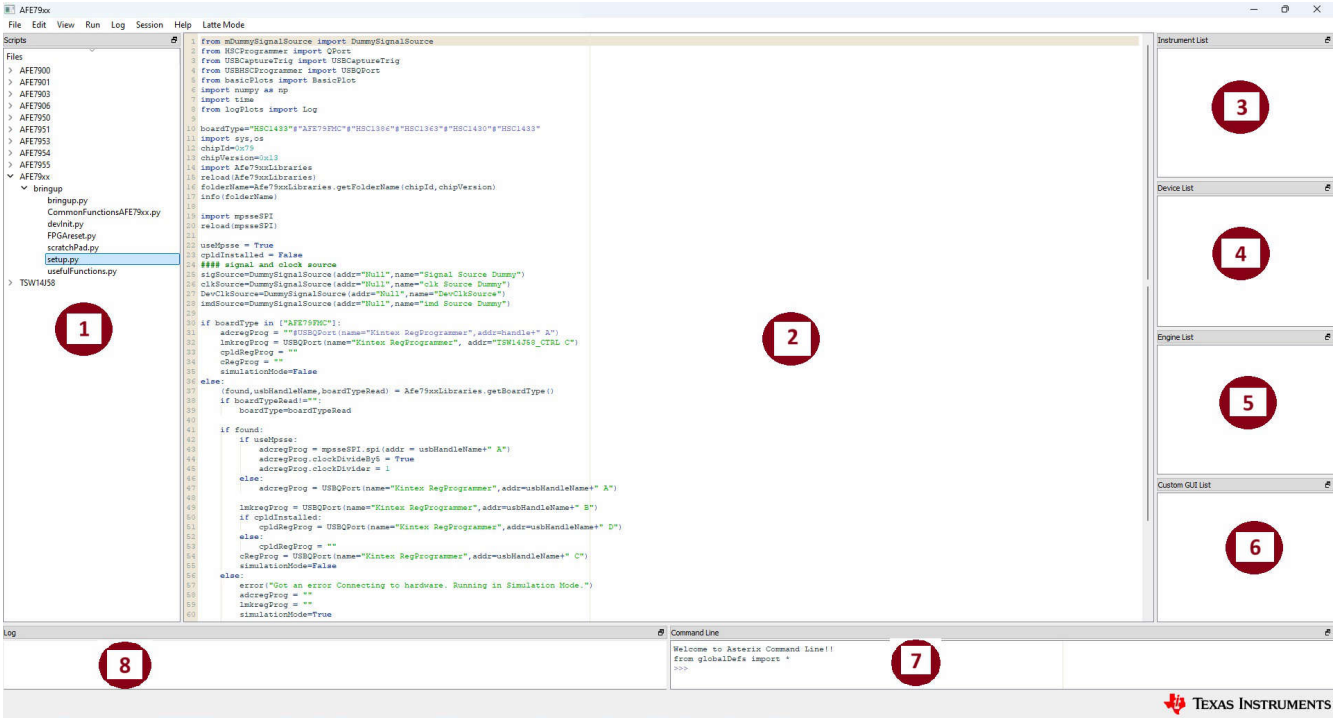

Figure 3-1. Latte GUI Overview

3.2.1 Latte User Interface

The Latte UI is split into eight windows (labeled 1 to 8) with the following functions:

- **Window 1:**

  This window (also called *Scripts*) shows the list of python scripts available that generate the register commands to configure the AFE79xxEVM. The script files shown are located in the *..\Documents\TexasInstruments\AFE79xxLatte\projects\AFE79xx\bringup* folder. Modify and create new scripts as necessary. Modified and new scripts appear in the Window 1 sub-window when Latte restarts.

- **Window 2:**

  This window (also called *Editor*) shows the code in the script currently selected. Use Window 2 to modify and save the code as necessary.
- **Window 3 to 6:**

  These windows update as the scripts run to configure the AFE79xxEVM and mostly are informational.
- **Window 7:**

  This window (also called *Command Line*) is used to enter and run individual commands. Examples of such commands include changing the TX, RX, FBRX DSA, NCOs, and so forth.
- **Window 8:**

  This window (also called *Log*) displays messages during execution of scripts to display the current status. This window is also used for troubleshooting.

3.2.2 Useful Latte Short-Cuts

Run Script file: Run a script file by first selecting the file in the Scripts window and then by pressing F5 (or selecting *Run* and then *Buffer* in the menu bar).

Run part of script: Run part of a script file by selecting the lines in the Editor window and then by pressing F7 (or selecting *Run* and then *Run Selection* in the menu bar).

Stop Execution: Stop the current execution by pressing F10 (or selecting *Run* and then *Stop* in the menu bar).

Clear Session: Clear the current session to reset the Latte UI to the initial state by pressing Ctrl-T (or selecting *Session* and then *Clear Session* in the menu bar). This process is equivalent to a restart, use this process to restart a session without closing the GUI.

4 Implementation Results

4.1 AFE79xxEVM Configuration

This section guides you through the sequence of steps to bring-up the AFE79xxEVM. The automatic setup process is broken down in this section for users to understand the process and make modifications accordingly.

4.1.1 Connect Latte to Board

This step establishes a connection between the PC running Latte and the AFE79xxEVM.

1. In the scripts window, select the *AFE79xx* drop-down, then the *bringup* drop-down. Select *setup.py*. On line 13, verify that the chip version is 0x13. Press F5 to run the program.
2. Check the Log window to verify that there are no errors. Check that the following line is displayed twice: *Kintex RegProgrammer - USB Instrument created*.
3. Missing or obsolete drivers for the FT4232H chip in the AFE79xxEVM is a common error source. In Latte, use the *View* tab then *USB Handles* to check USB handle connections to Latte. There are four connections for the TSW14J58 and four connections to the EVM. Alternatively, use the device manager to verify a connection between the PC and the EVM by checking the USB instantiations.
4. Update your PC with the appropriate driver, if necessary.

Figure 4-1. Latte Log After Successful setup.py

4.1.2 Compile Libraries

In this step, the library of scripts packaged with the Latte UI is compiled and takes approximately 30 seconds to run.

1. In the scripts window, select *devInit.py*.
2. Select F5 to run the program.
3. Check the Log window for status and errors.

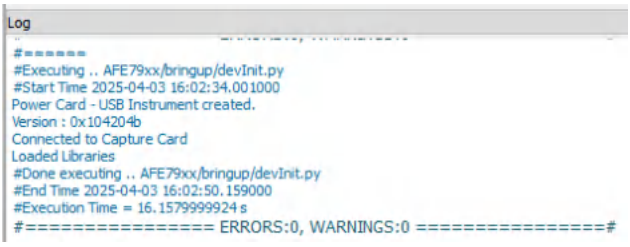

Figure 4-2. Latte Log After Successful devInit.py

4.1.3 Program AFE79xx EVM

Follow the below instructions to program the LMK04828 and AFE79xx on the AFE79xxEVM.

1. Select the script named *bringup.py* and press F5. No errors are expected, ignore any warnings regarding SPI control, relinquish, or reset property. This step takes a few minutes.
2. Check the Log window to monitor any errors. This step completes the AFE79xxEVM configuration. Current consumption into the AFE79xxEVM is approximately 3A.

3. A mismatch FPGA bitfile version error indicates that the firmware does not match the configuration file. For bitfile version 204b, check that the physical position of jumper J35 is covering pins 2 and 3 (the two pins positioned furthest from the FPGA fan).
4. An LOS error indicates that the SerDes RX is electrically idle and the TX output is not normal. Resolve this error by resending the data (the DAC pattern) and reconfiguring the AFE79xxEVM by rerunning *bringup.py*.
5. GPIO warnings or sysref errors typically indicate supply voltage or current limitations. Verify the power supply to the AFE79xxEVM and verify that a 5.5V supply voltage and a 5A current limit is used. Restart the Latte UI and rerun the scripts.

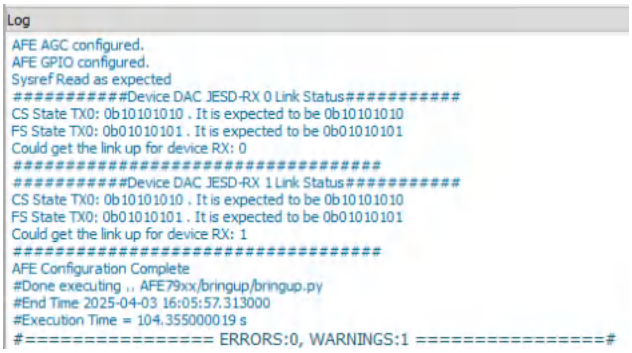

Figure 4-3. Latte Log After Successful bringup.py

4.1.4 TXDAC Evaluation

1. Connect the signal analyzer to J9 (TXA), J7 (TXB), J10 (TXC), or J8 (TXD) to monitor the TXDAC output.
2. Highlight a portion of applicable code, and press F7 to run. See Figure 4-4 for typical performance measurement.

```
### TX Tone Out

## Send 10MHz Tone to TX AB
amplA = -10 #band 0amp in dBfs
freqA = 10 #band 0 freq in MHz
amplB = -10 #band 1amp
freqB = 10 #band 1 freq
AFE.selectCH(2,0)
AFE.FPGA.sendSingleTone(0,freqA,amplA,freqB,amplB)

## Send 10MHz Tone to TX CD
amplA = -10 #band 0amp
freqA = 10 #band 0 freq
amplB = -10 #band 1amp
freqB = 10 #band 1 freq
AFE.selectCH(2,2)
AFE.FPGA.sendSingleTone(0,freqA,amplA,freqB,amplB)
```

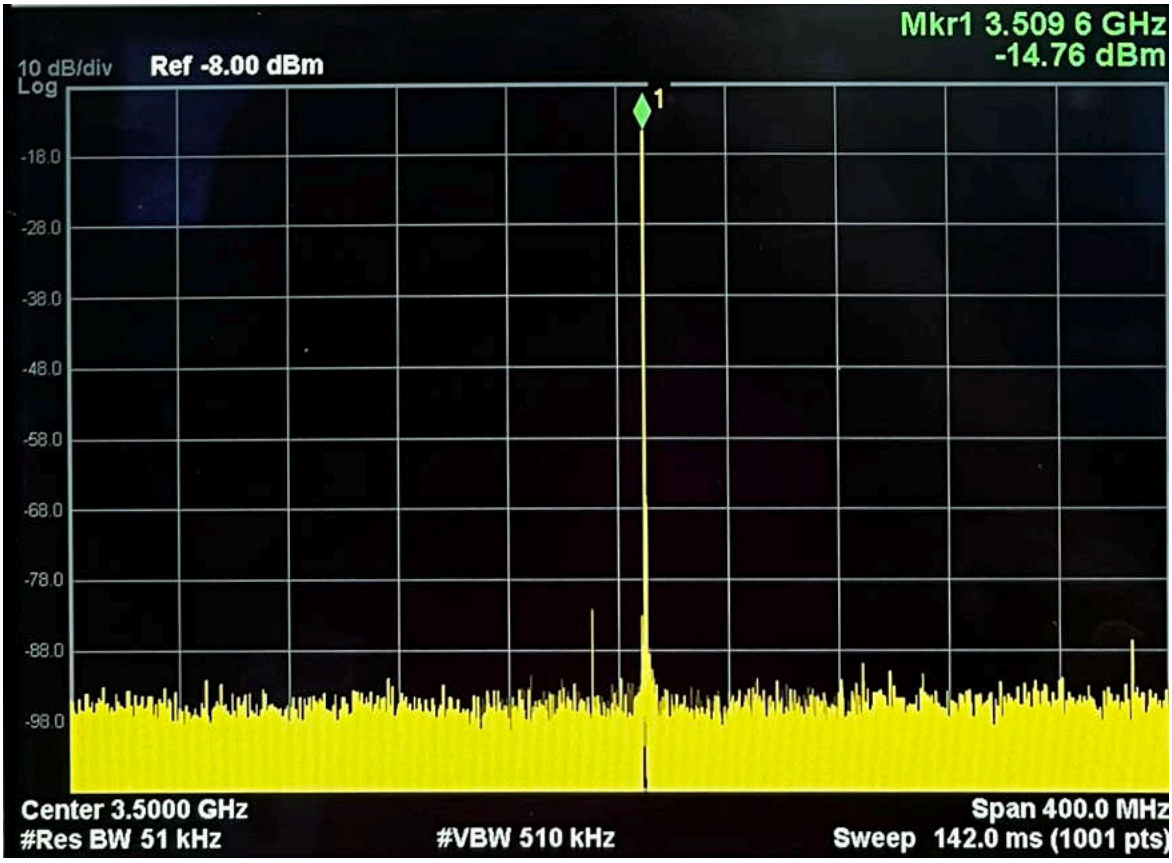

Figure 4-4. Typical TXDAC 10MHz Single Tone Performance at 3.5GHz NCO with -10dBFS Amplitude

4.1.5 RXADC and FBADC Evaluation

1. Connect the signal generator to J3 (RXA), J1 (RXB), J4 (RXC), or J2 (RXD) to supply the RXADC input at the defined NCO + 10MHz. Connect the signal generator to J5 (FBAB) or J6 (FBCD) to supply the FBADC input at the defined NCO + 10MHz.
2. Highlight portion of applicable code below and select F7 to run. In Latte Window 6 in Section 3.2.1, select *CGui_CGui_Custom_Gui* to view the capture.
3. In the capture window, select the *Finite Samples* capture type. View the capture in the *Complex* tab.

```
### RX/FB Tone In
AFE.selectCh(0,0,0) # select RX A, band 0
AFE.selectCh(0,0,1) # select RX A, band 1
AFE.selectCh(0,1,0) # select RX B, band 0
AFE.selectCh(0,1,1) # select RX B, band 1
AFE.selectCh(0,2,0) # select RX C, band 0
AFE.selectCh(0,2,1) # select RX C, band 1
AFE.selectCh(0,3,0) # select RX D, band 0
AFE.selectCh(0,3,1) # select RX D, band 1

AFE.selectCh(1,0) #select FBAB
AFE.selectCh(1,1) #select FBCD
```

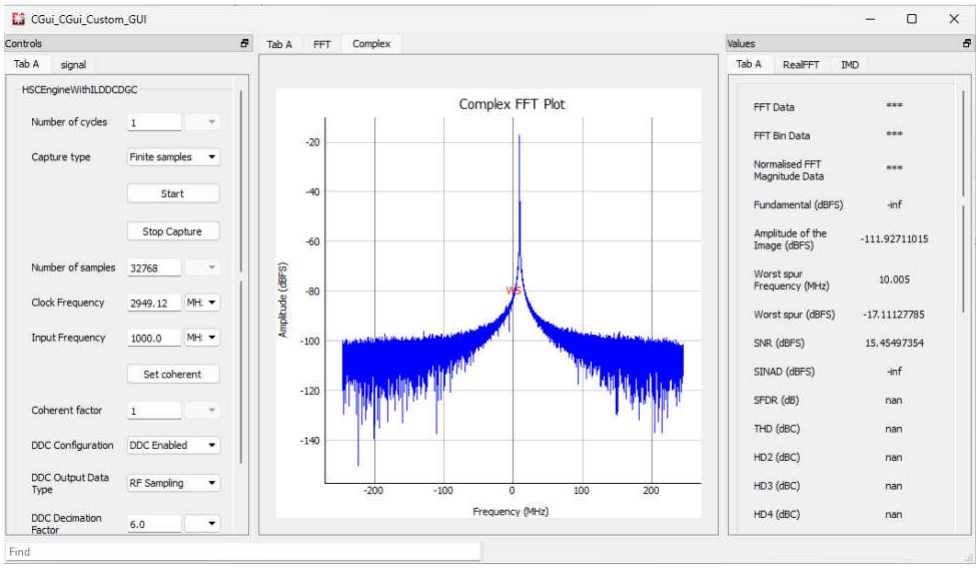

Figure 4-5. Typical RXADC 10MHz Single Tone Performance at 3.5GHz NCO

4.2 AFE79xxEVM Configuration Modifications

The provided scripts configure the AFE79xx with the default settings declared in Latte scripts. You can change the settings by modifying a set of parameters.

This section includes steps to modify the bringup the AFE79xxEVM through the python scripts. The example is the default AFE79xxEVM. Table 4-1 shows the default mode configuration overview.

Table 4-1. AFE79xx EVM Default Configuration Overview

Mode	Default Programming
TX (transmitter)	4 TXDACs are enabled, DSA = 0, LMFSHd_2TX = 44210, 24× interpolation, 491.52MSPS data rate
RX (receiver)	4 RXADCs are enabled, DSA = 0, LMFSHd_2RX = 12410, 12× decimation, 245.76MSPS data rate
FBRX (feedback receiver)	2 FBADCs are enabled, DSA = 0, LMFSHd_1FB = 24410, 6× decimation, 491.52MSPS data rate
SerDes	8 lanes running at 9830.4Mbps
Data Converter Clock Rates	F_{RXADC} = 2949.12MSPS, F_{FBADC} = 2949.12MSPS, F_{TXDAC} = 11796.48MSPS.
Status	RX AGC is disabled, RX, TX DSA step impairments is uncorrected, DAC in interleaved mode.

4.2.1 Data Converter Clocks Settings

This parameter is used to configure the data converter clocks and clock distribution path.

```
#Configures the reference input frequency to the on-chip PLL of the AFE79xx.
sysParams.FRef     = 491.52
#Configures the RXADC converter sample rate.
sysParams.FadcRx   = 2949.12
#Configures the FBADC converter sample rate.
sysParams.FadcFb         = 2949.12
#Configures the TXDAC converter sample rate.
sysParams.Fdac     = 2949.12*4
#Sets the clock source for the RXADC converters. The source is now from the on-chip PLL.
sysParams.externalClockRx = False
#Sets the clock source for the TXDAC converters. The source is now from the on-chip PLL.
sysParams.externalClockTx = False
```

4.2.2 Data Rate and JESD Parameters

Data rates in the signal chain often connect with the JESD mode (LMFS, SerDes rate). The device data sheet provides a list of compatible modes. Use the following parameters in the *bringup.py* script \to modify the configuration. Rerun the script after assigning new values to the following parameters.

```
## In below parameters, each element sets the particular LMFS-Hd for the particular channels.
# JESD and Serdes Parameters
sysParams.LMFSHdRx                = ["12410","12410","12410","12410"]
sysParams.LMFSHdFb                = ["24410","24410"]
sysParams.LMFSHdTx                = ["44210","44210","44210","44210"]
# Decimation and interpolation parameters for the data converter signal chains.
sysParams.ddcFactorRx                 = [12,12,12,12]
sysParams.ddcFactorFb                 = [6,6]
sysParams.ducFactorTx                 = [24,24,24,24]
```

4.2.3 Steps to Modify NCO

1. The default AFE79xx EVM has the following RF frequency matching network:
   a. RXA, RXB, FBAB, TXA, and TXB = 3500MHz
   b. RXC, RXD, FBCD, TXC, and TXD = 2600MHz
2. The example script to change the NCO to match the default RF frequency matching network is the following:

```
## Update RX NCO
afeInst = 0 #AFE Instance of AFE79_INST_TYPE type. If using the EVM this should be 0.
rxChSel = 0 #Value to select the RX chain.Value 0 for RXA to 3 for RXD.
bandNo = 0 #Band number. 0-band0, 1-band1.
ncoNo = 0 #NCO number. 0-NCO0, 1-NCO1.
ncoFreq = 7200#NCO frequency to set the NCO to in MHz.

if sysParams.ncoFreqMode == '1KHz':
     mixer = ncoFreq*1e3 #Should pass value in KHz in 1KHz      ncoFreqMode and the frequency word
value in FCW mode.

elif sysParams.ncoFreqMode == 'FCW':
     mixer = int(round(2**32*ncoFreq/sysParams.FadcRx)) #Should pass value in KHz in 1KHz
ncoFreqMode and the frequency word value in FCW mode.

CAFE.updateRxNco(afeInst,rxChSel,mixer,bandNo,ncoNo)
engine.DDCNCOFreqWord=((ncoFreq)%sysParams.FadcRx)/(sysParams.FadcRx)*2**32 #Updating NCO word in
capture window

## Update TX NCO
afeInst = 0 #AFE Instance of AFE79_INST_TYPE type. If using the EVM   this should be 0.
txChSel = 0 #Value to select the TX chain.Value 0 for TXA to 3 for TXD.
ncoNo = 0 #NCO number. 0-NCO0, 1-NCO1.
band0NCO0 = 2600000 #NCO frequency to set the band 0 NCO0 to in KHz.
band1NCO0 = 2600000 #NCO frequency to set the band 1 NCO0 to in KHz.
band0NCO1 = 3500000 #NCO frequency to set the band 0 NCO1 to in KHz.
band1NCO1 = 3500000 #NCO frequency to set the band 1 NCO1 to in KHz.
CAFE.updateTxNcoDb(afeInst,txChSel,ncoNo,band0NCO0,band1NCO0,band0NCO1,band1NCO1)
```

4.2.4 Steps to Modify DSA

Enable data transmission on the DAC and data capture on the ADC. Adjust the RXNCO, FBNCO, and TXNCO at this point.

Adjust the RXDSA, FBDSA, and TXDSA at this point.

```
## Set RX DSA
afeInst = 0 #AFE Instance of AFE79_INST_TYPE type. If using the EVM this should be 0.
rxChSel = 0 #Value to select the RX chain.Value 0 for RXA to 3 for RXD.
dsaSetting = 20 #Analog DSA Index. Attenuation applied is   dsaSetting*0.5dB
CAFE.setRxDsa(afeInst,rxChSel,dsaSetting)

## Set TX DSA
afeInst = 0 #AFE Instance of AFE79_INST_TYPE type. If using the EVM this should be 0.
txChSel = 0 #Value to select the TX chain.Value 0 for TXA to 3 for TXD.
dsaSetting = 20 #Analog DSA Index. Attenuation applied is dsaSetting*1dB
CAFE.setTxDsa(afeInst,txChSel,dsaSetting)
```

5 Hardware Design Files

5.1 Schematics

Click here for the device schematics.

5.2 PCB Layouts

Click here for the PCB layouts.

5.3 Bill of Materials (BOM)

Click here for the bill of materials.

6 Additional Information

6.1 Status Check and Troubleshooting Guidelines

This section provides a general guideline on the status indicators of the AFE79xx EVM and also the respective troubleshooting guidelines.

6.1.1 AFE79xx EVM Status Indicators

At this point, the green LED D3 is illuminated. D3 indicates that PLL loop 2 of the LMK04828 is locked. Optionally, the LED D4 indicates that PLL loop 1 of the LMK04828 is locked. If there are external equipment providing a 10MHz reference to the LMK04828 for lab equipment synchronization, then this LED D4 must illuminate. The EVM is still functional without PLL loop 1 running, but PLL loop 2 is necessary for a successful bring-up.

- If PLL loop 1 is not running, check the 10MHz reference. The 10MHz reference is necessary to achieve signal coherency with the signal generators and spectrum analyzer.
- If PLL loop 2 is not locked, contact TI applications for additional support.

6.1.2 TSW14J58EVM Status Indicators

On the LED strip, TX_Sync and RX_Sync are not illuminated. TX_Active and RX_Active is illuminated. Illumination specifications are necessary requirements for the JESD204B transceiver mode to work. TX_Active flashing indicating the TXDAC JESD204B link is established, while RX_Active flashing indicating the RXADC or FBADC JESD204B link is established.

Trademarks

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2023) to Revision B (September 2025) **Page**

- Updated document to reflect current EVM user's guide format....1
- Added *TSW14J58EVM* and *TSW14J58 capture card* information throughout....1
- Added *Features* section....1
- Added *Kit Contents* section....3
- Added *Specifications* section....3
- Added *Device Information* section....3
- Updated *Hardware Setup* section....5
- Updated *AFE79xx EVM and TSW14J58 EVM Connections* section....5
- Updated *Required Software* section....7
- Moved *Required Software* from *Hardware* to *Software* 7
- Updated *Software Installation Sequence* section....7
- Deleted *Software Installation Checks* section....7
- Updated *Latte Overview* section....7
- Moved *Latte Overview* to *Software* section....7
- Deleted *AFE79xx EVM Automatic Configuration* section....9
- Added *Implementation Results* section....9
- Updated from: AFE79xxEVM Manual Configuration to: AFE79xxEVM Configuration....9
- Moved *AFE79xxEVM Configuration* to *Implementation Results* 9
- Added *Latte Log After Successful setup.py* figure....9
- Added *Latte Log After Successful devInit.py* figure....9
- Added *Latte Log After Successful bringup.py* figure....9
- Deleted *Typical TXDAC Single Tone Performance at 3.5 GHz* figure....10
- Added *### TX Tone Out* code block....10
- Added *Typical TXDAC 10MHz Single Tone Performance at 3.5GHz NCO with -10dBFS Amplitude* figure....10
- Updated *RXADC and FBADC Evaluation* section....11
- Deleted *HSDC PRO ADC Performance FFT Binning Configuration* figure....11
- Deleted *HSDC PRO ADC Data Capture and Typical Single Tone 3.5-GHz Performance for RXADC* figure....11
- Deleted *Typical Single Tone 3.5-GHz Performance for FBADC* figure....11
- Added *### RX/FB Tone In* code block....11
- Added *Typical RXADC 10MHz Single Tone Performance at 3.5GHz NCO* code block....11
- Updated from: *AFE79xx EVM Automatic Configuration* to: *AFE79xxEVM Configuration Modifications* 12
- Updated *AFE79xx EVM Automatic Configuration* section....12
- Added *Steps to Modify NCO* section....13
- Deleted *AFE79xxEVM Manual Configuration* section....13
- Deleted *Setup the TSW14J5x With the HSDC Pro* section....13
- Deleted *##RXDSA Adjustment* code block....13
- Added *## Set RX DSA* code block....13
- Added *Hardware Design Files* section....14
- Added *Additional Information* section....15
- Moved *Status Check and Troubleshooting Guidelines* to *Additional Information* section....15

Changes from Revision * (October 2019) to Revision A (April 2023) **Page**

- Added *Caution and Warnings* section....2

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