User's Guide

ADS9224REVM-PDK

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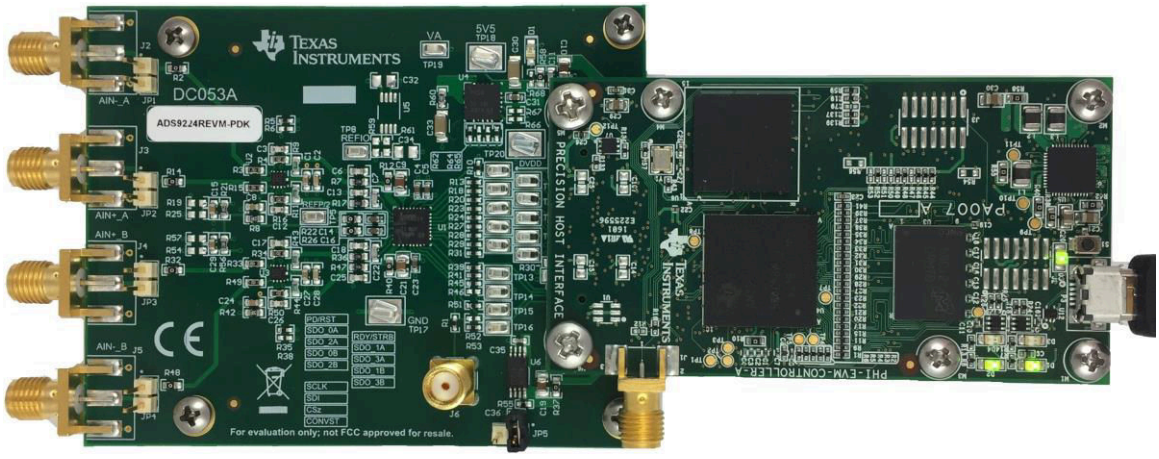
ABSTRACT

This user's guide describes the characteristics, operation, and use of the ADS9224R evaluation module (EVM) performance demonstration kit (PDK). The EVM-PDK eases the evaluation of the ADS9224R device with hardware, software, and computer connectivity through a universal serial bus (USB) interface. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the ADS9224REVM-PDK. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials.

The following related documents are available through the Texas Instruments web site at www.ti.com.

Related Documentation

Device	Literature Number
ADS9224R	SBAS876
THS4551	SBOS778
REF5025	SBOS410
TPS7A4700	SBVS204



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1 Overview

The ADS9224REVM-PDK is an evaluation platform for the ADS9224R, a dual, simultaneous-sampling, 16-bit, 3-MSPS, fully-differential input successive approximation register (SAR) analog-to-digital converter (ADC). The ADS9224R features an enhanced serial multiSPI® digital interface. The evaluation kit includes the ADS9224REVM board and the *Precision Host Interface* (PHI) controller board that enables the accompanying computer software to communicate with the ADC using a USB interface for data capture and analysis.

The ADS9224REVM board includes the ADS9224R SAR ADC, all the peripheral analog circuits, and components required to extract optimum performance from the ADC.

The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS9224R
- Supplies power to all active circuitry on the ADS9224REVM-PDK board

Along with the ADS9224REVM and PHI controller board, this evaluation kit includes an A-to-micro-B USB cable to connect to a computer.

1.1 ADS9224REVM-PDK Features

The ADS9224REVM-PDK includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS9224R ADC
- USB powered—no external power supply is required
- A PHI controller that provides a convenient communication interface to the ADS9224R ADC over USB 2.0 (or higher) for power delivery as well as digital input and output
- Easy-to-use evaluation software for Windows® 7, 8, and 10, 64-bit operating systems
- The software suite includes graphical tools for data capture, histogram analysis, spectral analysis, linearity analysis, and reference settling analysis. This suite also has a provision for exporting data to a text file for post-processing.

1.2 ADS9224REVM Features

The ADS9224REVM includes the following features:

- Onboard low-noise and low distortion ADC fully-differential amplifier input drivers optimized to meet ADC performance
- Onboard ultra-low-noise, low-dropout (LDO) regulator for excellent, 5-V single-supply regulation of the voltage reference and all the fully-differential amplifier input drivers

2 Analog Interface

The ADS9224R is a dual-channel, simultaneous-sampling ADC that supports fully-differential inputs. Each channel of the ADS9224R uses a THS4551 fully-differential amplifier (FDA) to drive the differential inputs of the ADC. This section covers driver details and board connections for a differential signal source.

2.1 Connectors for Signal Source

The ADS9224REVM is designed for easy interfacing to multiple analog sources. SMA connectors allow the EVM to have input signals connected through coaxial cables. In addition, header connectors JP1 through JP4 provide a convenient way to connect input signals. All analog inputs are buffered by the THS4551 high-speed FDA in order to properly drive the ADS9224R ADC inputs.

Table 2-1. J2 to J5 SMA Analog Interface Connections

Pin Number	Signal	Description
J2	AIN-_A	CHA negative differential input. This SMA connector can be grounded by installing a shunt on JP1 for single-ended signals. 1-kΩ input impedance
J3	AIN+_A	CHA positive differential input or input for single-ended signals. 1-kΩ input impedance
J4	AIN+_B	CHB positive differential input or input for single-ended signals. 1-kΩ input impedance
J5	AIN-_B	CHB negative differential input. This SMA connector can be grounded by installing a shunt on JP4 for single-ended signals. 1-kΩ input impedance

Table 2-2. JP1 to JP4 Header Descriptions

Pin Number	Signal	Description
JP1.1	AIN-_A	CHA negative differential input. This SMA connector can be grounded by installing a shunt on JP1 for single-ended signals. 1-kΩ input impedance.
JP2.1	AIN+_A	CHA positive differential input or input for single-ended signals. 1-kΩ input impedance.
JP3.1	AIN+_B	CHB positive differential input or input for single-ended signals. 1-kΩ input impedance.
JP4.1	AIN-_B	CHB negative differential input. This SMA connector can be grounded by installing a shunt on JP4 for single-ended signals. 1-kΩ input impedance.

2.2 ADC Differential Input Signal Driver

The analog inputs of the ADS9224R SAR ADC are not high-impedance but rather present a dynamic load as the sample-and-hold switches open and close. The current demand of the SAR ADC input increases as a function of the sampling rate. Thus, the evaluation board provides the THS4551 FDA driver that maintains ADC performance with maximum loading at the full device throughput of 3 MSPS.

2.2.1 Input Signal Path

Figure 2-1 shows the signal path for the differential signal applied at the board inputs. The board input impedance is 1 kΩ. The overall signal-path bandwidth is limited to 1.5-MHz by the 1-kΩ resistor and 100-pF capacitor at the FDA feedback. The two THS4551 FDAs drive the ADS9224R differential inputs through an RC charge-kickback filter. These drivers provide a low dynamic impedance source at the ADC inputs at the full throughput of 3 MSPS.

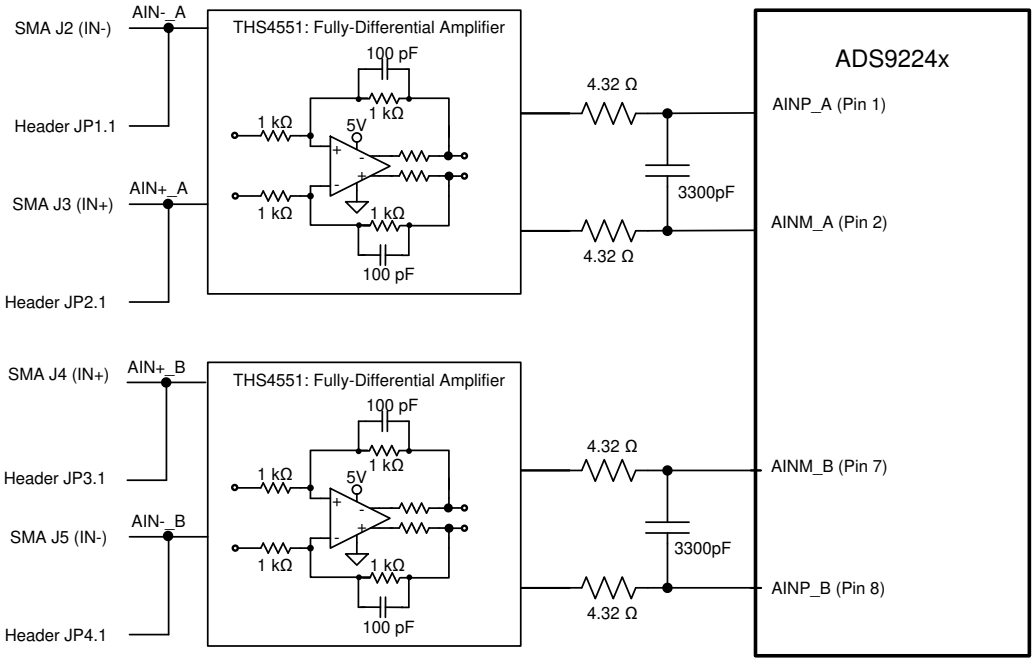


Figure 2-1. THS4551 Differential Input Driving Path

The ADS92x4REVM incorporates two THS4551 FDAs to drive the ADC inputs. The FDAs shift the signal to the appropriate common-mode voltage level. Figure 2-2 shows the fully-differential amplifier circuit. A differential input signal with a common-mode voltage of 0 V is applied to the inputs of the THS4551. The FDA establishes a fixed common-mode voltage at the ADC inputs using the FDA V_{OCM} input pin. The ADS9224R incorporates a REF / 2 buffer output pin for setting the common-mode voltage. The ADS9224R REF / 2 output is connected to each THS4551 V_{OCM} input pin. The THS4551 shifts the signal to the required common-mode voltage of REF / 2. Because of the THS4551 output swing specification to GND, either the input signals must be limited to a differential voltage of ±3.876 V amplitude in order to avoid saturating the amplifier output, or the negative supply must be driven below GND (in other words, –200 mV) to extend the output range.

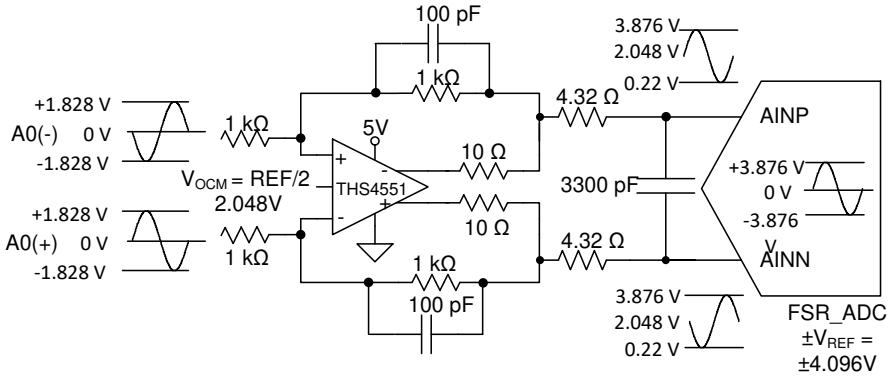


Figure 2-2. THS4551 Fully-Differential Amplifier Driver

2.3 ADS9224R Internal Reference

The ADS9224R device incorporates an internal 2.5-V band-gap reference and independently matched reference buffers for each ADC. The internal reference output pin (REFOUT) is decoupled with a 1-µF capacitor and can be probed at test point TP8. The internally matched reference buffers provide a gain of 1.6384 V/V. These reference buffers generate a high-precision, 4.096-V reference voltage for each ADC channel at pins REFP_A and REFP_B. These pins are decoupled with 10-µF decoupling capacitors. Additionally, a mid-reference output (REFby2) is available at test point TP5. This internal REFby2 buffer provides a common-mode voltage for input amplifiers driving the ADC inputs.

3 Digital Interfaces

As noted in Section 1, the EVM interfaces with the PHI that, in turn, communicates with the computer using the USB interface. There are two devices on the EVM that communicate with the PHI: the ADS9224R ADC (over SPI or multiSPI) and the EEPROM (over I^2C). The EEPROM comes preprogrammed with the information required to configure and initialize the ADS9224REVM-PDK platform. After the hardware is initialized, the EEPROM is no longer used.

3.1 multiSPI™ for ADC Digital IO

The ADS9224REVM-PDK supports several interface modes, as detailed in the ADS9224R data sheet. In addition to the standard SPI modes (single-, dual-, and quad-SDO lines), the multiSPI modes support single- and dual-data output rates. The PHI is capable of operating at a 3.3-V logic level and is directly connected to the digital I/O lines of the ADC. Table 3-1 lists the test points available for probing the SPI pins in both SPI and parallel byte mode.

Table 3-1. SPI Test Points

Designator	Signal	Description
TP1	$\overline{RST}$	Asynchronous reset; active low.
TP2	READY/STR	Indicates data-ready or strobe output for data capture.
TP3	SDO-0/0A	SPI mode: data output 0 for channel A.
		Parallel byte mode: least significant bit (LSB) from the data byte.
TP4	SDO-1/1A	SPI mode: data output 1 for channel A.
		Parallel byte mode: LSB+1 from the data byte.
TP6	SDO-2/2A	SPI mode: data output 2 for channel A.
		Parallel byte mode: LSB+2 from the data byte.
TP7	SDO-3/3A	SPI mode: data output 3 for channel A.
		Parallel byte mode: LSB+3 from the data byte.
TP9	SDO-4/0B	SPI mode: data output 4 for channel A.
		Parallel byte mode: LSB+4 from the data byte.
TP10	SDO-5/1B	SPI mode: data output 5 for channel A.
		Parallel byte mode: LSB+5 from the data byte.
TP11	SDO-6/2B	SPI mode: data output 6 for channel A.
		Parallel byte mode: LSB+6 from the data byte.
TP12	SDO-7/3B	SPI mode: data output 7 for channel A.
		Parallel byte mode: MSB from the data byte.
TP13	SCLK	Clock input pin for the serial interface.
TP14	SDI	Serial data input pin.
TP15	$\overline{CS}$	Chip-select input pin; active low.
TP16	CONVST	Conversion start input pin.

4 Power Supplies

The PHI controller provides multiple power-supply options for the EVM, derived from the USB supply of the computer.

The EEPROM on the ADS9224REVM use a 3.3-V power supply generated directly by the PHI. The ADC and analog input drive circuits are powered by the TPS7A4700 onboard the EVM. The TPS7A4700 is a low-noise linear regulator that uses the 5.5-V supply out of a switching regulator on the PHI to generate a much cleaner 5.0-V output. The 3.3-V supply to the digital section of the ADC is provided directly by an LDO regulator on the PHI.

The power supply for each active component on the EVM is bypassed with a ceramic capacitor placed close to that component. Additionally, the EVM layout uses thick traces or large copper fill areas, where possible, between bypass capacitors and their loads in order to minimize inductance along the load current path.

The LM7705 outputs a –230-mV option to drive the negative supply (VS–) of the fully-differential input amplifiers. This option allows the amplifier outputs to swing all the way to ground and achieve a full-scale differential signal at the ADC input. Configure JP8 in the [1-2] position to use the –230-mV supply for VS–. If the entire full-scale range is not required, VS– can be connected to GND by configuring JP8 in the [2-3] position. U8 can be disabled by uninstalling the jumper on JP7. Table 4-1 lists the relevant power supply test points on the EVM.

Table 4-1. Power-Supply Test Points

Designator	Signal	Description
TP17	GND	EVM ground
TP18	LDO_IN_5V5	5.5-V supply from PHI EVM controller
TP19	VA	5-V analog supply
TP20	DVDD	3.3-V digital supply
TP21	VS–	Negative supply for fully-differential input amplifiers

5 Setup

This section explains the initial hardware and software setup procedures that must be completed for the proper operation of the ADS9224xEVM-PDK.

5.1 Default Jumper Settings

JP1-JP2 and JP3-JP4 are used to connect differential analog sources to channel A and channel B inputs, respectively. In addition, shunts can be used on jumpers JP1 and JP4 to ground the negative inputs and support single-ended signals, as described in Section 2.1.

. Figure 5-1 shows the default factory jumper locations and settings.

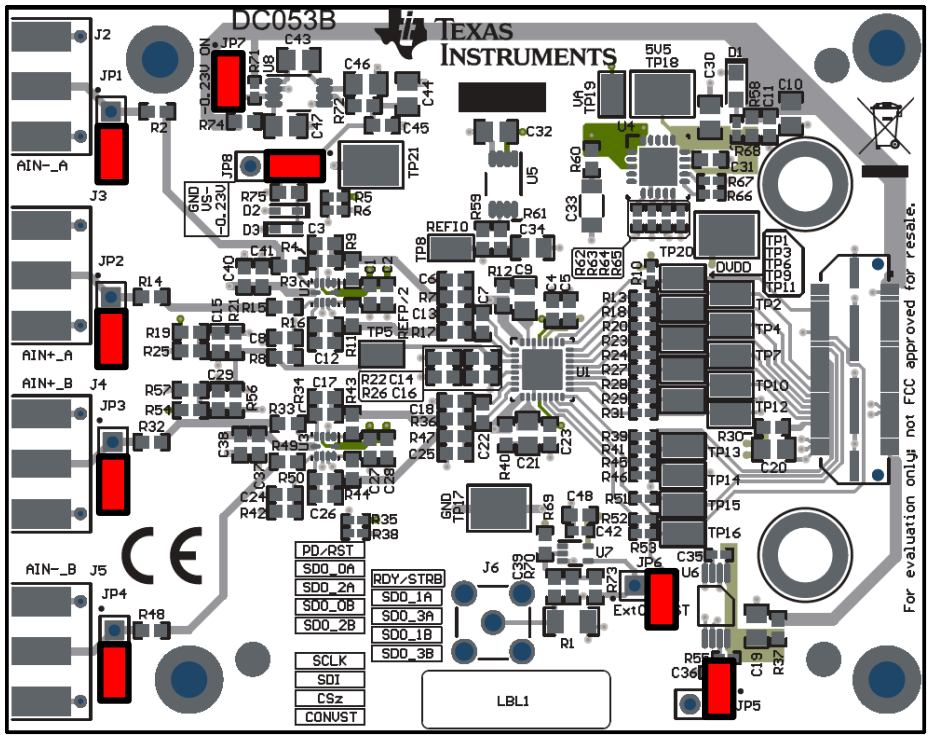


Figure 5-1. ADS9224REVM-PDK Jumper Locations

Table 5-1 explains the functionality of each of these jumpers and their default configurations.

Table 5-1. Default Jumper Configurations

Designator	Default Configuration	Description
JP1	Open	CHA negative differential input. This pin can be grounded by shunting JP1 pin 1 and JP1 pin 2 for single-ended signals.
JP2	Open	CHA positive differential input or input for single-ended signals.
JP3	Open	CHB negative differential input. This pin can be grounded by shunting JP1 pin 1 and JP1 pin 2 for single-ended signals.
JP4	Open	CHB positive differential input or input for single-ended signals.
JP5	Open	EEPROM write protect function (EEPROM rewrite disabled).
JP6	Open	External CONVST is disconnected.
JP7	Installed	Shutdown pin on U8 LDO is disabled.
JP8	1-2	Negative supply for fully-differential input amplifiers is connected to –230 mV.

5.2 EVM Graphical User Interface (GUI) Software Installation

Download the latest version of the EVM GUI installer from the *Tools and Software* folder of the ADS9224R, and run the GUI installer to install the EVM GUI software on the user's computer.

Note

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Otherwise, depending on the antivirus settings, an error message may appear or the *installer.exe* file may be deleted.

Accept the license agreements and follow the onscreen instructions to complete the installation.

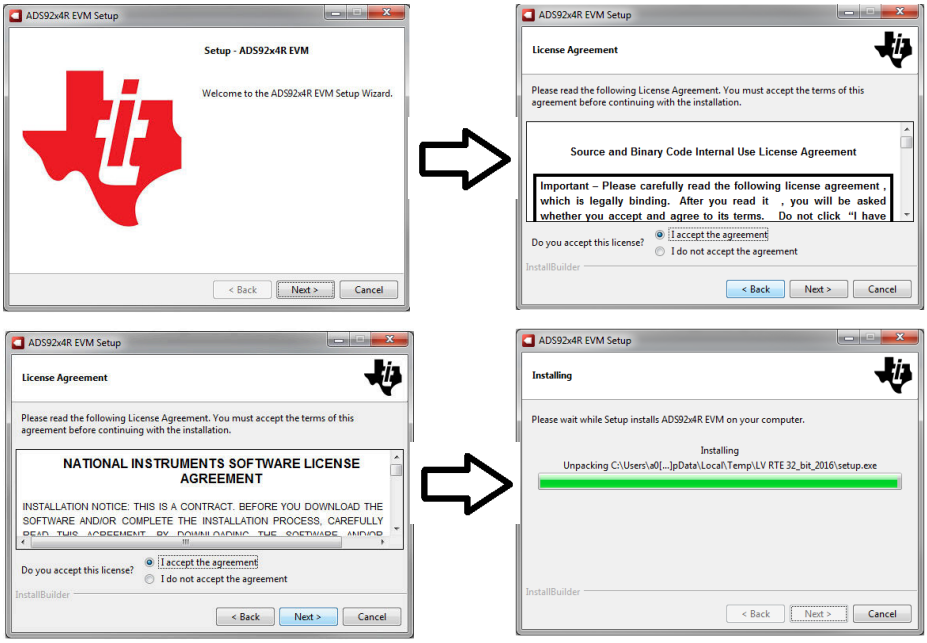


Figure 5-2. ADS9224R Software Installation Prompts

As a part of the ADS9224REVM GUI installation, a prompt with a *Device Driver Installation* will appear on the screen. Click *Next* to proceed.

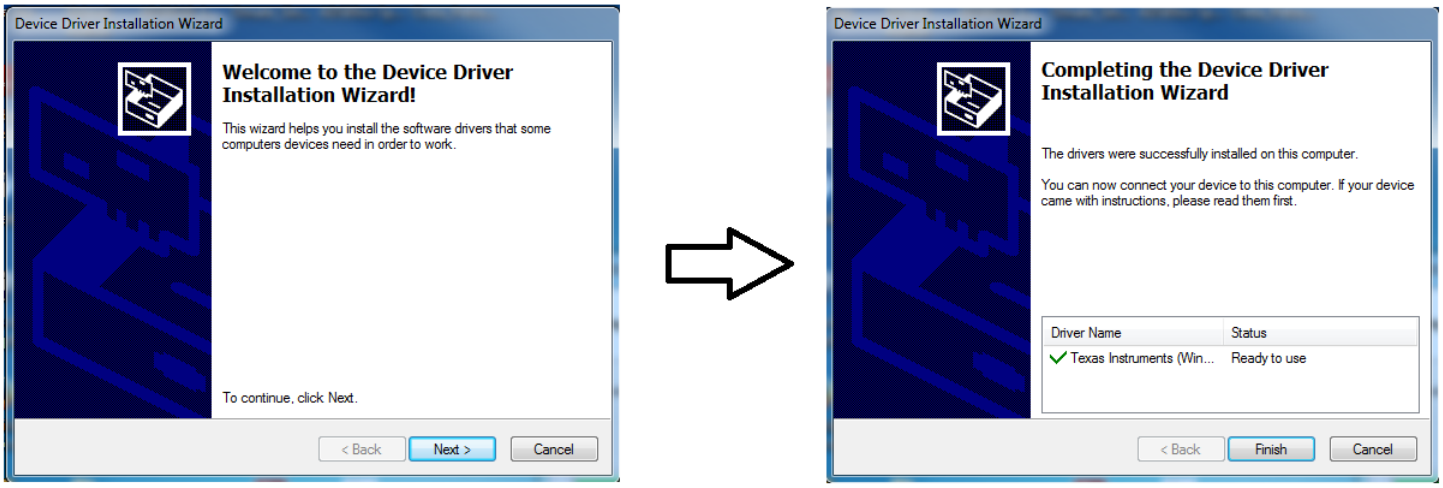


Figure 5-3. Device Driver Installation Wizard Prompts

Note

A notice may appear on the screen stating that Widows cannot verify the publisher of this driver software. Select *Install this driver software anyway*.

The ADS9224xEVM-PDK requires *LabVIEW™ Run-Time Engine,* and may prompt for the installation of this software if not already installed.

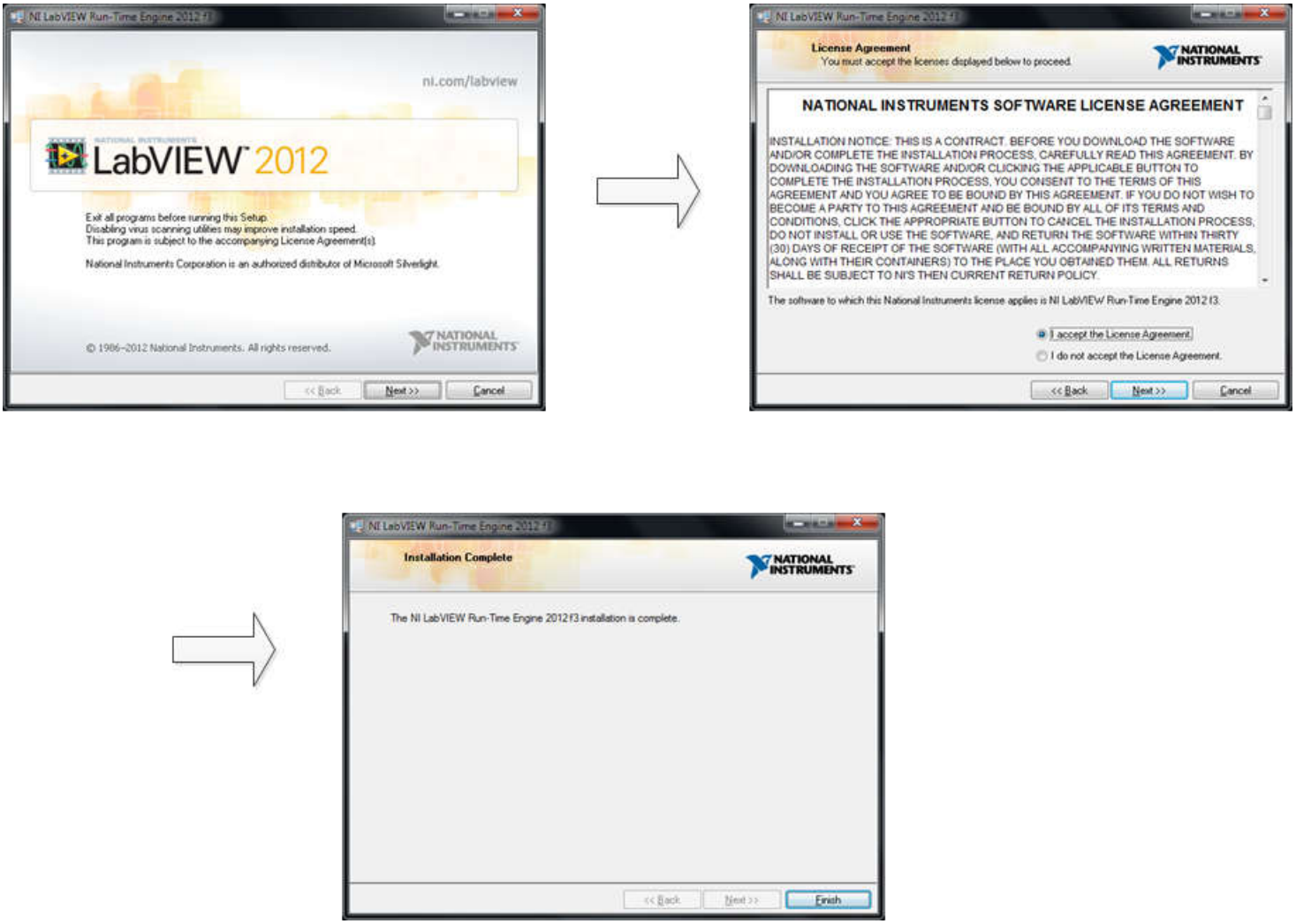


Figure 5-4. LabVIEW Run-Time Engine Installation

After these installations, verify that *C:\Program Files (x86)\Texas Instruments\ADS9224REVM* is as shown in Figure 5-5.

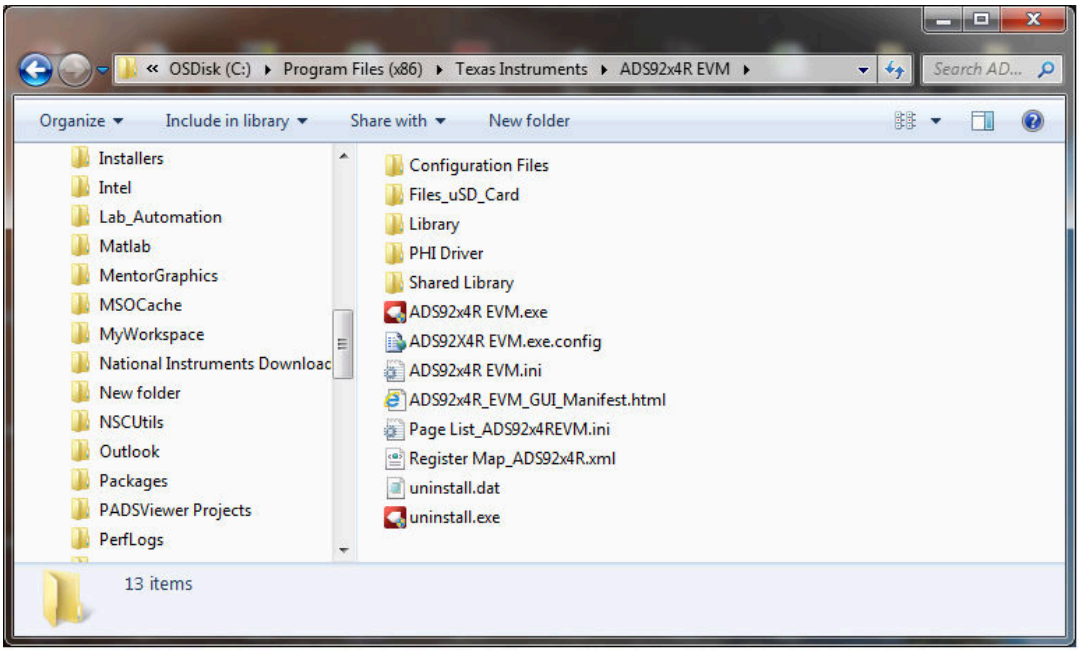


Figure 5-5. ADS9224REVM-PDK Folder Post-Installation

6 Operation

The following instructions are a step-by-step guide to connecting the ADS9224REVM-PDK to the computer and evaluating the performance of the ADS9224R:

1. Connect the ADS9224REVM to the PHI, and install the two screws, as indicated in Figure 6-1.
2. Use the provided USB cable to connect the PHI to the computer.
   - LED D5 on the PHI lights up, indicating that the PHI is powered up.
   - LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC.

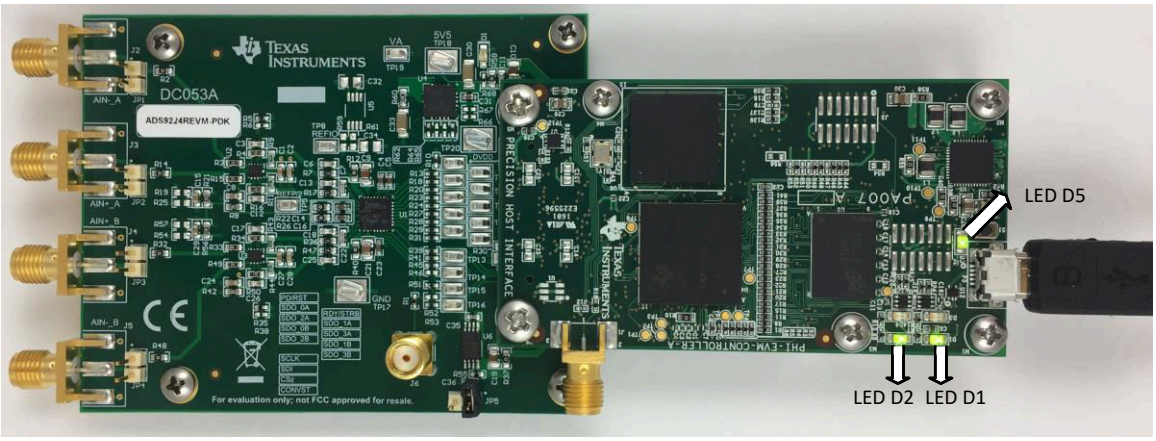


Figure 6-1. EVM-PDK Hardware Setup and LED Indicators

3. Double-click on the *ADS92x4R EVM.exe*, file to launch the ADS9224REVM-PDK GUI software. Figure 6-2 shows the ADS9224REVM software folder.

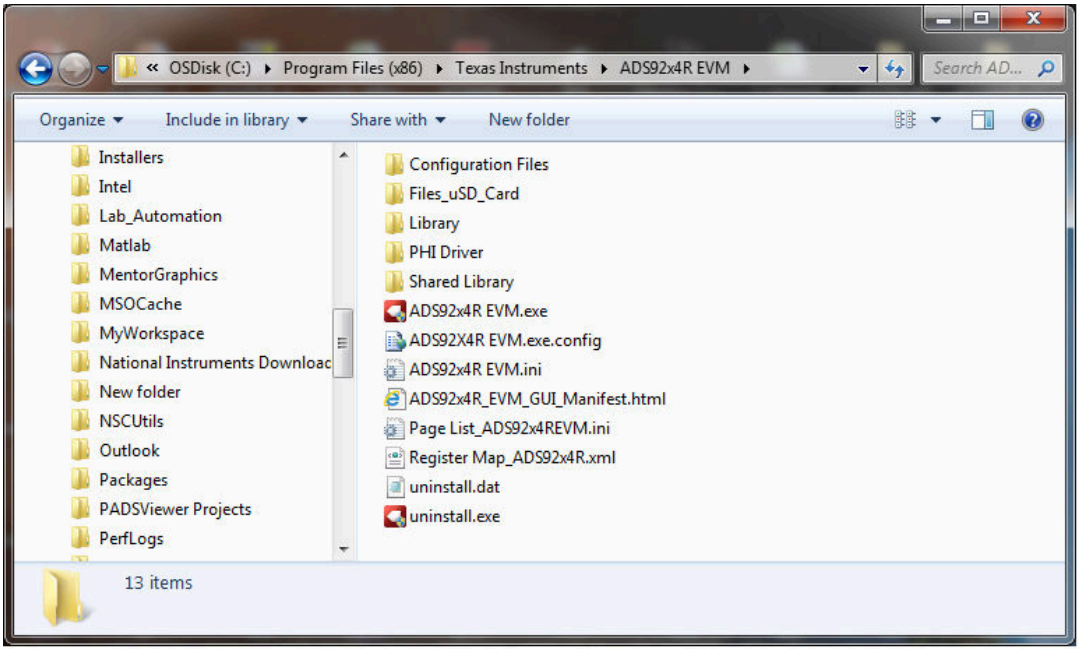


Figure 6-2. Launch the EVM GUI Software

6.1 EVM GUI Global Settings for ADC Control

Although the EVM GUI does not allow direct access to the levels and timing configuration of the ADC digital interface, the EVM GUI does allow high-level control over virtually all functions of the ADS9224R. The available functions include interface modes, sampling rate, and number of samples to be captured.

Figure 6-3 presents the input parameters and the default values of the GUI, through which the various functions of the ADS9224R are exercised. These settings are global and are applied to all the pages listed in *Pages* section at the top of the left pane.

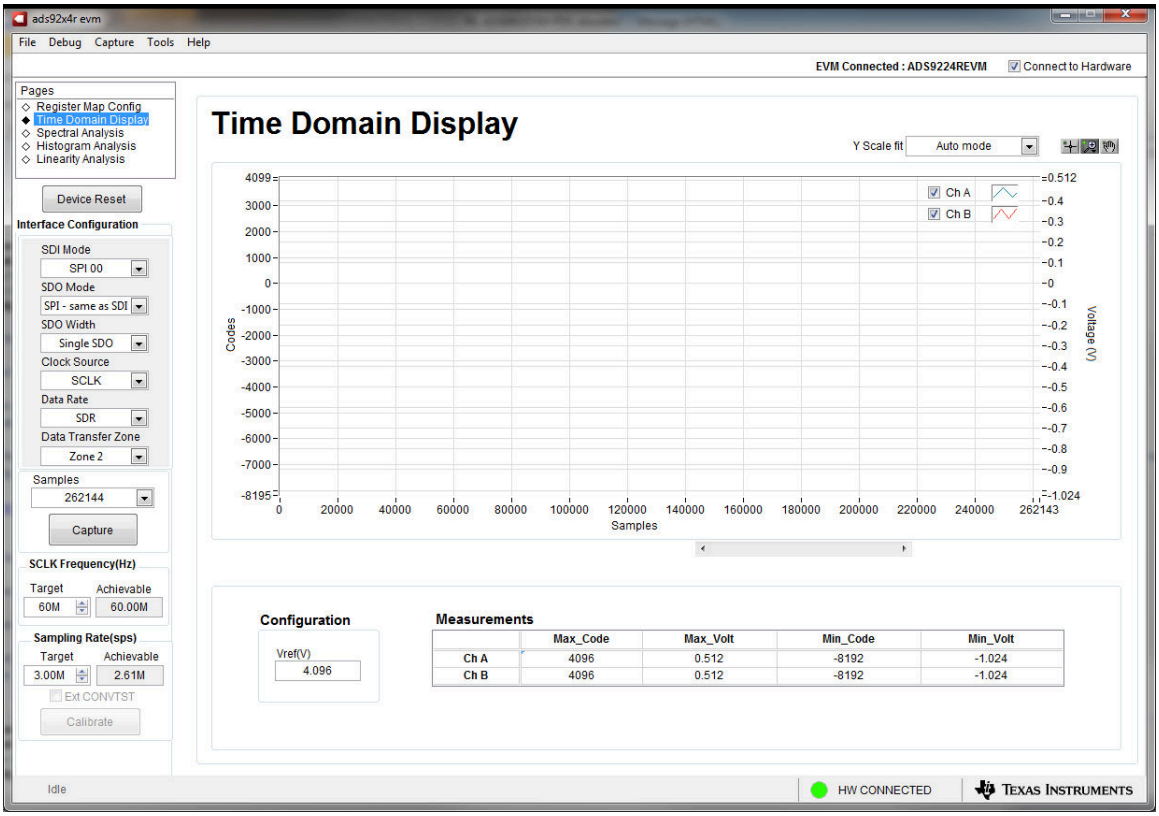


Figure 6-3. EVM GUI Global Input Parameters

The host configuration options in this pane allow the user to choose from various SPI and multiSPI host interface options available on the ADS9224R. The host always communicates with the ADS9224R using the standard SPI protocol over the single SDI lane, irrespective of the mode selected for data capture.

The drop-down boxes under the *Interface Configuration* submenu allow the user to select the data capture protocol. The *SDO Width* drop-down menu allows selection between Single-, Dual- and Quad-SDO lanes. The *SDO Mode* drop-down menu allows selection between standard SPI and multiSPI modes. The ADS9224REVM-PDK software supports maximum throughput of 3-MSPS when using Dual- and Quad-SDO lanes, and a maximum throughput of 2.61-MSPS when using Single-SDO lane. For maximum throughput of 3-MSPS, select the Dual or Quad-SDO lanes.

In SPI mode, the *SDI Mode* drop-down menu allows selection between the four SPI protocol combinations for CPOL and CPHA.

In multiSPI mode, the *Data Rate* drop-down menu allows selection between SDR and DDR modes. Detailed descriptions of each of these modes is available in the ADS9224R data sheet. The selected data capture protocol is summarized in the *Protocol Selected* indicator box.

Select *SCLK Frequency* and *Sampling Rate* on this pane. Enter the targeted values for these two parameters, and the GUI computes the best values that can be achieved, considering the timing constraints of the selected device protocol.

Specify a target SCLK frequency (in Hz), and the GUI tries to match this frequency as closely as possible by changing the PHI PLL settings. However, the achievable frequency may differ from the target value entered. Similarly, the sampling rate of the ADC can be adjusted by modifying the *Target Sampling Rate* argument (also in Hz). The achievable ADC sampling rate can differ from the target value depending on the applied SCLK frequency and selected *Device Mode*. The closest achievable match is then displayed. Thus, this pane allows the user to test various available settings on the ADS9224R in an iterative fashion until the best settings for the corresponding test scenario are found.

The *Device Reset* button functions as a master reset to both the ADS9224REVM and the GUI. When the button is pressed, the ADC resets to the reset configuration explained in the ADS9224R data sheet. The GUI also updates the interface configuration settings and the register map to reflect the device reset state.

6.2 Register Map Configuration Tool

Use the register map configuration tool to view and modify the registers of the ADS9224R. To select this tool, click on the *Register Map Config* radio button in the *Pages* section at the top of the left pane, as shown in Figure 6-4. At power-up, the values on this page correspond to the host configuration settings that enable ADC sampling at the maximum sampling rate specified for the ADC. Edit the register values by double-clicking the corresponding value field. If interface mode settings are affected by the change in register values, this change reflects on the left pane immediately. The effect of changes in the register value reflect on the ADS9224R device on ADS9224REVM-PDK based on the *Update Mode* selection, as described in Figure 6-4.

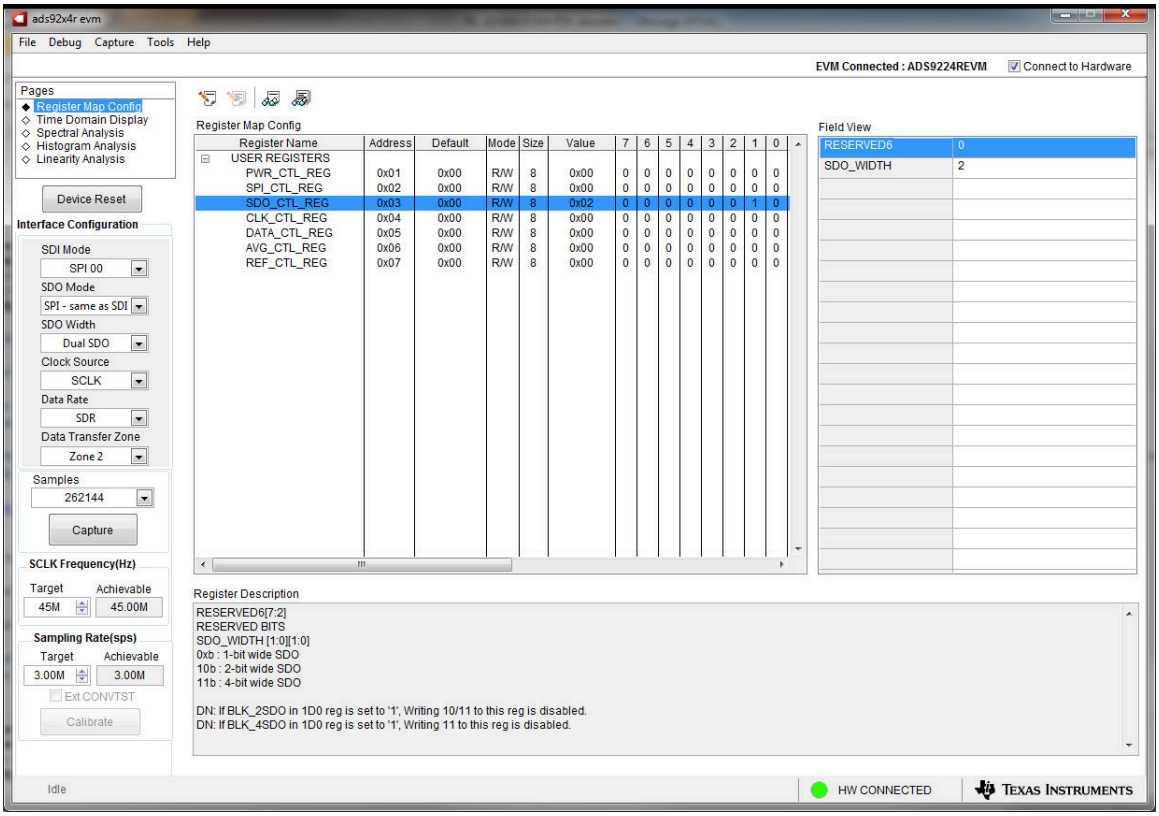


Figure 6-4. Register Map Configuration

6.3 Time Domain Display Tool

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits.

To trigger a capture of the data of the selected number of samples from the ADS9224R, as per the current interface mode settings, use the *Capture* button shown on the left pane of Figure 6-5. The sample indices are on the x-axis. The two y-axes show the corresponding output codes, as well as the equivalent analog voltages based on the specified reference voltage. To display channel A (Ch A) data or channel B (Ch B) data, select the proper channel, as shown in the top right section of Figure 6-5. Switching pages to any of the analysis tools described in the subsequent sections triggers calculations that are performed on the same set of data.

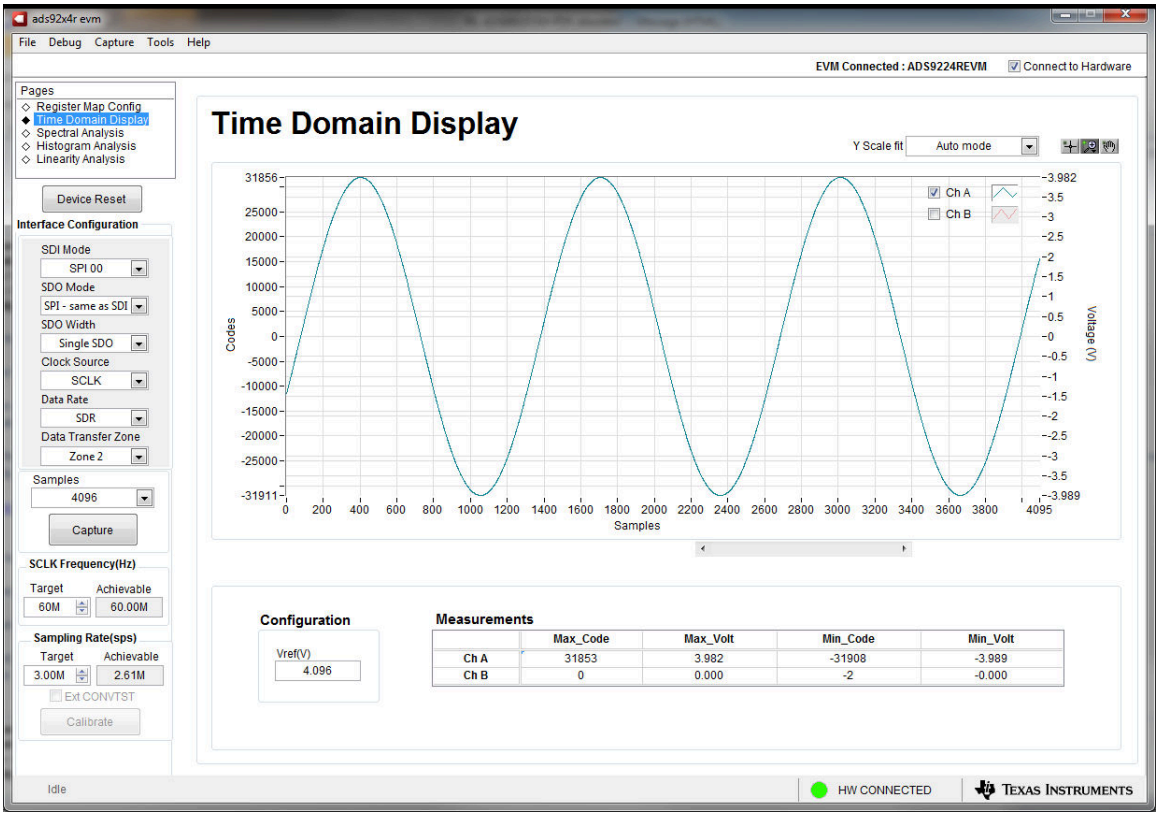


Figure 6-5. Time Domain Display Tool Options

6.4 Spectral Analysis Tool

The spectral analysis tool evaluates the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS9224R SAR ADC. Evaluation is done through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The window setting of *None* can be used to search for noise spurs over frequency in dc inputs.

For dynamic performance evaluation, the external differential source must have better specifications than the ADC. The measured system performance must not be limited by the performance of the signal source. Therefore, the external reference source must meet the source requirements mentioned in Table 6-1.

Table 6-1. External Source Requirements for Evaluation of the ADS9224R

Specification Description	Specification Value
Signal frequency	Less than f_S / 2
External source type	Balanced differential
External source common-mode voltage	0 V or floating
Source differential signal (V_{PP} amplitude for –0.5 dBFS)	±3.875 V_P OR 7.75 V_{PP}
Maximum noise	20 μV_{RMS}
Minimum SNR	103.2 dB
Maximum THD	–120 dB

For 2-kHz SNR and ENOB evaluation at a maximum throughput of 3 MSPS, the number of samples must be a minimum of 65536.

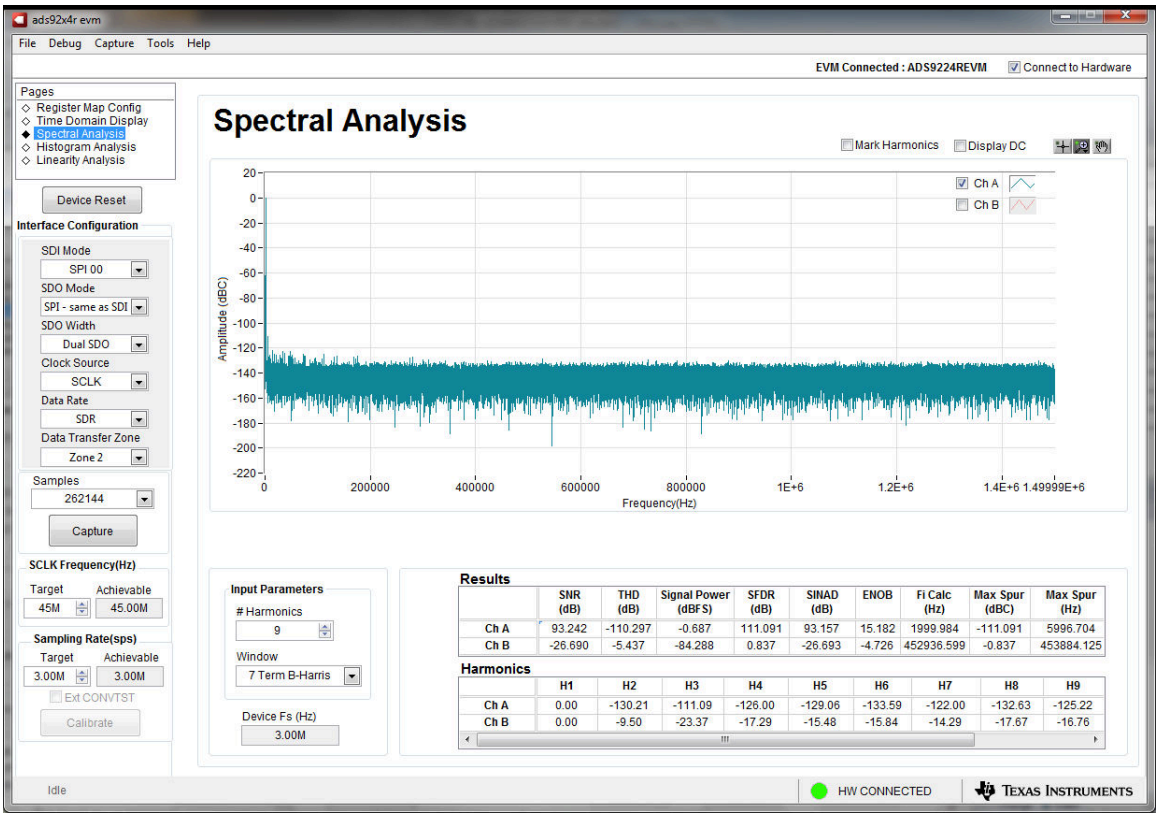


Figure 6-6. Spectral Analysis Tool

Finally, the FFT tool includes windowing options that are required to mitigate the effects of noncoherent sampling (a discussion that is beyond the scope of this document). The 7-Term Blackman Harris window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

6.5 Histogram Tool

Noise degrades ADC resolution. The histogram tool can be used to estimate *effective resolution*. Effective resolution is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a dc signal. The cumulative effect of noise coupling to the ADC output from sources (such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC) is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel.

The histogram corresponding to a dc input is displayed on clicking the *Capture* button, as shown in Figure 6-7:

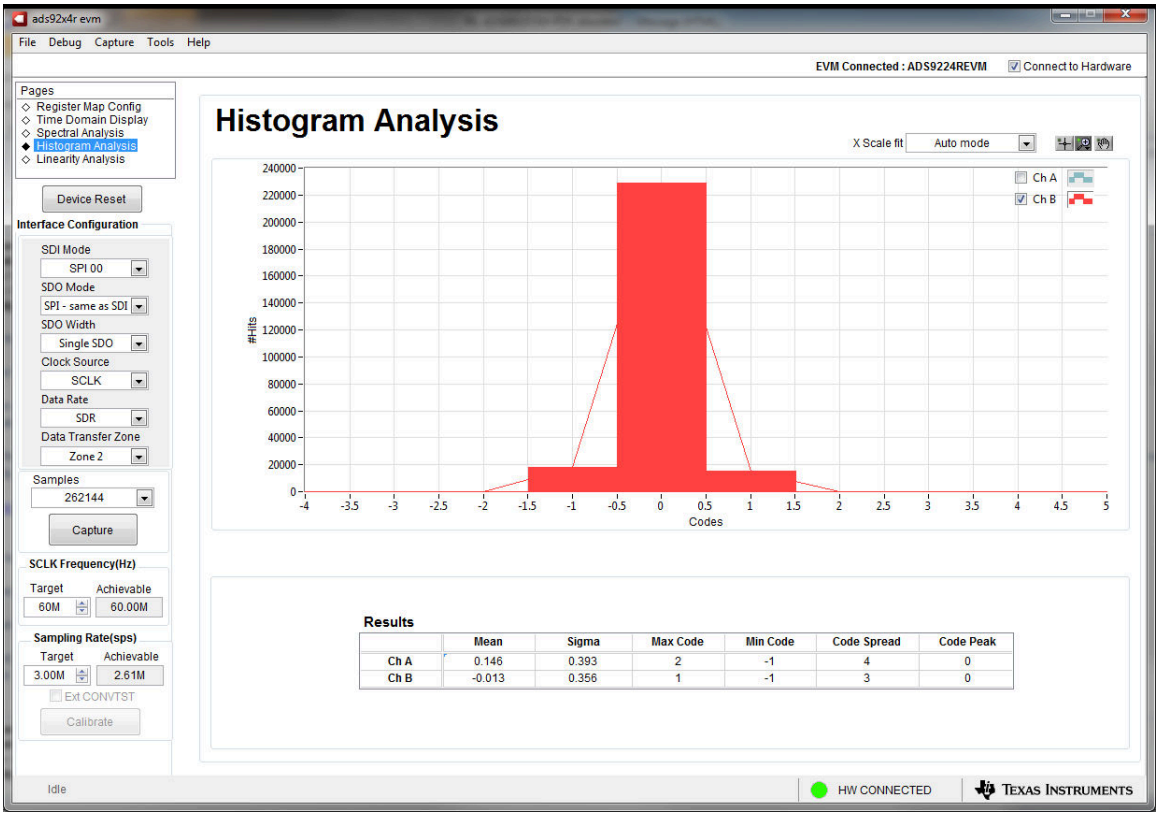


Figure 6-7. Histogram Analysis Tool

7 ADS9224REVM Bill of Materials, PCB Layout, and Schematics

This section contains the ADS9224REVM bill of materials, PCB layout, and the EVM schematics.

7.1 Bill of Materials

The following table lists the ADS9224REVM bill of materials.

Table 7-1. ADS9224REVM Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		DC053	Any
C1, C8, C15, C24, C27, C29, C37, C39, C40	9	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0603	0603	885012206046	Wurth Elektronik
C2, C28, C38, C41	4	0.01uF	CAP, CERM, 0.01 uF, 10 V, +/- 10%, X7R, 0603	0603	0603ZC103KAT2A	AVX
C3, C12, C17, C26	4	100pF	CAP, CERM, 100 pF, 50 V, +/- 1%, C0G/NP0, 0603	0603	06035A101FAT2A	AVX
C4, C5, C14, C16, C23, C31, C48	7	1uF	CAP, 1uF, 25V, ±10%, X7R, 0603	0603	CL10B105KA8NNNC	Samsung
C6, C13, C18, C25	4	330pF	CAP, CERM, 330 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	C0603C331J5GACTU	Kemet
C7, C22	2	3300pF	CAP, CERM, 3300 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H332JA01D	MuRata
C9, C10, C19, C20, C21, C30, C47	7	10uF	CAP, CERM, 10 uF, 16 V, +/- 10%, X7R, 0805	0805	CL21B106KOQNNNE	Samsung Electro-Mechanics
C11	1	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 1%, C0G/NP0, 0603	0603	GRM1885C1H102FA01J	MuRata
C33	1	47uF	CAP, CERM, 47 uF, 25 V, +/- 20%, X5R, 1206_190	1206_190	C3216X5R1E476M160AC	TDK
C35, C36, C42	3	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402	0402	GRM155R71C104KA88D	MuRata
C43, C46	2	4.7uF	CAP, CERM, 4.7 µF, 16 V,+/- 10%, X5R, 0805	0805	CL21A475KOFNNNE	Samsung Electro-Mechanics
C44	1	22uF	CAP, CERM, 22 µF, 16 V,+/- 10%, X5R, 0805	0805	CL21A226KOQNNNE	Samsung Electro-Mechanics
C45	1	0.47uF	CAP, CERM, 0.47 uF, 16 V, +/- 10%, X5R, 0603	0603	GRM188R61C474KA93D	MuRata
D1	1	Green	LED, Green, SMD	LED_0805	APT2012LZGCK	Kingbright
D2, D3	2	75V	Diode, Switching, 75 V, 0.3 A, SOD-523F	SOD-523F	1N4148WT	Fairchild Semiconductor

Table 7-1. ADS9224REVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
H1, H2, H3, H4	4		MACHINE SCREW PAN PHILLIPS 4-40	Machine Screw, 4-40, 1/4 inch	PMSSS 440 0025 PH	B&F Fastener Supply
H6, H7, H8, H9	4		Hex Standoff, #4-40, Aluminum, 1/4"	1/4 inch Aluminum Hex Standoff	1891	Keystone
H10, H11	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL
H12, H13	2		ROUND STANDOFF M3 STEEL 5MM	ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik
J1	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A	Samtec
J2, J3, J4, J5	4		Connector, End launch SMA, 50 ohm, SMT	End Launch SMA	142-0701-801	Cinch Connectivity
J6	1		SMA Straight PCB Socket Die Cast, 50 Ohm, TH	SMA Straight PCB Socket Die Cast, TH	5-1814832-1	TE Connectivity
JP1, JP2, JP3, JP4, JP5, JP6, JP7	7		Header, 100mil, 2x1, Gold, TH	Header, 100mil, 2x1, TH	HTSW-102-07-G-S	Samtec
JP8	1		Header, 100mil, 3x1, Gold, TH	Header, 100mil, 3x1, TH	HTSW-103-07-G-S	Samtec
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
R1	1	49.9	RES, 49.9, 1%, 0.25 W, 1206	1206	RC1206FR-0749R9L	Yageo America
R2, R12, R14, R22, R26, R32, R40, R48, R74	9	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603ZT0R00	Stackpole Electronics Inc
R3, R4, R15, R16, R33, R34, R49, R50	8	1.00k	RES, 1.00 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD071KL	Yageo America
R5, R10, R35, R55, R68, R71	6	10.0k	RES, 10.0 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF1002X	Panasonic

Table 7-1. ADS9224REVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R7, R17, R36, R47	4	4.32	RES, 4.32, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06034R32FKEA	Vishay-Dale
R8, R21, R42, R56	4	100	RES, 100, 1%, 0.1 W, 0603	0603	RC0603FR-07100RL	Yageo America
R9, R11, R43, R44	4	10.0	RES, 10.0, 0.1%, 0.1 W, 0603	0603	TNPW060310R0BEEA	Vishay-Dale
R13, R18, R20, R23, R24, R27, R28, R29, R31, R39, R41, R45, R51, R53	14	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GE0R00X	Panasonic
R30	1	5.11	RES, 5.11, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06035R11FKEA	Vishay-Dale
R37	1	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEY0R00V	Panasonic
R58, R72, R75	3	0	RES, 0, 5%, 0.1 W, 0603	0603	ERJ-3GEY0R00V	Panasonic
R60	1	0.1	RES, 0.1, 1%, 0.1 W, 0603	0603	ERJ-3RSFR10V	Panasonic
R62, R65	2	0	RES, 0, 5%, 0.063 W, 0402	0402	ERJ-2GE0R00X	Panasonic
R69	1	1.24k	RES, 1.24 k, 1%, 0.1 W, 0603	0603	RC0603FR-071K24L	Yageo
R70	1	1.00k	RES, 1.00 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF1001V	Panasonic
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8	8		Shunt, 100mil, Gold plated, Black	Shunt 2 pos. 100 mil	881545-2	TE Connectivity
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP19	17		Test Point, Miniature, SMT	Testpoint_Keystone_Miniature	5015	Keystone
TP17, TP18, TP20, TP21	4		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone
U1	1		Dual, Low Latency, Simultaneous-Sampling SAR ADC, RHB0032E (VQFN-32)	RHB0032E	ADS9224RRHB	Texas Instruments

Table 7-1. ADS9224REVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
U2, U3	2		Low Noise, Precision, 150MHz, Fully Differential Amplifier, RUN0010A (WQFN-10)	RUN0010A	THS4551IRUNR	Texas Instruments
U4	1		36-V, 1-A, 4.17-uVRMS, RF LDO Voltage Regulator, RGW0020A (VQFN-20)	RGW0020A	TPS7A4700RGWR	Texas Instruments
U6	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm
U7	1		Single Schmitt-Trigger Inverter, DCK0005A (SOT-SC70-5)	DCK0005A	SN74LVC1G14DCKT	Texas Instruments
U8	1		Low Noise Negative Bias Generator, 8-pin Mini SOIC, Pb-Free	DGK0008A	LM7705MM/NOPB	Texas Instruments
C32	0	1uF	CAP, CERM, 1 uF, 10 V, +/- 10%, X7R, 0805	0805	0805ZC105KAT2A	AVX
C34	0	10uF	CAP, CERM, 10 uF, 16 V, +/- 10%, X7R, 0805	0805	CL21B106KOQNNNE	Samsung Electro-Mechanics
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H5	0		Cable, USB-A to micro USB-B, 1 m		102-1092-BL-00100	CnC Tech
R6, R38	0	10.0k	RES, 10.0 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF1002X	Panasonic
R19, R25, R54, R57	0	100k	RES, 100 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD07100KL	Yageo America
R46, R52	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GE0R00X	Panasonic
R59	0	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
R61	0	0.22	RES, 0.22, 1%, 0.1 W, 0603	0603	ERJ-3RQFR22V	Panasonic
R63, R64, R66, R67	0	0	RES, 0, 5%, 0.063 W, 0402	0402	ERJ-2GE0R00X	Panasonic
R73	0	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603ZT0R00	Stackpole Electronics Inc
U5	0		3 µVpp/V Noise, 3 ppm/°C Drift Precision Series Voltage Reference, DGK0008A (VSSOP-8)	DGK0008A	REF5025AIDGKR	Texas Instruments

7.2 PCB Layout

Figure 7-1 through Figure 7-5 illustrate the EVM PCB layout.

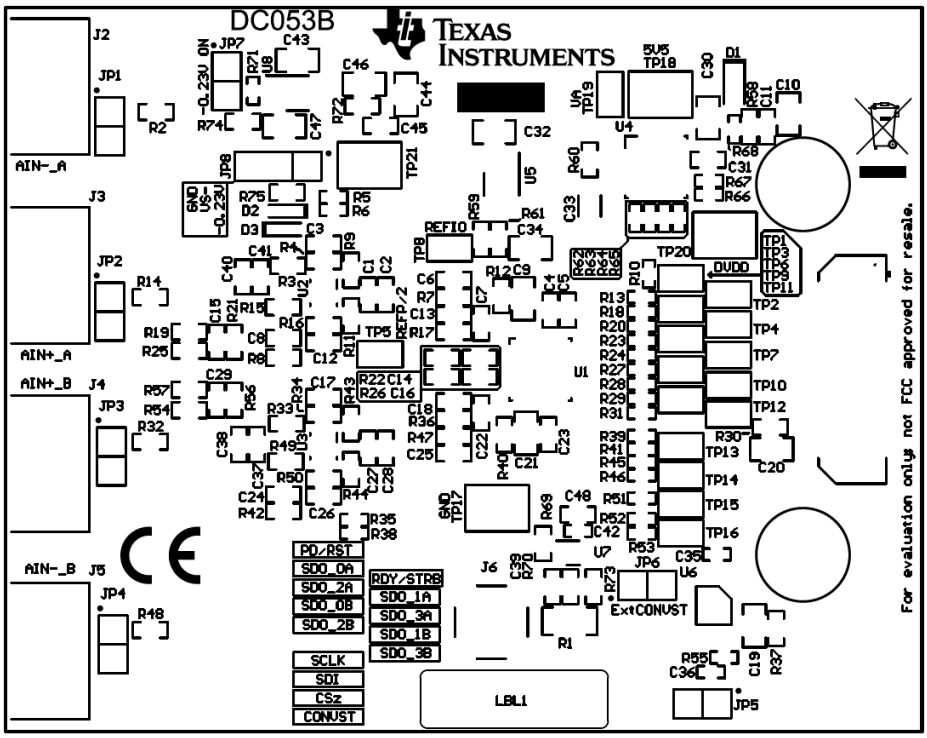


Figure 7-1. ADS9224REVM PCB Top Overlay

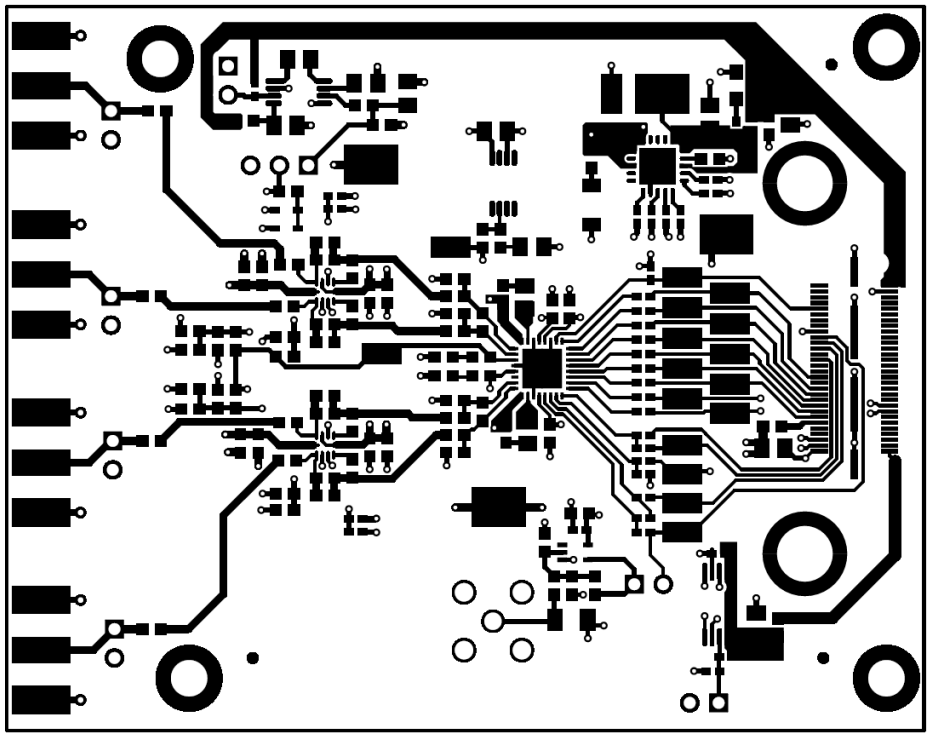


Figure 7-2. ADS9224REVM PCB Layer 1: Top Layer

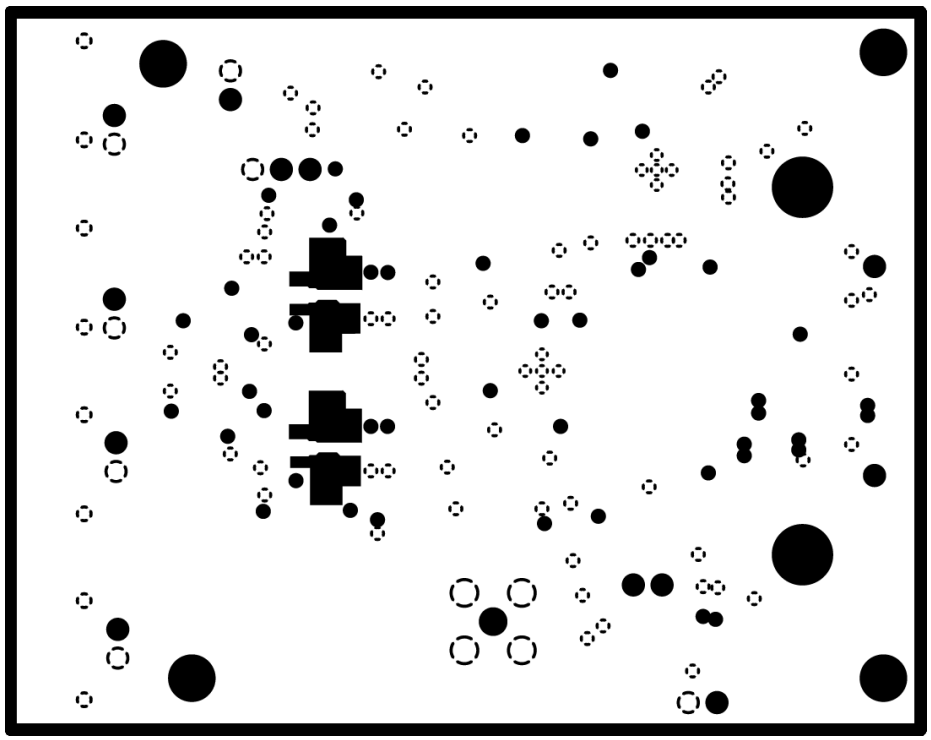


Figure 7-3. ADS9224REVM PCB Layer 2: GND Plane

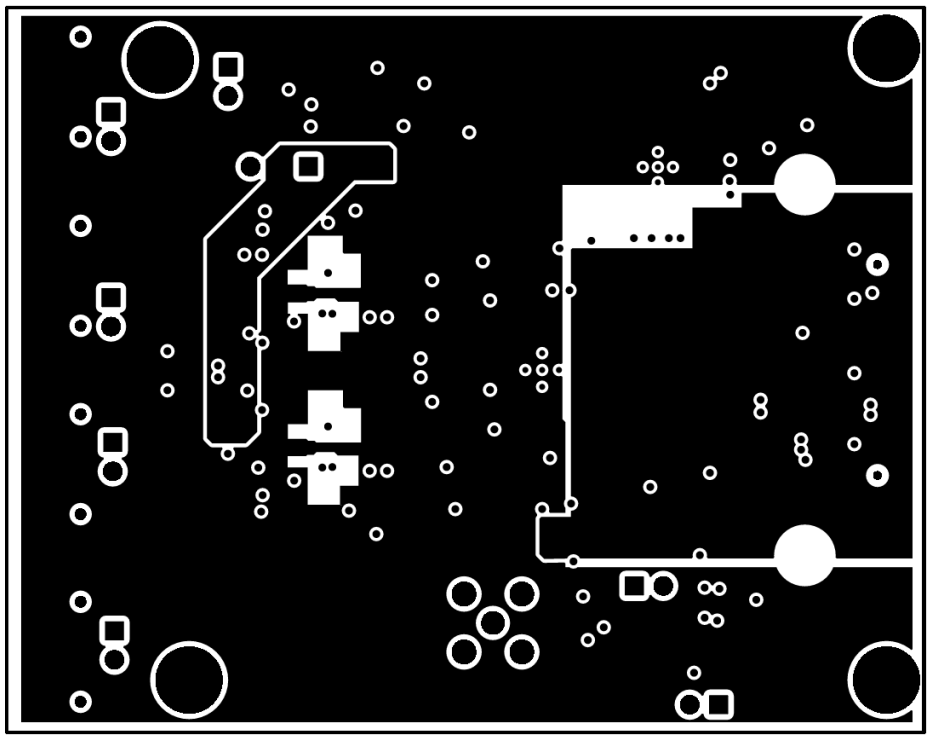


Figure 7-4. ADS9224REVM PCB Layer 3: Power Planes

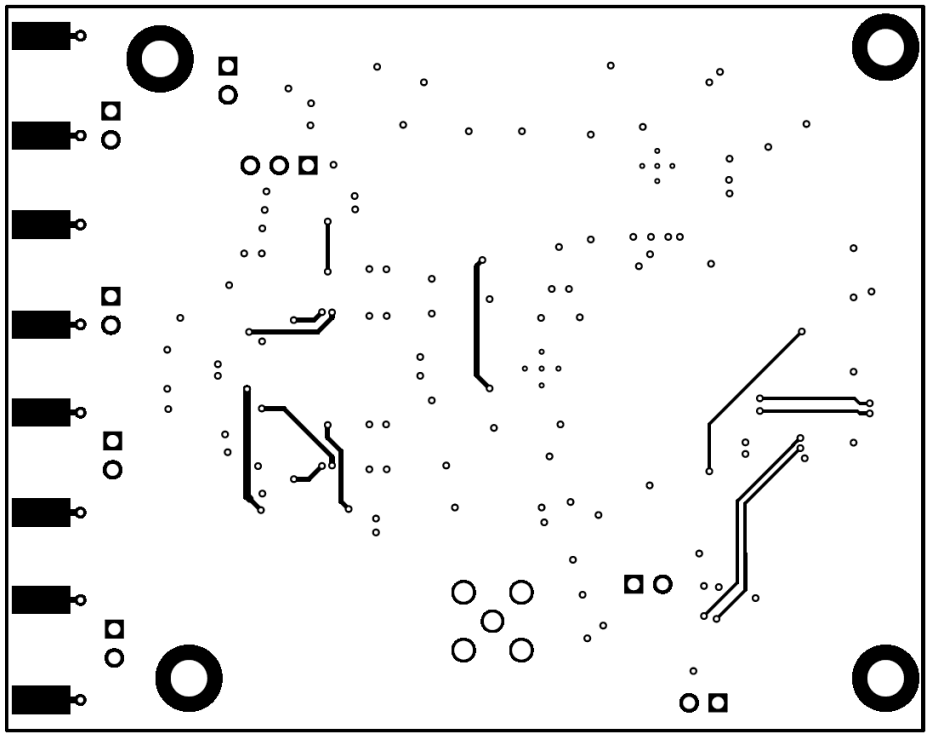


Figure 7-5. ADS9224REVM PCB Layer 4: Bottom Layer

7.3 Schematics

Figure 7-6 and Figure 7-7 illustrate the EVM schematics.

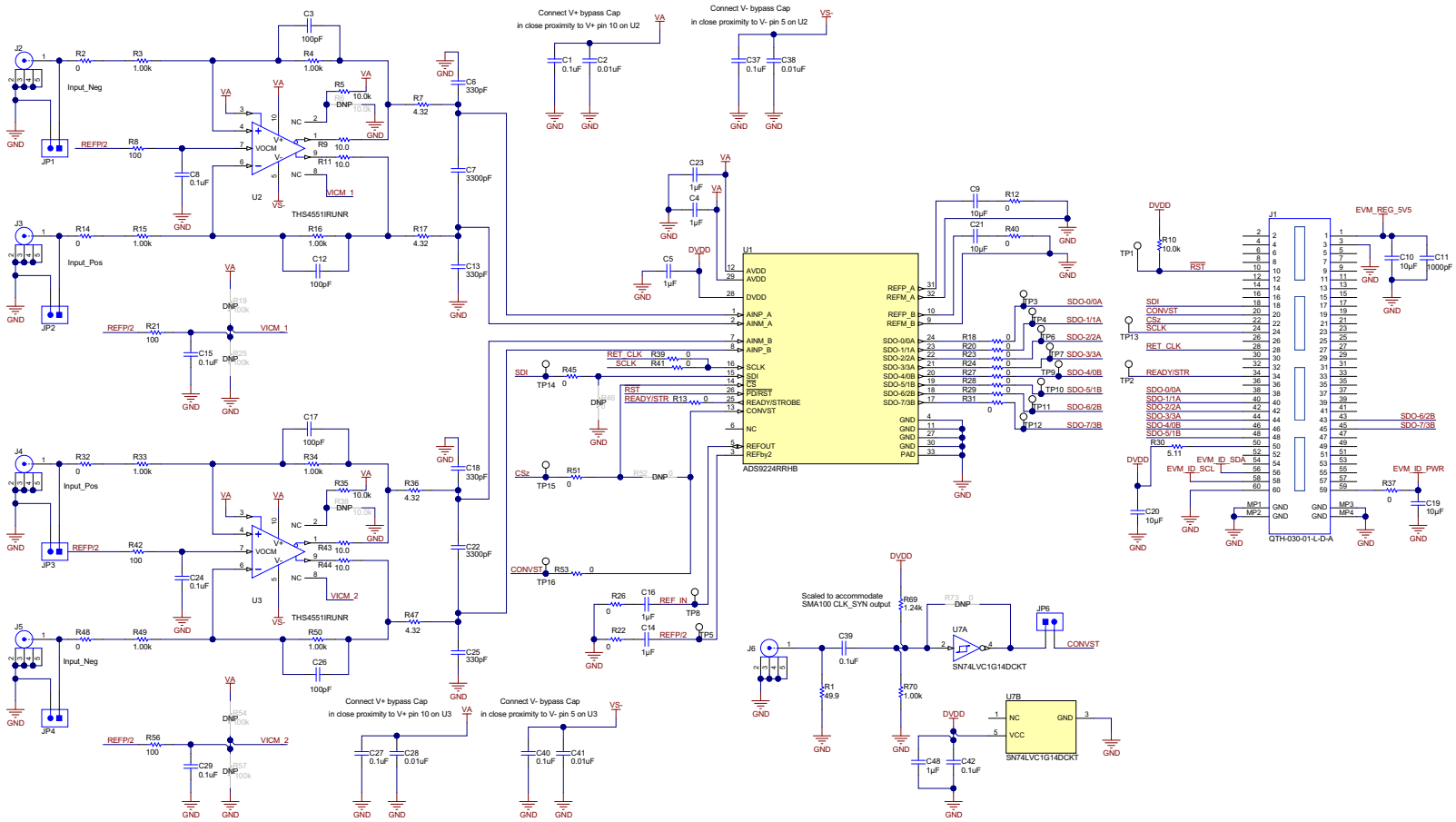
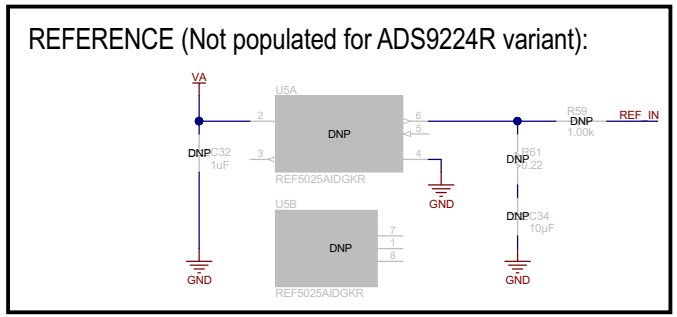
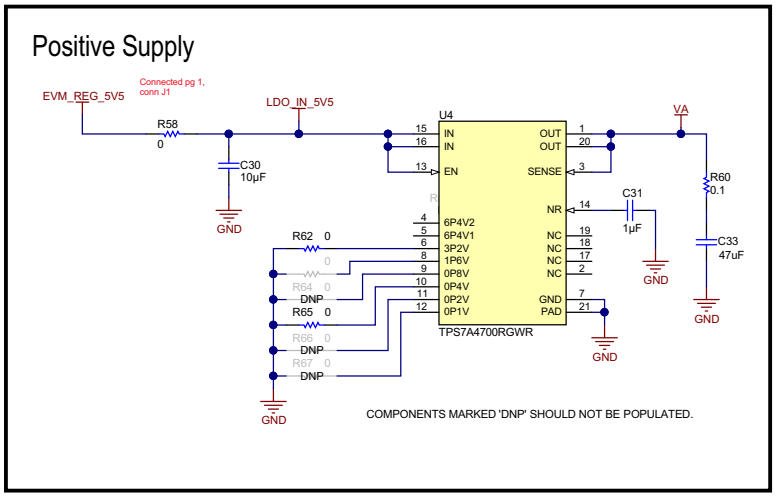
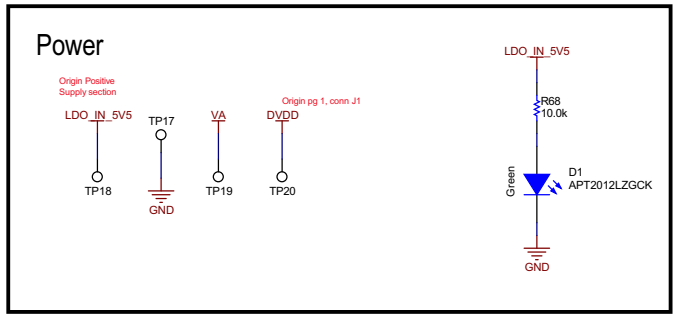
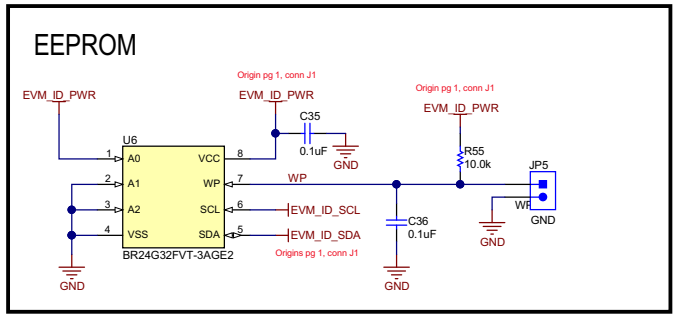


Figure 7-6. ADS9224REVM Schematic Diagram 1









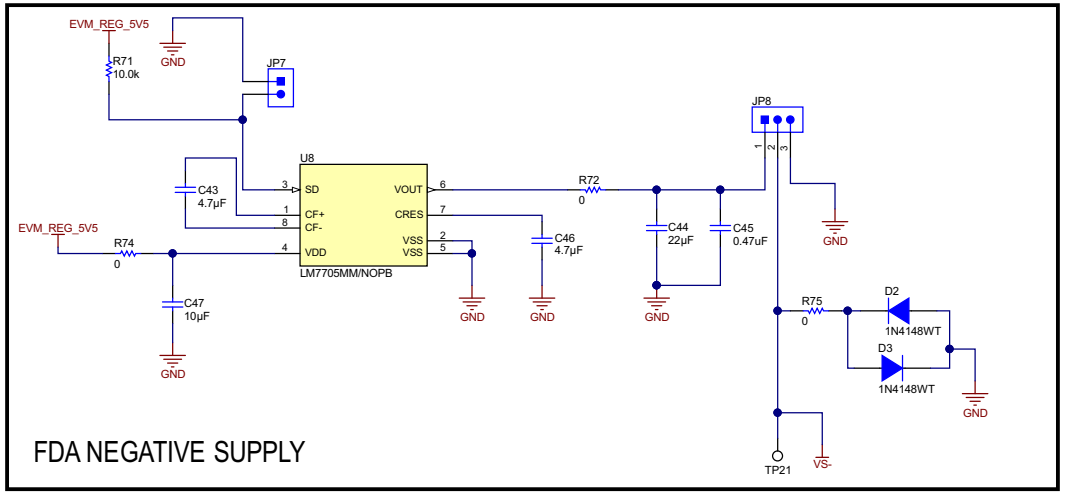


Figure 7-7. ADS9224REVM Schematic Diagram 2

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2019) to Revision B (March 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (July 2018) to Revision A (June 2019)	Page
• Changed J2, J4, and J5 in *J2 to J5 SMA Analog Interface Connections* table	5
• Changed *JP1 to JP4 Header Descriptions* table	5
• Changed discussion of how the input signal must be limited in *Input Signal Path* section	6
• Added REFby2 discussion and added test point TP8 to discussion of REFOUT in *ADS9224R Internal Reference* section	7
• Added *SPI Test Points* table to *multiSPI™ for ADC Digital IO* section	7
• Added last paragraph and *Power-Supply Test Points* table to *Power Supplies* section	8
• Changed *shunts can be used on jumpers JP2* to *shunts can be used on jumpers JP1* in *Default Jumper Settings* section	9
• Added JP6, JP7, and JP8 rows to *Default Jumper Configurations* table	9
• Changed *signal frequency* and *source differential signal* specification values in *External Source Requirements for Evaluation of the ADS9224R* table	17
• Changed *ADS9224EVM Bill of Materials* table	19
• Changed *Schematics* figures	26

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