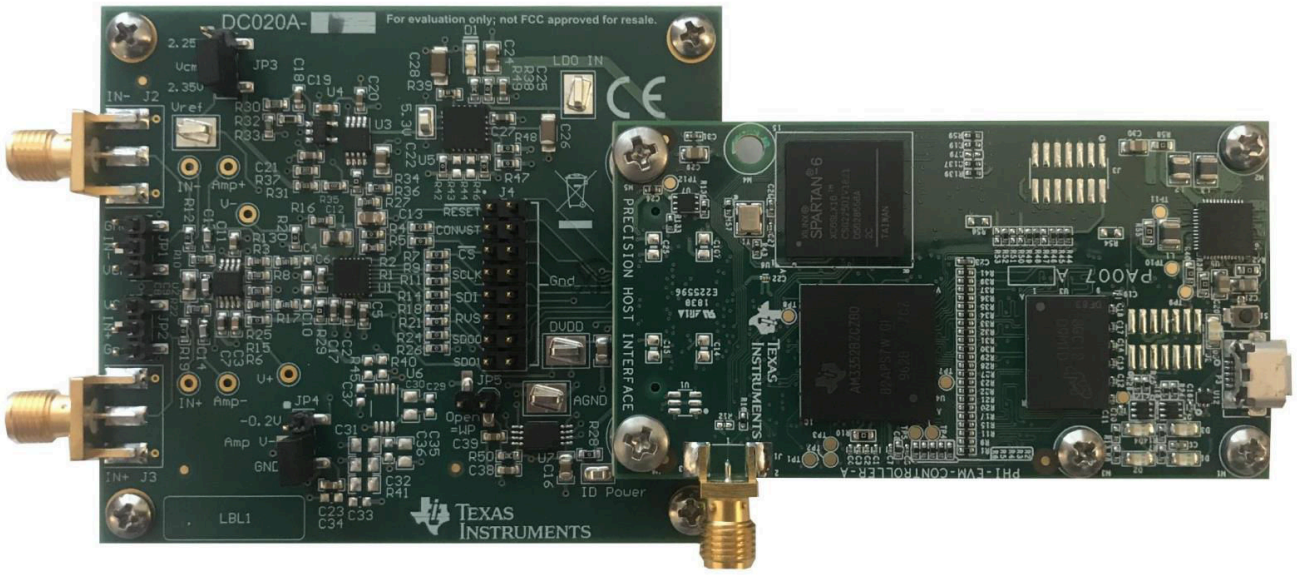
User's Guide

ADS8900EVM-PDK Evaluation Module

ABSTRACT



This user's guide describes the operation and use of the ADS8900B evaluation module (EVM). The ADS8900B is a 20-bit, fully differential, unipolar, successive approximation register (SAR), analog-to-digital converter (ADC) with a maximum throughput of 1 MSPS. The device is a very low-power ADC with excellent noise and distortion performance for ac or dc signals. The performance demonstration kit (PDK) eases EVM evaluation with additional hardware and software for computer connectivity through a universal serial bus (USB). The ADS8900BEVM-PDK includes the ADS8900BEVM as a daughter card, precision host adaptor (PHI) digital controller, and USB cable. This user's guide covers circuit description, schematic diagram, and bill of materials for the ADS8900BEVM daughter card.

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1 EVM Overview

Table 1-1 lists the related documents that are available for download from Texas Instruments at www.ti.com.

Table 1-1. Related Documentation

Device	Literature Number
ADS8900	SBAS728
THS4551	SBOS778
OPA376	SBOS406
TPS7A4700	SBVS204
REF5050	SBOS410

1.1 ADS8900EVM-PDK Kit Features

The ADS8900BEVM-PDK includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS8900B ADC. The ability to emulate the ADS8910B and ADS8920B ADCs is also available. This feature allows for diagnostic testing and accurate performance evaluation of these two devices using the ADS8900B.
- USB powered: no external power supply is required.
- The PHI controller that provides a convenient communication interface to the ADS8900B ADC over a USB 2.0 (or higher) for power delivery as well as digital input and output.
- Easy-to-use evaluation software for Microsoft® Windows® 7, Windows® 8, and Windows® 10 operating systems.
- The software suite includes graphical tools for data capture, histogram analysis, spectral analysis, and linearity analysis. This suite also has a provision for exporting data to a text file for post-processing.

1.2 ADS8900EVM Features

As shown in Figure 1-1, the ADS8900EVM includes the following features:

- Onboard low-noise and low-distortion ADC input drivers optimized to meet ADC performance.
- Onboard precision 5.0-V voltage reference filtered and followed by a low-noise, low-offset, and low-impedance buffer. The reference driver circuit is optimized for 1-LSB voltage regulation under maximum loading conditions at full device throughput of 1 MSPS.
- Onboard ultra-low-noise, low-dropout (LDO) regulator for excellent 5-V, single-supply regulation of all operational amplifiers and voltage reference.

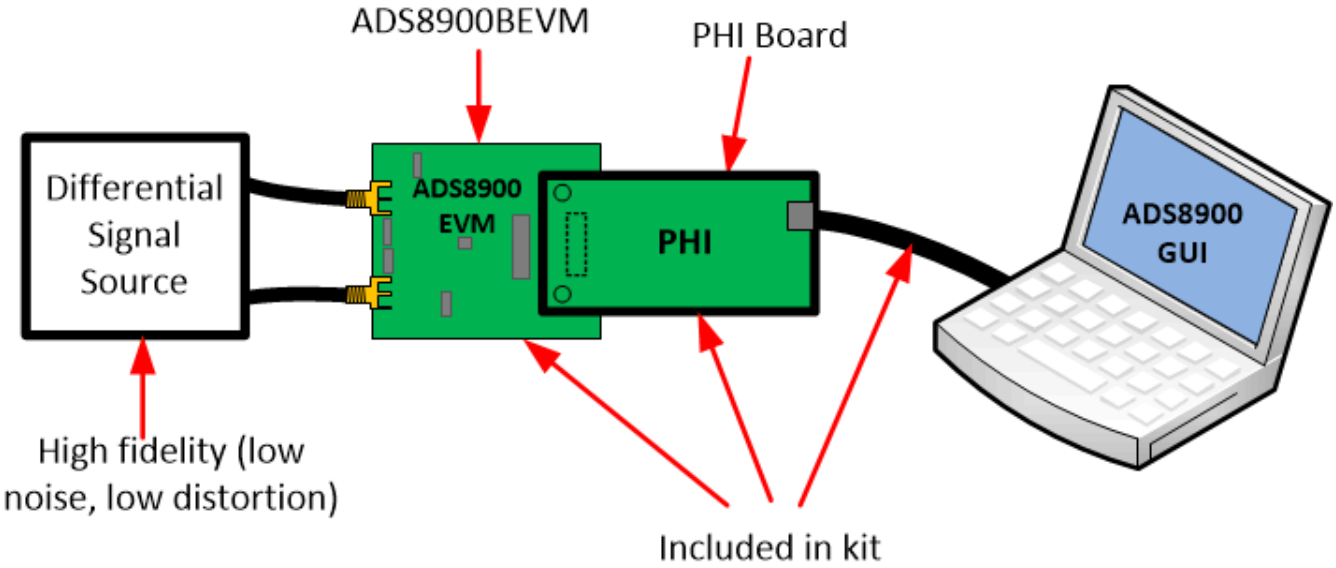


Figure 1-1. System Connection for Evaluation

2 Analog Interface

As an analog interface, the evaluation board uses operational amplifiers in a variety of configurations to drive the ADS8900B signal and reference inputs. This section covers driver details including jumper configuration for different input signal common modes and board connectors for a differential signal source.

2.1 ADS8900B Connections and Decoupling

Figure 2-1 shows the power-supply connections, reference connections, and the associated decoupling filter capacitors for the ADS8900. The reference filter comprised of C12 and R16 is at the reference buffer output and must be as close as possible to the ADC reference pin (pin 7). This figure also shows the analog input connections, but the driver amplifier is in Figure 2-2. The digital signal connections are shown on the right hand side of Figure 2-1. The connector J4 is a test point header that can be used to monitor digital signals. Also, J4 can be used to apply digital signals in cases where the included PHI controller is not used. Each digital signal has a series 0-Ω resistor. This resistor can be changed to a 50-Ω resistor to provide signal conditioning for noisy digital signals. The included PHI controller digital signals do not require this conditioning so the default value is 0 Ω. Figure 2-1 also shows the PHI connector, J1. This connector provides the SPI digital signals, power supplies, and I^2C communications for the EVM.

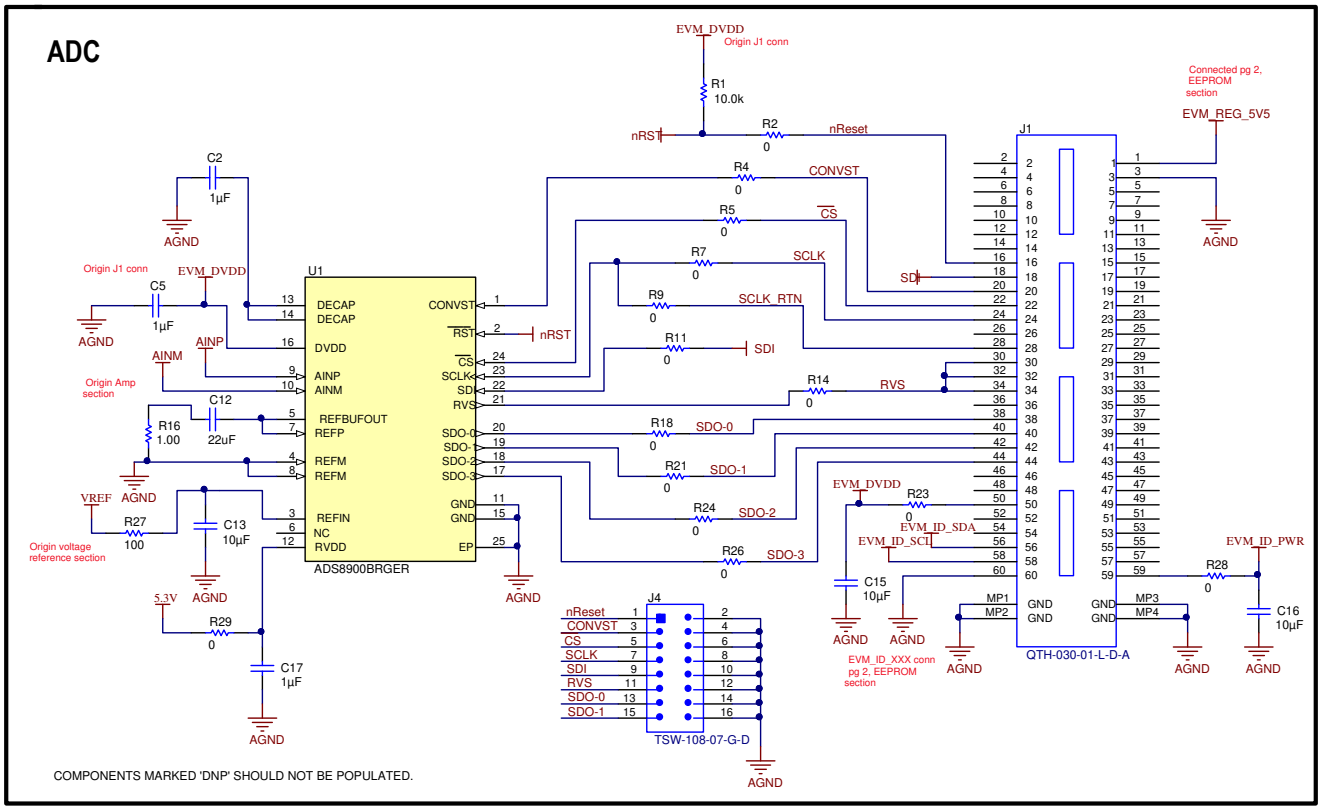


Figure 2-1. Decoupling and ADC Signal Connections

2.2 ADC Amplifier Input Drive

Figure 2-2 shows the fully differential drive amplifier (FDA) configurations used for this EVM. The FDA is a very common type of amplifier used in driving fully differential data converters because this amplifier outputs a differential signal with a fixed common-mode voltage as required by the ADC. The common-mode voltage is set on pin 2 of U2. This voltage is generated in Figure 2-3 and can be set to either 2.5 V or 2.6 V with jumper JP3. The THS4551 is used in this example because this device is a very low-noise and low-distortion FDA. The FDA gain is set to 1 V/V using R3, R10, R25, and R22. For best distortion, 0.1% resistors are used. The output filter is optimized for good ADC settling (R8, R17, and C6). The charge bucket capacitor C6 must be a C0G-type capacitor for low distortion. The jumpers JP1 and JP2 are not installed if the input signal is differential. Section 2.3 describes how these jumpers can be used to convert a single-ended signal to a differential signal.

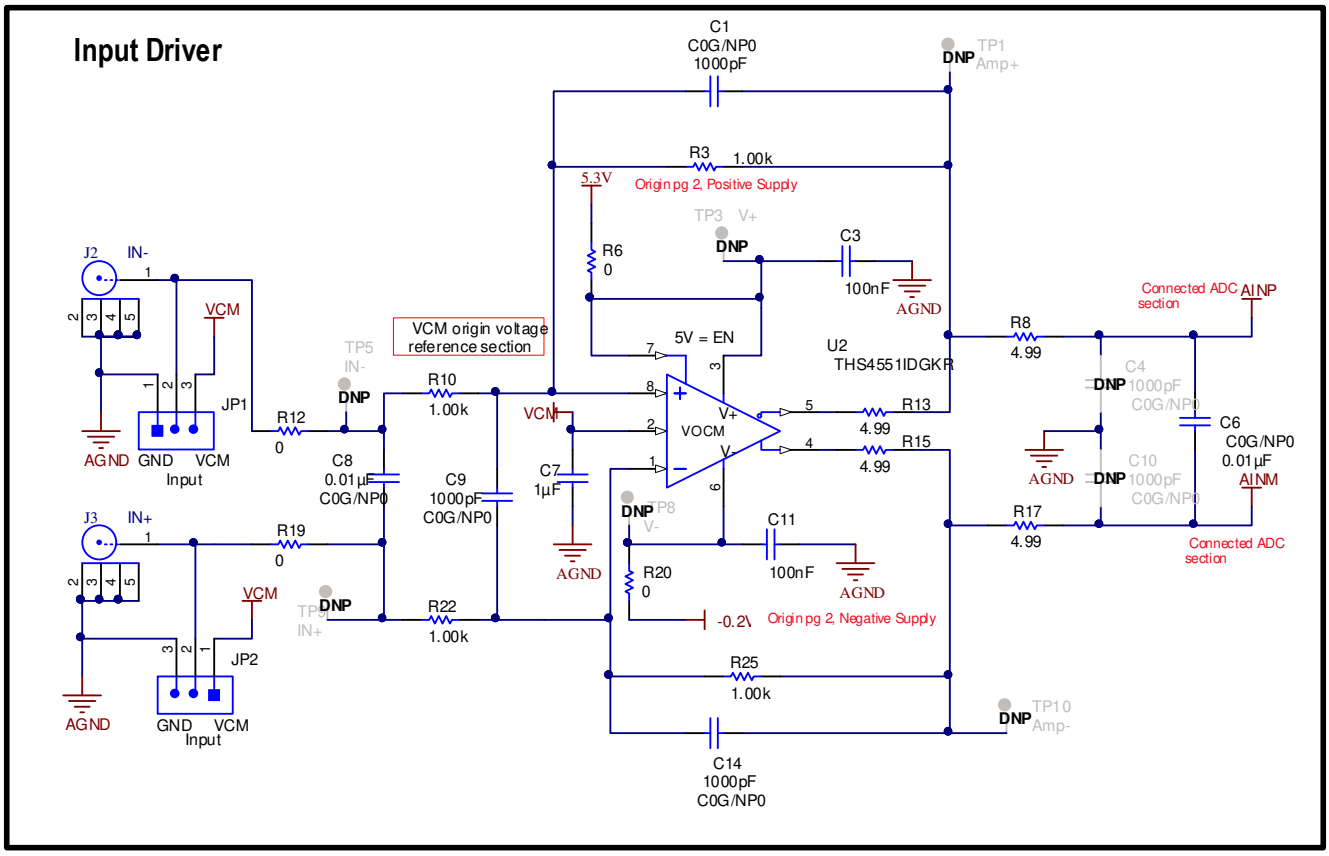


Figure 2-2. THS4551 Fully Differential Amplifier ADC Drive

2.3 Voltage Reference and VCM Scaling

Figure 2-3 shows the voltage reference circuit, output filtering, voltage divider, and buffer circuit. The REF5050 5-V, low-noise, low-drift voltage reference is used here. The voltage reference is connected to the ADC directly to the right of R34 on the VREF node. The filter R36 and C22 are selected for best noise performance and stability. As noted in the REF5050 data sheet, the series resistor R36 is included to keep the capacitor ESR in the desired range. The reference connects to a buffered input on the ADC so the reference does not need to respond to transient current demands. The voltage divider (R36, R31, and R37), and associated jumper (JP3) are used to set the common-mode input for the FDA. The jumper provides the option of changing the common-mode input from 2.5 V to 2.6 V. A common-mode of 2.5 V is midscale for a 0-V to 5-V FDA output swing. Because of output swing limitations, some distortion may occur when the signal swings towards 0 V. The 2.6-V common-mode shifts the signal away from ground to avoid this distortion. The theory behind this approach is documented in the *Driving a SAR ADC with a Fully Differential Amplifier* video.

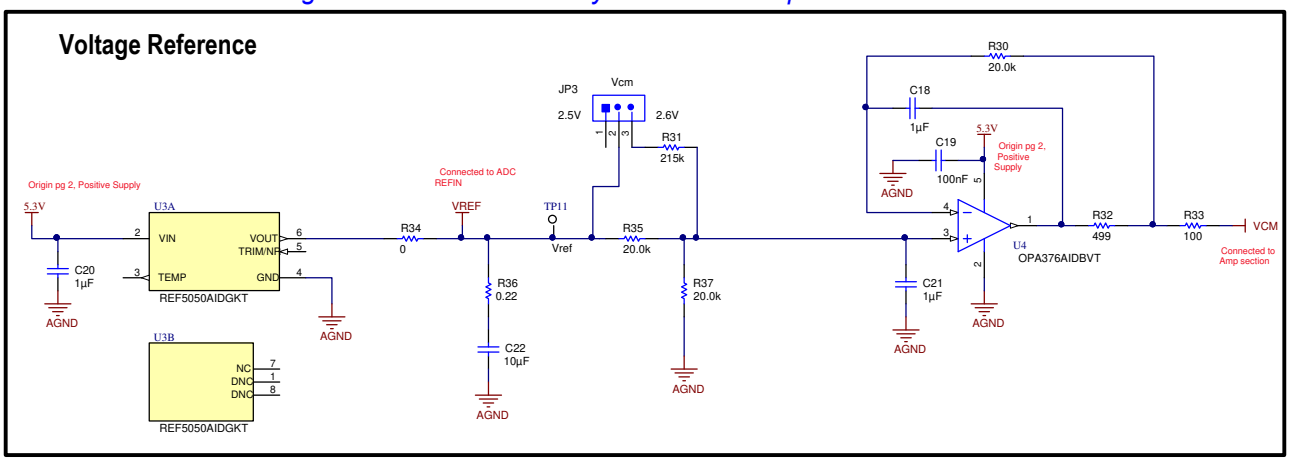


Figure 2-3. Voltage Reference and VCM Scaling

3 Digital Interface

As noted in Section 1, the EVM interfaces with the PHI that, in turn, communicates with the computer over USB. There are two devices on the EVM with which the PHI communicates: the ADS8900B ADC (over SPI or multiSPI™) and the EEPROM (over I^2C). The EEPROM comes preprogrammed with the information required to configure and initialize the ADS8900BEVM-PDK platform. When the hardware is initialized, the EEPROM is no longer used.

3.1 multiSPI™ for ADC Digital I/O

The ADS8900BEVM-PDK supports all interface modes, as detailed in the ADS8900B data sheet. In addition to the standard SPI modes (with single-, dual- and quad-SDO lanes), the multiSPI modes support single- and dual-data output rates and the four possible clock source settings as well. The PHI is capable of operating at a 1.8-V logic level and is directly connected to the digital I/O lines of the ADC.

3.2 I^2C Bus for Onboard EEPROM

The circuit shown in Figure 3-1 is used with the EVM controller (PHI), for EVM identification. This circuit is not required by the ADS8900B for operation. The jumper (JP5) is write protected and does not need to be changed for EVM operation.

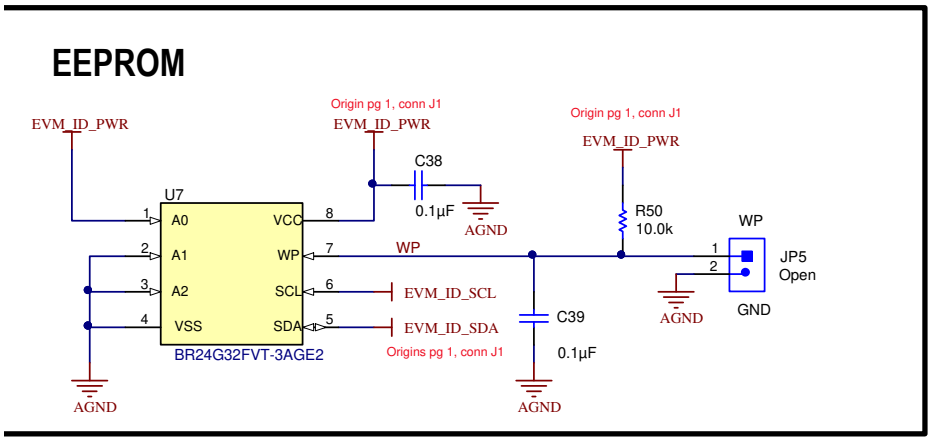


Figure 3-1. EEPROM for EVM ID

4 Power Supplies

The PHI provides multiple power-supply options for the EVM, derived from the computer USB supply. The EEPROM on the ADS8900BEVM uses a 3.3-V power supply generated directly by the PHI. The positive and negative supplies are derived from the 5.5-V regulated supply from the PHI (EVM_REG_5V5).

4.1 Positive Supply and Test Points

The analog supply of the ADC (AVDD = 5.3 V) is powered by the TPS7A4700RGWR (U5) low-dropout regulator (LDO). The input to this LDO is the regulated 5.5-V supply from the PHI. This LDO can be programed to different voltages by soldering or desoldering resistors R42 to R48.

A test point for each power supply is provided. Furthermore, a light-emitting diode (LED) is used to indicate when the 5.5-V supply from the PHI turns on. This power turns on shortly after the software is booted. The EVM is not powered until the software is started, so TI does not recommend connecting the external signal source until the EVM is powered. Figure 4-1 shows the positive supply and test points for the TPS7A4700RGWR.

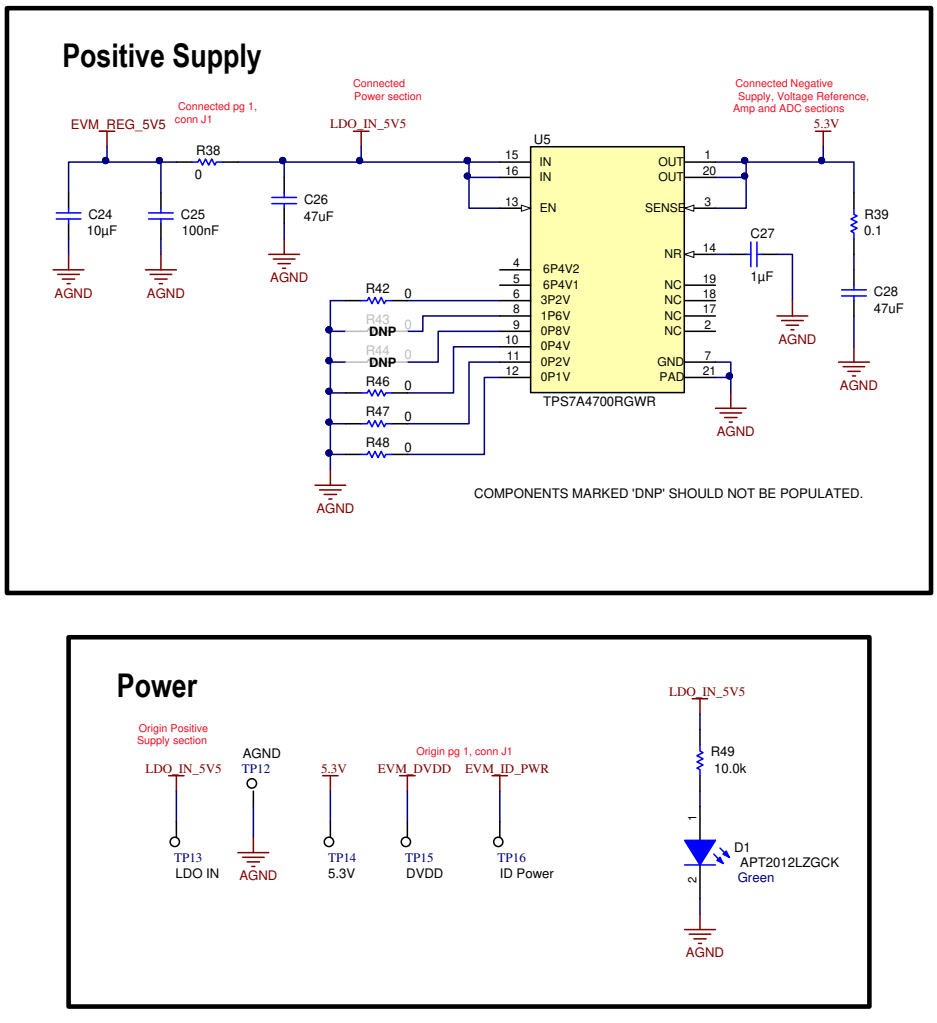


Figure 4-1. Positive Supply and Test Points

4.2 Negative Supply

The negative supply, as shown in Figure 4-2, is not installed on the EVM but can be populated in the rare circumstance that this option is desired. The purpose of this negative charge pump is to generate a small –0.23-V power-supply rail for the FDA driver amplifier to assure that the amplifier can swing to 0 V without an output swing limitation. This feature is needed to run the linearity sweep for the EVM because the linearity test requires a linear sinusoidal input signal that drives below 0 V and above 5 V (that is, a saturated input). Without the negative charge pump, the THS4551 amplifier distorts when its output approaches 0 V.

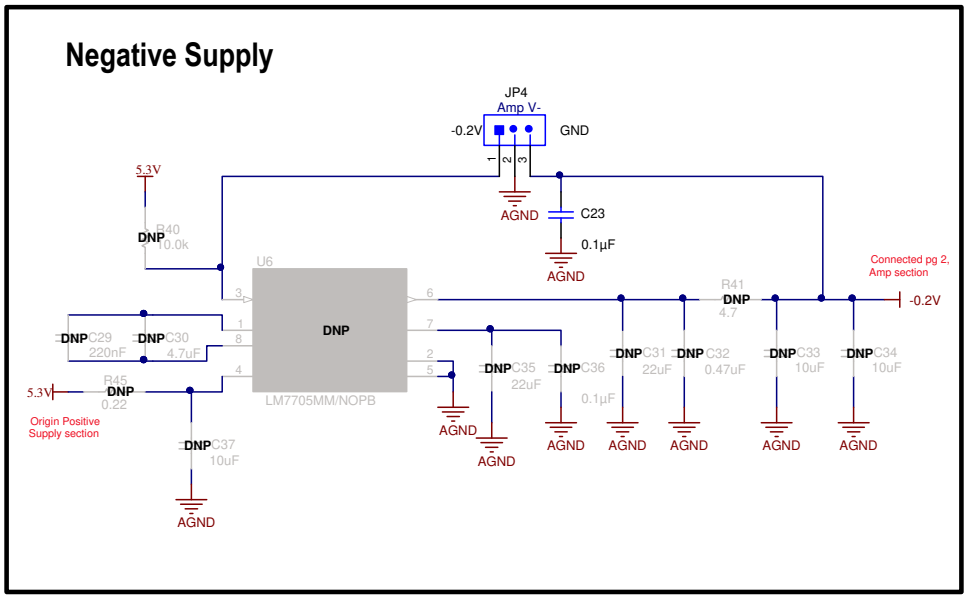


Figure 4-2. Negative Supply

5 ADS8900EVM-PDK Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for the proper operation of the ADS8900EVM-PDK.

5.1 Software Installation

Download the latest version of the EVM GUI installer from the *Tools and Software* folder of the ADS8900BEVM and run the GUI installer to install the EVM GUI software on your computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message may appear or the installer. The .exe file can be deleted after installation.

Accept the license agreements and follow the on-screen instructions shown in Figure 5-1 to complete the installation.

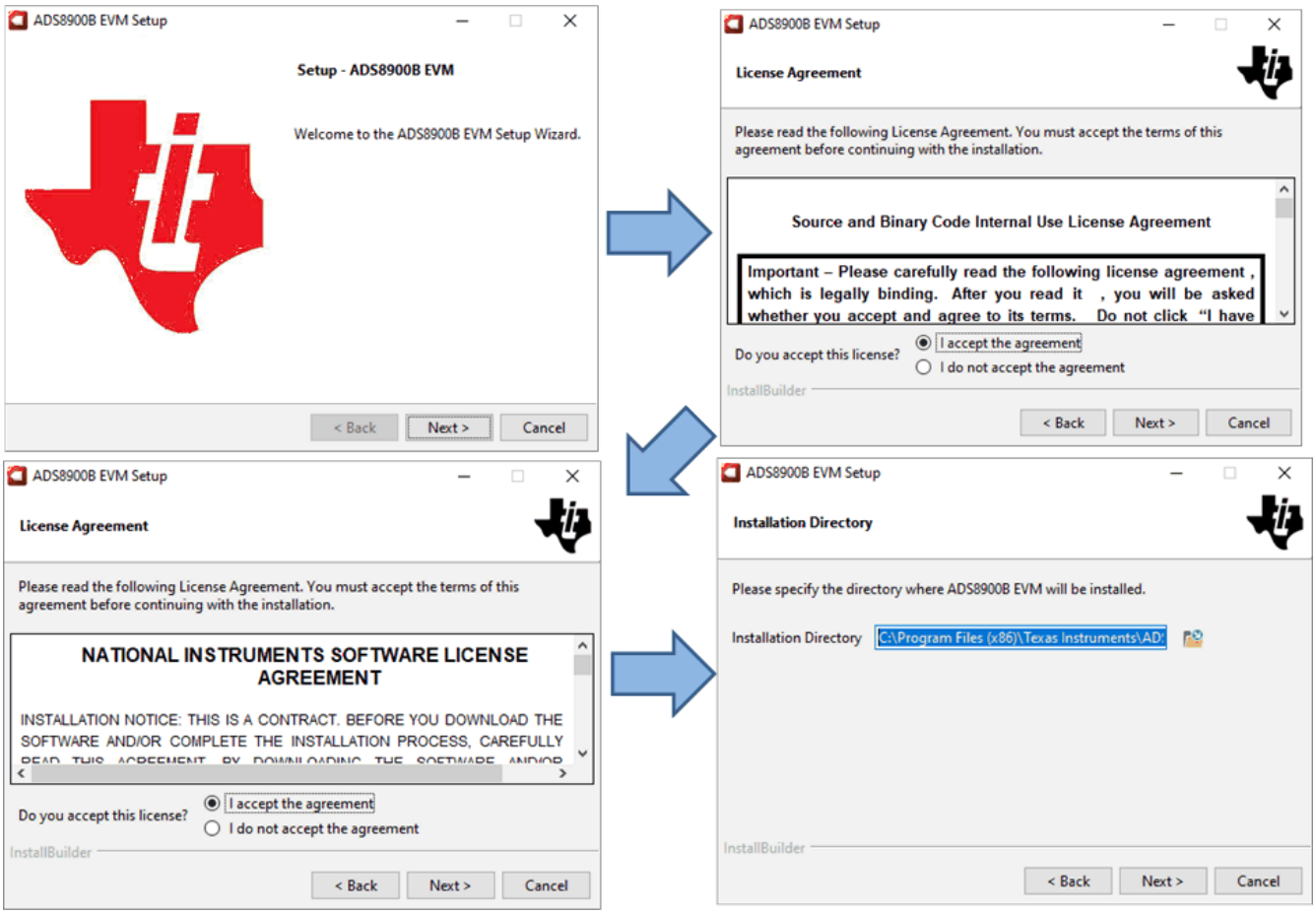


Figure 5-1. ADS8900 Software Installation Prompts

As a part of the ADS8900 EVM GUI installation, a prompt with a *Device Driver Installation* (as shown in Figure 5-2) appears on the screen. Click *Next* to proceed.

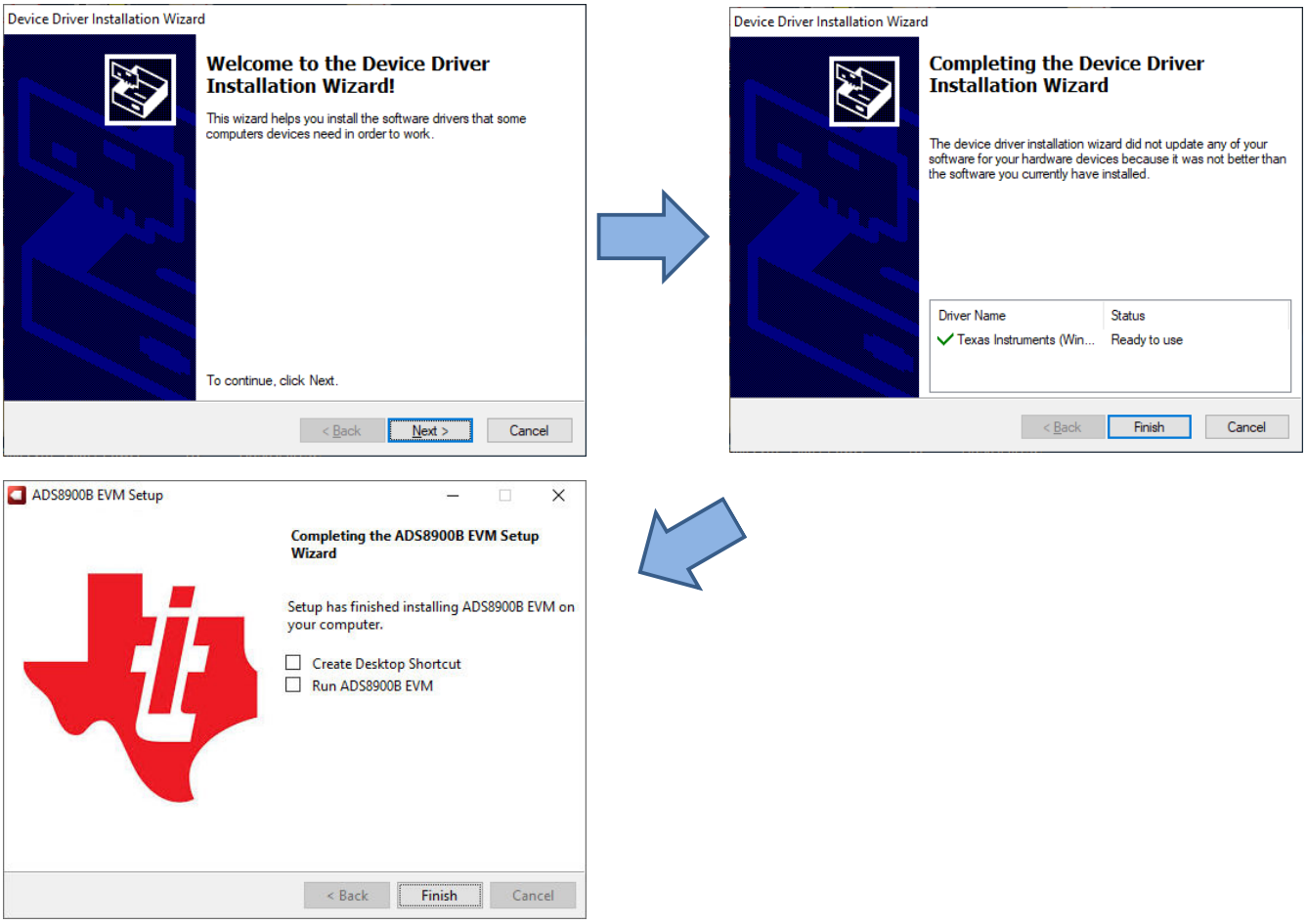


Figure 5-2. Device Driver Installation Wizard Prompts

Note

A notice may appear on the screen stating that Windows cannot verify the publisher of this driver software. Select *Install this driver software anyway*.

The ADS8900BEVM-PDK requires the LabVIEW™ run-time engine and may prompt for the installation of this software, if not already installed. Figure 5-3 shows the installation steps.

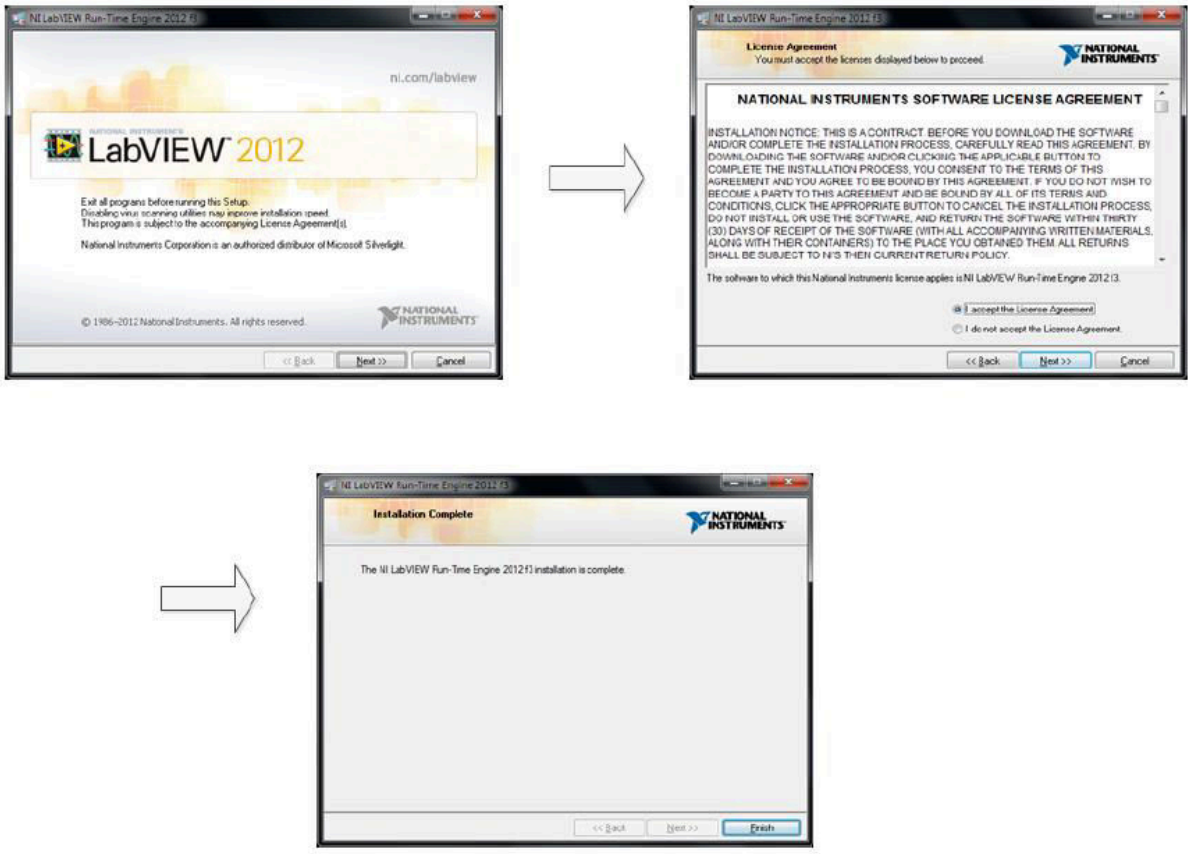


Figure 5-3. LabVIEW™ Run-Time Engine Installation

After these installations, verify that *C:\Program Files (x86)\Texas Instruments\ADS8900 EVM* is as shown in Figure 5-4.

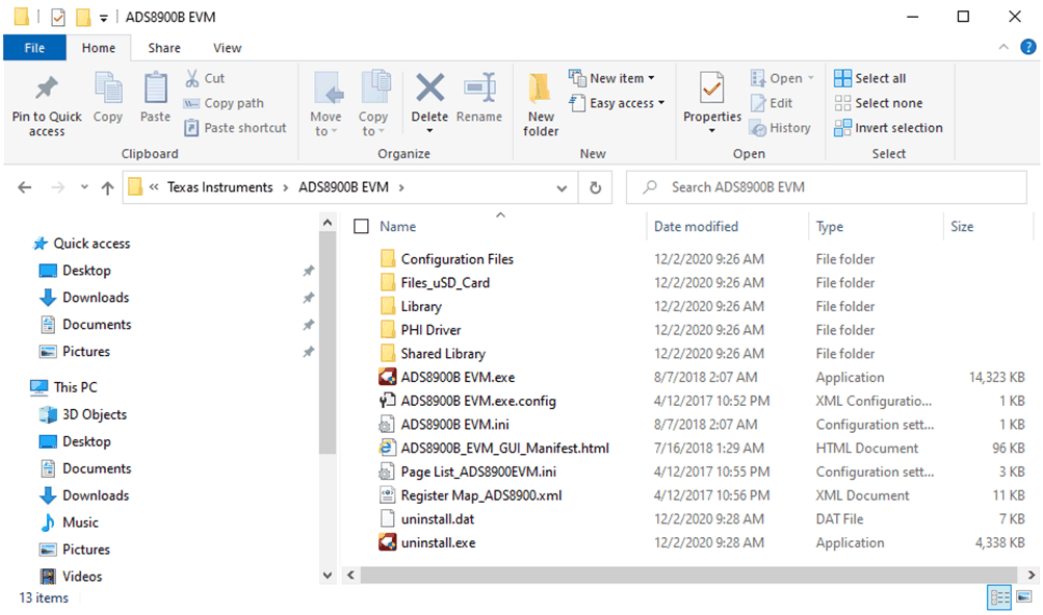


Figure 5-4. ADS8900 EVM Folder Post-Installation

5.2 Default Jumper Settings for Differential Inputs

The EVM can be jumper configured for both differential and single-ended inputs. The jumpers also impact the common-mode (offset) requirements for the input signal. Some jumpers are only used in unusual circumstances, and are normally configured as described in this section. Table 5-1 provides jumper configurations for differential inputs. Figure 5-5 shows the input full-scale signals and the ADC output.

Table 5-1. Jumper Configuration for Fully Differential Input

Jumper	Default Setting	Purpose
JP1	Removed	When installed, this jumper forces input J2 to GND or VCM. This jumper is not installed for differential inputs but is installed for single-ended inputs.
JP2	Removed	When installed, this jumper forces input J3 to GND or VCM. This jumper is not installed for differential inputs but can be installed for single-ended inputs.
JP3	2.6-V position	Both the 2.5-V and 2.6-V position can be used for a fully differential input signal. The 2.6-V position shifts the signal from GND by 0.1 V to minimize distortion resulting from output swing limitations. This shift works because the amplifier positive supply is set to 5.3 V. The signal out of AINP and AINN ranges from 0.1 V to 5.1 V when the jumper is in the 2.6-V position. The signal out of AINP and AINN ranges from 0 V to 5.0 V when the jumper is in the 2.5-V position.
JP4	GND position	This jumper selects the negative supply voltage. The default board configuration does not include the negative supply, so the –0.2-V position does not work without installing U6 and the associated components.
JP5	Removed	Removing this jumper sets the EEPROM write protect on. The EEPROM is factory programed and does not need to be reprogrammed, so keeping the write protect on is recommended.

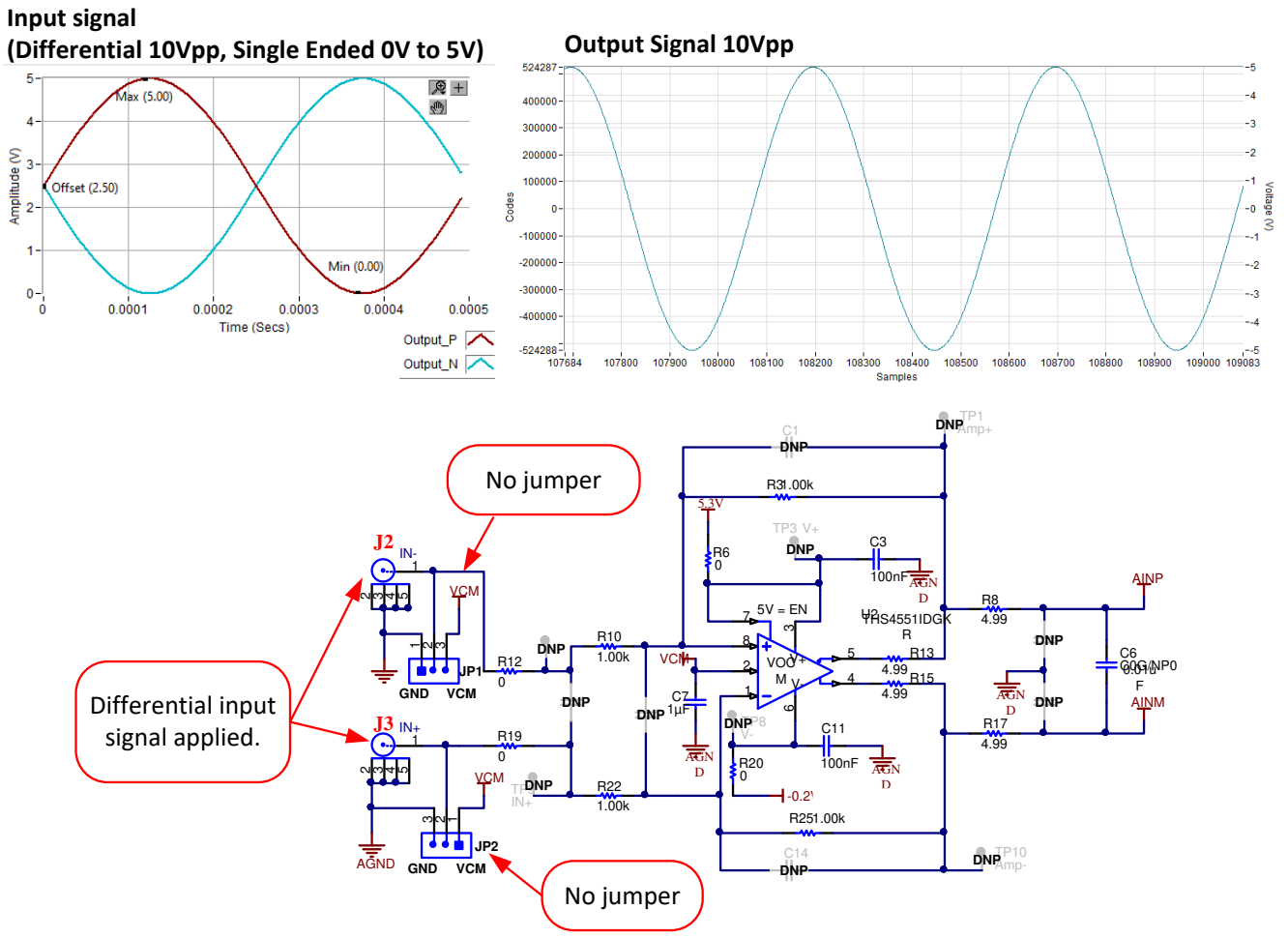


Figure 5-5. Differential Input Signal and Expected ADC Response

5.3 Default Jumpers for Bipolar, Single-Ended Inputs

The EVM can be jumper configured for both differential and single-ended inputs. The jumpers also impact the common-mode (offset) requirements for the input signal. Some jumpers are only used in unusual circumstances, and are normally configured as described in this section. Table 5-2 provides jumper configurations for a bipolar, single-ended input. Figure 5-6 shows the input full-scale signal and the ADC output. The output signal is half full scale.

Table 5-2. Jumper Configurations for Bipolar, Single-Ended Input

Jumper	Default Setting	Purpose
JP1	GND position	When installed in this position, the input J2 is connected to GND. Connect the input J3 to a single-ended input signal with the offset set to 0 V (bipolar input).
JP2	Removed	Leave this jumper unconnected, and apply a single-ended signal with a 0-V offset to connector J3.
JP3	2.6-V position	Both the 2.5-V and 2.6-V position can be used for a fully differential input signal. The 2.6-V position shifts the signal from GND by 0.1 V to minimize distortion resulting from output swing limitations. This shift works because the amplifier positive supply is set to 5.3 V. The signal out of AINP and AINN ranges from 0.1 V to 5.1 V when the jumper is in the 2.6-V position. The signal out of AINP and AINN ranges from 0 V to 5.0 V when the jumper is in the 2.5-V position.
JP4	GND position	This jumper selects the negative supply voltage. The default board configuration does not include the negative supply, so the –0.2-V position does not work without installing U6 and the associated components.
JP5	Removed	Removing this jumper sets the EEPROM write protect on. The EEPROM is factory programed and does not need to be reprogrammed, so keeping the write protect on is recommended.

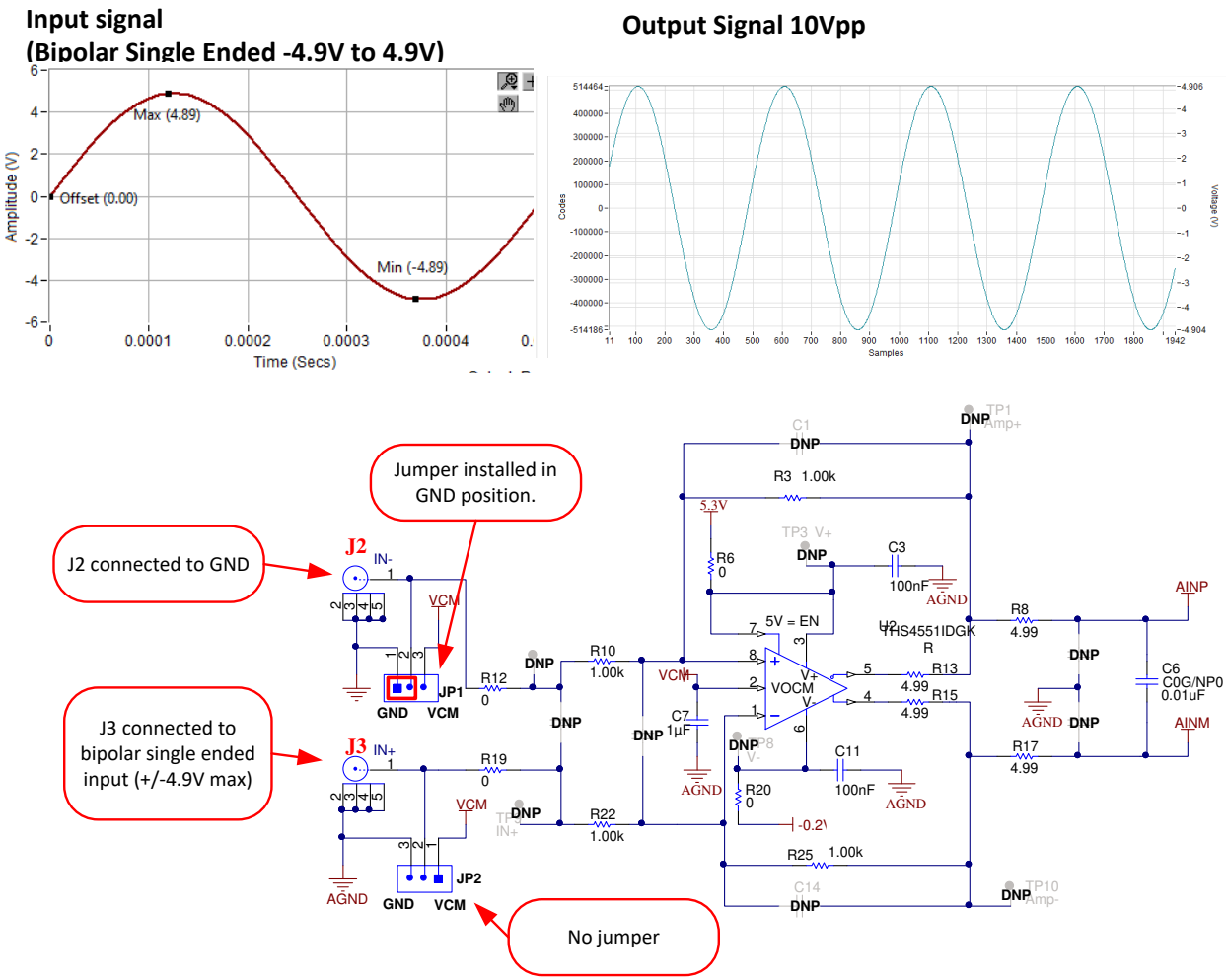


Figure 5-6. Bipolar, Single-Ended, –5.0-V to 5.0-V Input

5.4 Default Jumpers for Unipolar, Single-Ended Inputs

The EVM can be jumper configured for both differential and single-ended inputs. The jumpers also impact the common-mode (offset) requirements for the input signal. Some jumpers are only used in unusual circumstances, and are normally configured as described in this section. Table 5-3 provides jumper configurations for a unipolar, single-ended input. Figure 5-7 shows the input full-scale signal and the ADC output. The output signal is half full scale. To achieve a full-scale output with a single-ended input, the gain of U2 must be adjusted to 2 V/V (change R3 and R25 to 2 kΩ).

Table 5-3. Jumper Configurations for Unipolar, Single-Ended Input

Jumper	Default Setting	Purpose
JP1	VCM position	When installed in this position, the input J2 is connected to VCM. Connect the input J3 to a single-ended input signal with the offset set equal to VCM (2.5 V or 2.6 V depending on JP3) for a unipolar input.
JP2	Removed	Leave this jumper unconnected, and apply a single-ended signal to J3 with offset set equal to VCM (2.5 V or 2.6 V depending on JP3) for a unipolar input.
JP3	2.6-V position	Both the 2.5-V and 2.6-V position can be used for a fully differential input signal. The 2.6-V position shifts the signal from GND by 0.1 V to minimize distortion resulting from output swing limitations. This shift works because the amplifier positive supply is set to 5.3 V. The signal out of AINP and AINN ranges from 0.1 V to 5.1 V when the jumper is in the 2.6-V position. The signal out of AINP and AINN ranges from 0 V to 5.0 V when the jumper is in the 2.5-V position.
JP4	GND position	This jumper selects the negative supply voltage. The default board configuration does not include the negative supply, so the –0.2-V position does not work without installing U6 and the associated components.
JP5	Removed	Removing this jumper sets the EEPROM write protect on. The EEPROM is factory programed and does not need to be reprogrammed, so keeping the write protect on is recommended.

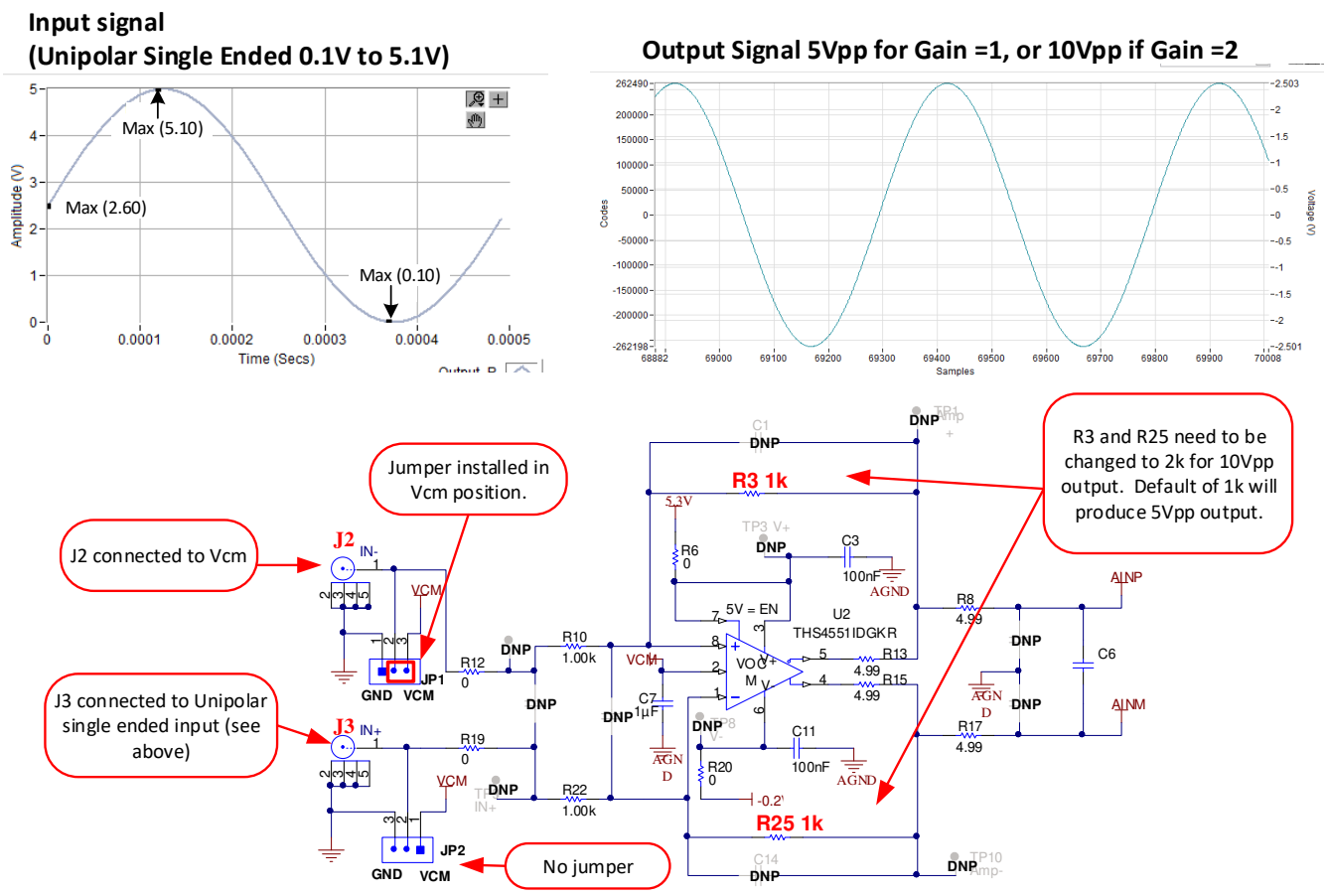


Figure 5-7. Unipolar, Single-Ended, 0-V to 5-V Input

5.5 External Source Requirements for ADS8900 Evaluation

The ADS8900B is a very low-distortion, low-noise ADC. In order to achieve the full specified ADC performance, use a low-distortion, low-noise signal source. Table 5-4 lists the recommended minimum specifications for a signal source that can be used to achieve the specified performance.

Table 5-4. External Source Requirements for ADS8900 Evaluation

Specification Description	Specification Value
Signal frequency	2 kHz
External source type	Balanced differential
External source common-mode	0 V or floating
External source impedance (R_S)	10 Ω–30 Ω
External source differential impedance ($R_{S\_DIFF} = 2 \times R_S$)	20 Ω–60 Ω
Source differential signal (V_{PP} amplitude for –0.1 dBFS)	(2 x Rs x 4.94 x 10-3) + 9.9 V or (RS_DIFF x 4.94 x 10-3) + 9.9 V
Maximum noise	10 μV_{RMS}
Maximum SNR	110 dB
Maximum THD	–130 dB

6 ADS8900EVM-PDK Operation

The following instructions are a step-by-step guide to connecting the ADS8900BEVM-PDK to the computer and evaluating the performance of the ADS8900B:

1. Connect the ADS8900VEVM to the PHI. Install the two screws as indicated in Figure 6-1.
2. Connect the USB on the PHI to the computer first:
   - LED D5 on the PHI lights up, indicating that the PHI is powered up.
   - LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC. Figure 6-1 shows the resulting LED indicators.
3. Start the software GUI as shown in Figure 6-2. Notice that the LEDs blink slowly when the FPGA firmware is loaded on the PHI. This process takes a few seconds and then the AVDD and DVDD power supplies turn on.
4. Connect the signal generators to the SMA inputs. The input range is either a differential 10-V_{PP} or a single-ended 10-V_{PP} range.

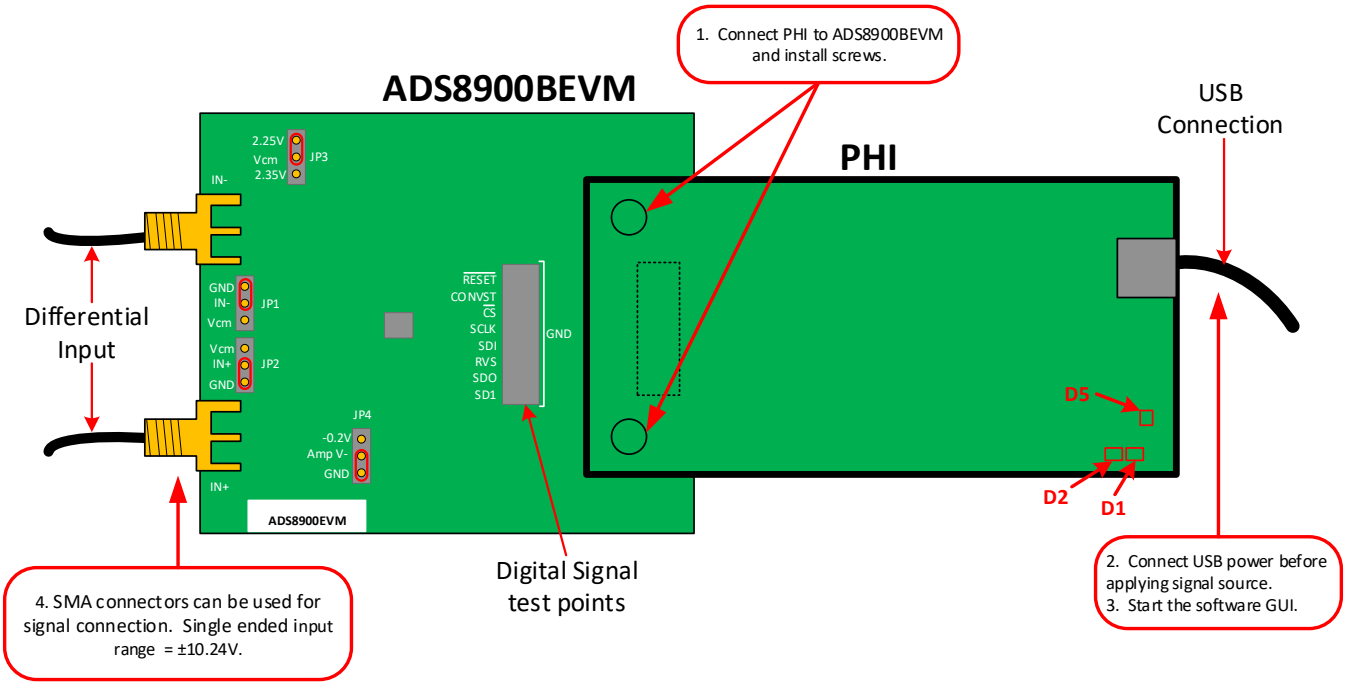


Figure 6-1. ADS8900BEVM Hardware Setup and LED Indicators

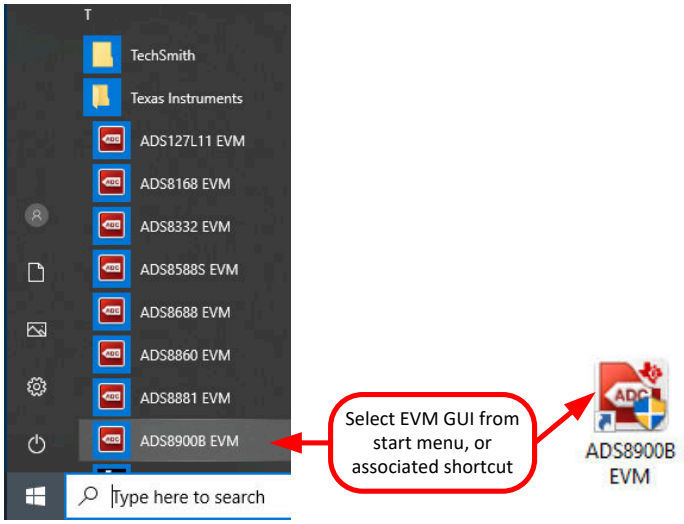


Figure 6-2. Launch the EVM GUI Software

6.1 EVM GUI Global Settings for ADC Control

Although the EVM GUI does not allow direct access to the levels and timing configuration of the ADC digital interface, the EVM GUI does give users high-level control over virtually all functions of the ADS8900, including interface modes, sampling rate, and number of samples to be captured.

Figure 6-3 identifies the input parameters of the GUI (as well as their default values) through which the various functions of the ADS8900 can be exercised. These are global settings as they persist across the GUI tools listed in the top left pane (or from one page to another).

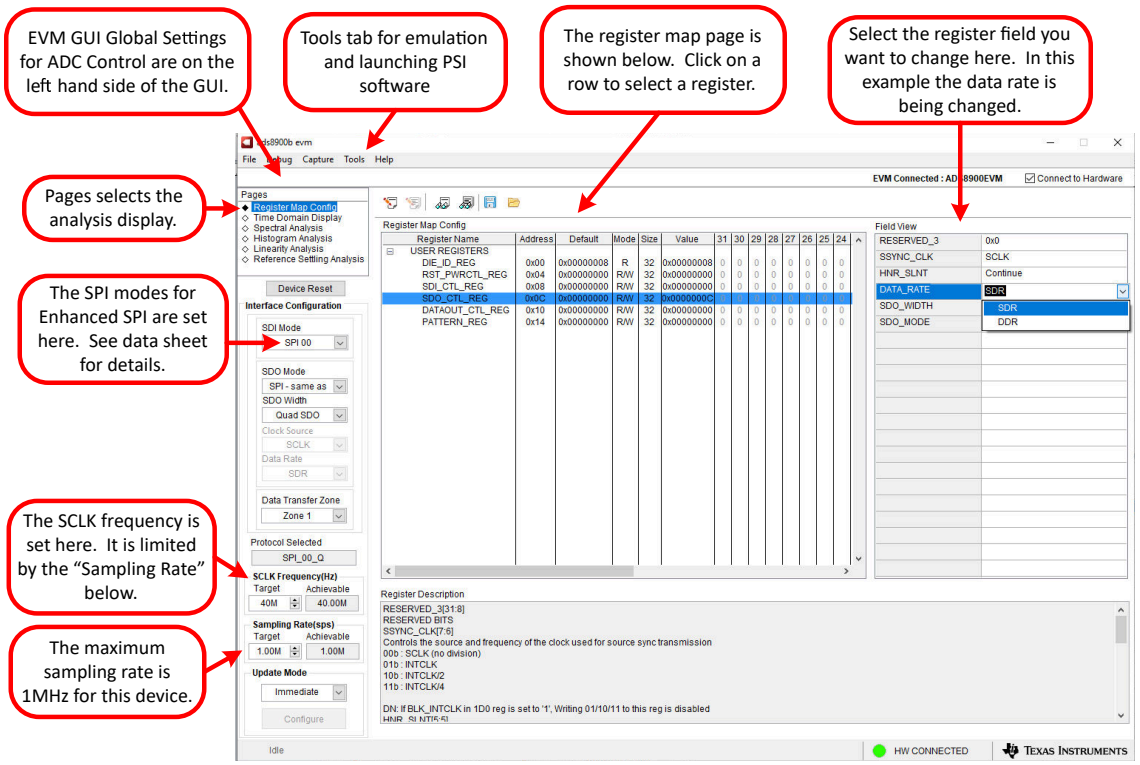


Figure 6-3. EVM GUI Global Input Parameters

The interface configuration options in this pane allow the user to choose from various SPI and multiSPI host interface options available on the ADS8900B. The host always communicates with the ADS8900B using the standard SPI protocol over the single SDI lane, irrespective of the mode selected for data capture.

The drop-down boxes under the interface configuration sub-menu allows the user to select the data capture mode. The SDO Mode drop-down allows selection between single-, dual- and quad-SDO lanes; Data Read between source and system synchronous modes and Output Data Rate between SDR and DDR modes. Detailed descriptions of each of these modes is available in the ADS8900 data sheet.

The user may select *SCLK Frequency* and *Sampling Rate* on this pane, which are dependent on the device mode selected. The GUI allows the user to enter the targeted values for these two parameters and the GUI computes the best values that can be achieved, considering the timing constraints of the selected device mode.

The user may specify a target SCLK frequency (in hertz) and the GUI matches this value as closely as possible by changing the PHI PLL settings and the achievable frequency that may differ from the target value displayed. Similarly, the sampling rate of the ADC can be adjusted by modifying the target *Sampling Rate* argument (also in hertz). The achievable ADC sampling rate may differ from the target value, depending on the applied SCLK frequency and the selected device mode, with the closest match achievable displayed thereafter.

The final option in this pane is the selection for the *Update Mode*. The default value is *Immediate*, which indicates that the interface settings selection made by the user is applied to configure both the host and the ADS8900 instantly. *Manual* indicates that the selection made is applied only when the user finalizes their choices and is ready to configure the device. This process is described in more detail in Section 6.2.

6.2 Register Map Configuration Tool

The register map configuration tool allows the user to view and modify the registers of the ADS8900. This configuration can be selected by clicking on the *Register Map Config* radio button on the *Pages* section of the left pane shown in Figure 6-4. At power up, the values on this page correspond to the reset values of the device registers. The register values can be edited by double clicking the corresponding value field. If interface mode settings are affected by the change in register values, this change is reflected on the left pane immediately. The impact of changes in the register value reflect on the ADS8900 device based on the *Update Mode* selection as described in Section 6.1.

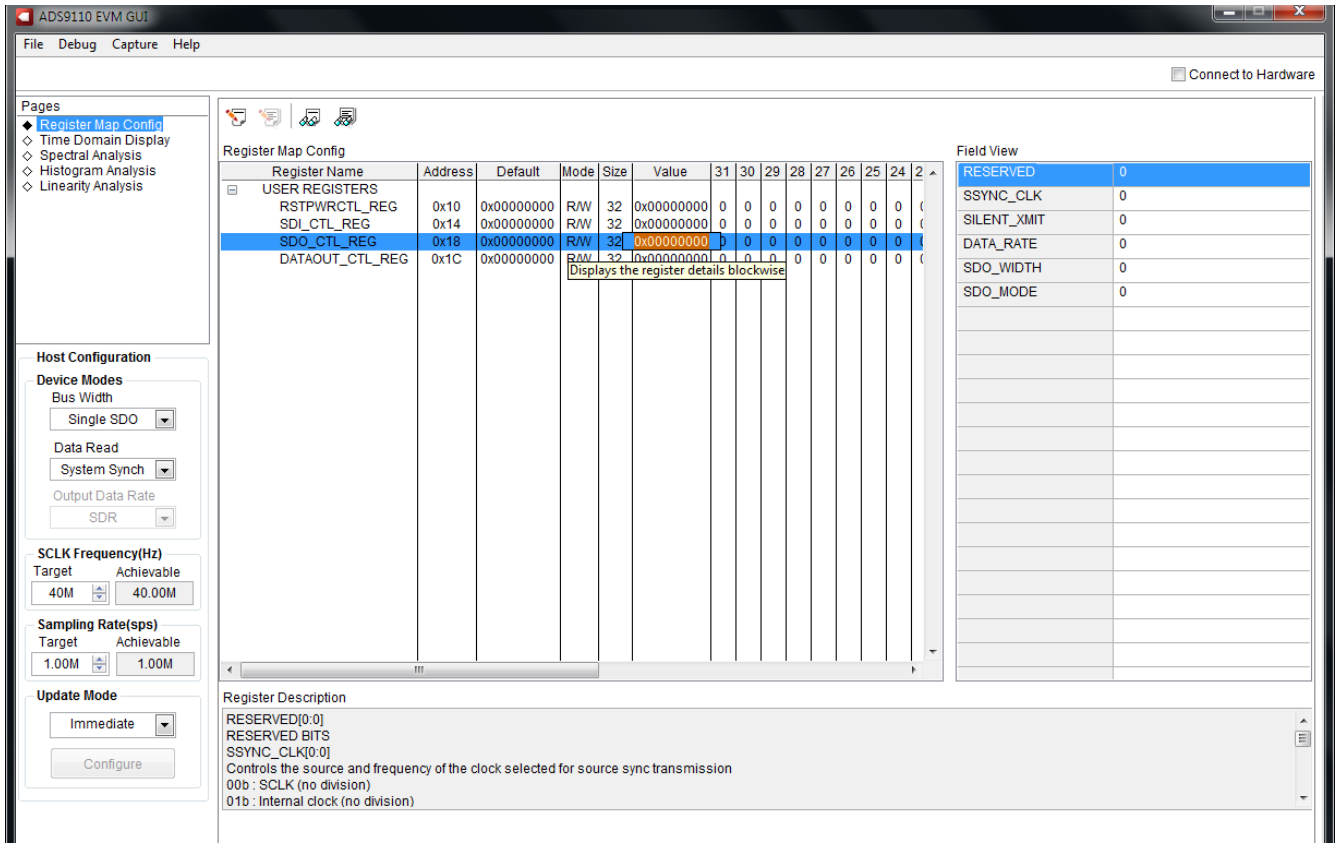


Figure 6-4. Register Map Configuration

Section 6.3 through Section 6.6 describe the data collection and analysis features of the ADS8900EVM-PDK GUI.

6.3 Time Domain Display Tool

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits.

The user can trigger a capture of the data of the selected number of samples from the ADS8900B, as per the current interface mode settings using the *Capture* button, as indicated in Figure 6-5. The sample indices are on the x-axis and there are two y-axes showing the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the analysis tools described in the subsequent sections triggers calculations to be performed on the same set of data.

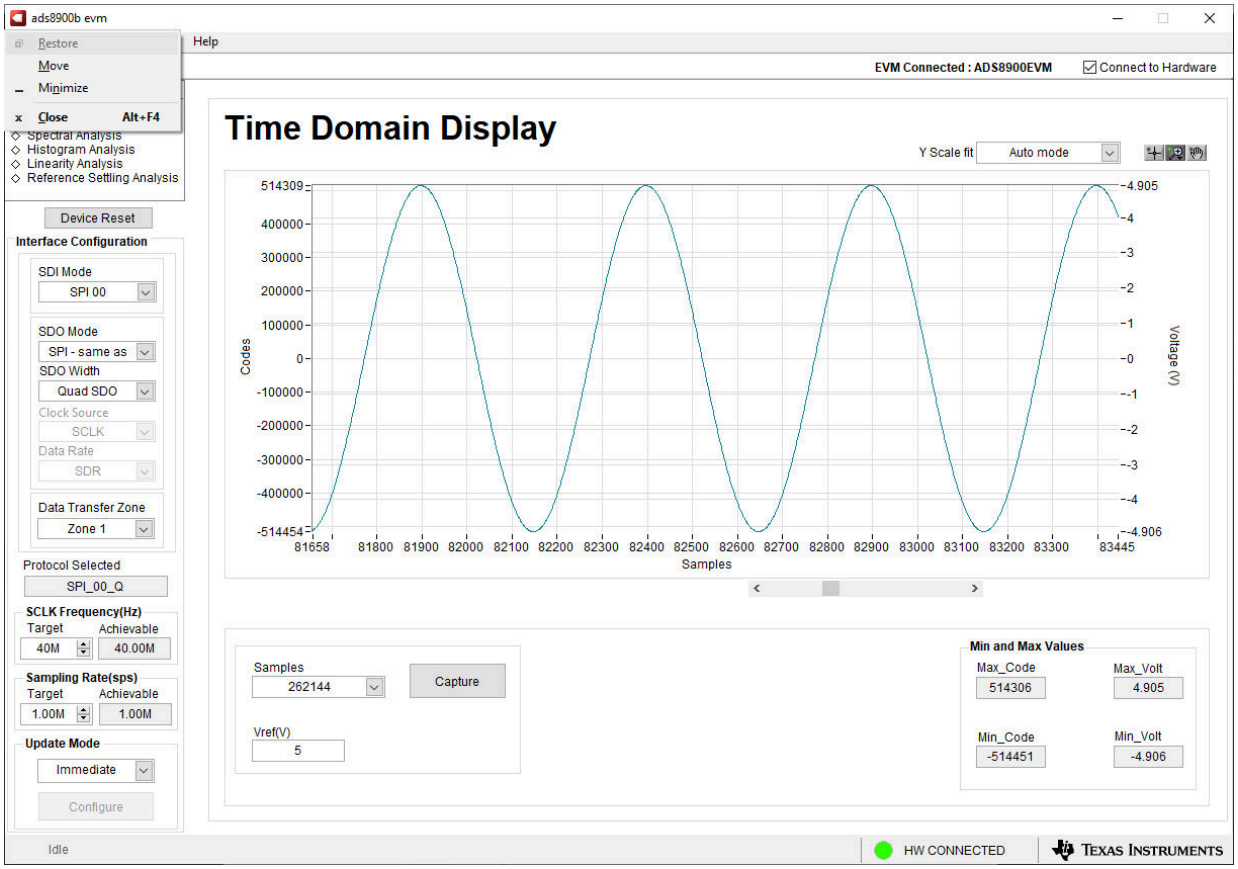


Figure 6-5. Time Domain Display Tool Options

6.4 Spectral Analysis Tool

The spectral analysis tool, shown in Figure 6-6, is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS8900B SAR ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. Also, the window setting of *None* can be used to look for noise spurs over frequency in DC inputs.

For dynamic performance evaluation, the external differential source must have better specifications than the ADC itself to ensure that the measured system performance is not limited by the performance of the signal source. Therefore, the external reference source must meet the source requirements mentioned in Figure 6-6

For 2-kHz SNR and ENOB evaluation at a maximum throughput of 1 MSPS, the number of samples must be 32768 or 65536. Any more samples bring the noise floor so low that the external source phase noise can dominate the SNR and ENOB calculations. However, for THD and SFDR evaluation, a larger number of samples must be used to reduce the noise floor below –140 dBc to analyze noise-free harmonics and spurs in the order of –120 dBc. Such analysis requires at least 262144 samples.

Figure 6-6. Spectral Analysis Tool

Note

The PSIEVM is often used to produce a single-tone sinusoidal signal. As shown in Figure 6-7, this GUI allows the PSIEVM software to be launched directly by clicking on *Tools* and then *Lauch PSI*.

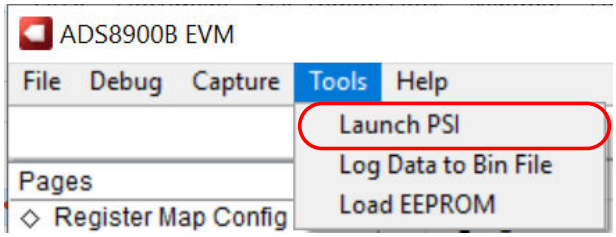


Figure 6-7. Launch PSI

6.5 Histogram Tool

Noise degrades ADC resolution, but the histogram tool (shown in Figure 6-8) can be used to estimate the *effective resolution*. This resolution is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel.

The histogram corresponding to a dc input is displayed on clicking on the *Capture* button, as shown in Figure 6-8.

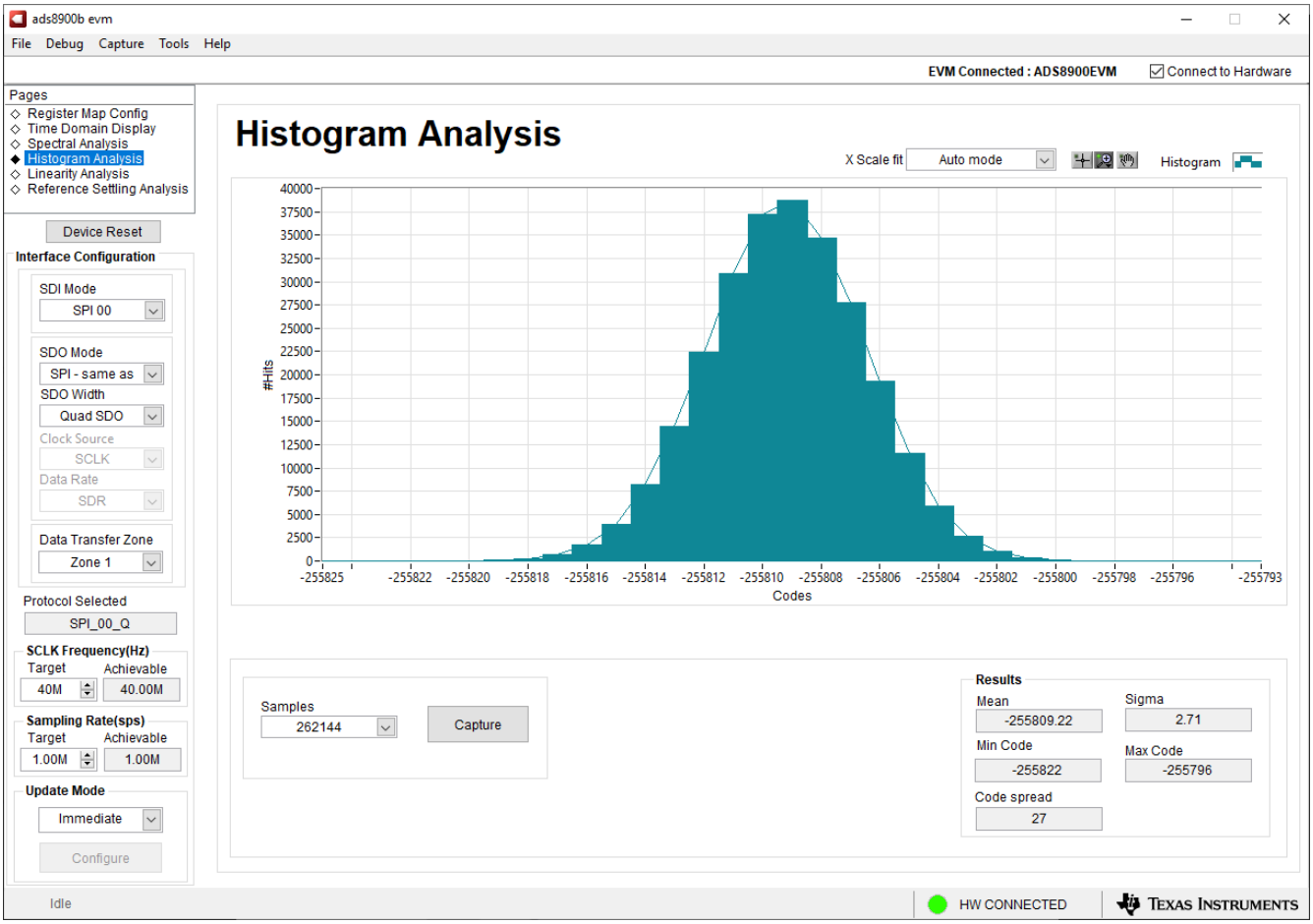


Figure 6-8. Histogram Analysis Tool

6.6 Linearity Analysis Tool

The linearity analysis tool (shown in Figure 6-9) measures and generates the DNL and INL plots over code for the specific ADS8900 installed in the evaluation board. This tool requires a 2-kHz sinusoidal input signal, which is slightly saturated (35 mV outside the full-scale range at each input or 0.13 dBFS) with very low distortion. The external source linearity must be better than the ADC linearity to ensure that the measured system performance reflects the linearity errors of the ADC and is not limited by the performance of the signal source. To make sure that the DNL and INL of the ADC are correctly measured, the external source must meet the requirements in Section 5.5.

CAUTION

This tool requires a negative supply on the THS4551 driver amplifier (U2). The easiest way to provide the negative supply is to install the negative charge pump LM7705 (U6). Also install the output filter capacitors and resistor associated with this charge pump (C31, C32, C33, C34, C35, C36, and R41).

The number-of-hits setting depends on the external noise source. For a 110-dB SNR external source with approximately 10 µVrms of noise, the total number of hits must be 512. For a source with 100-dB SNR, the recommended number of hits is 1024.

Note

This analysis can take a couple of minutes to run and the evaluation board must remain undisturbed during the complete duration of the analysis.

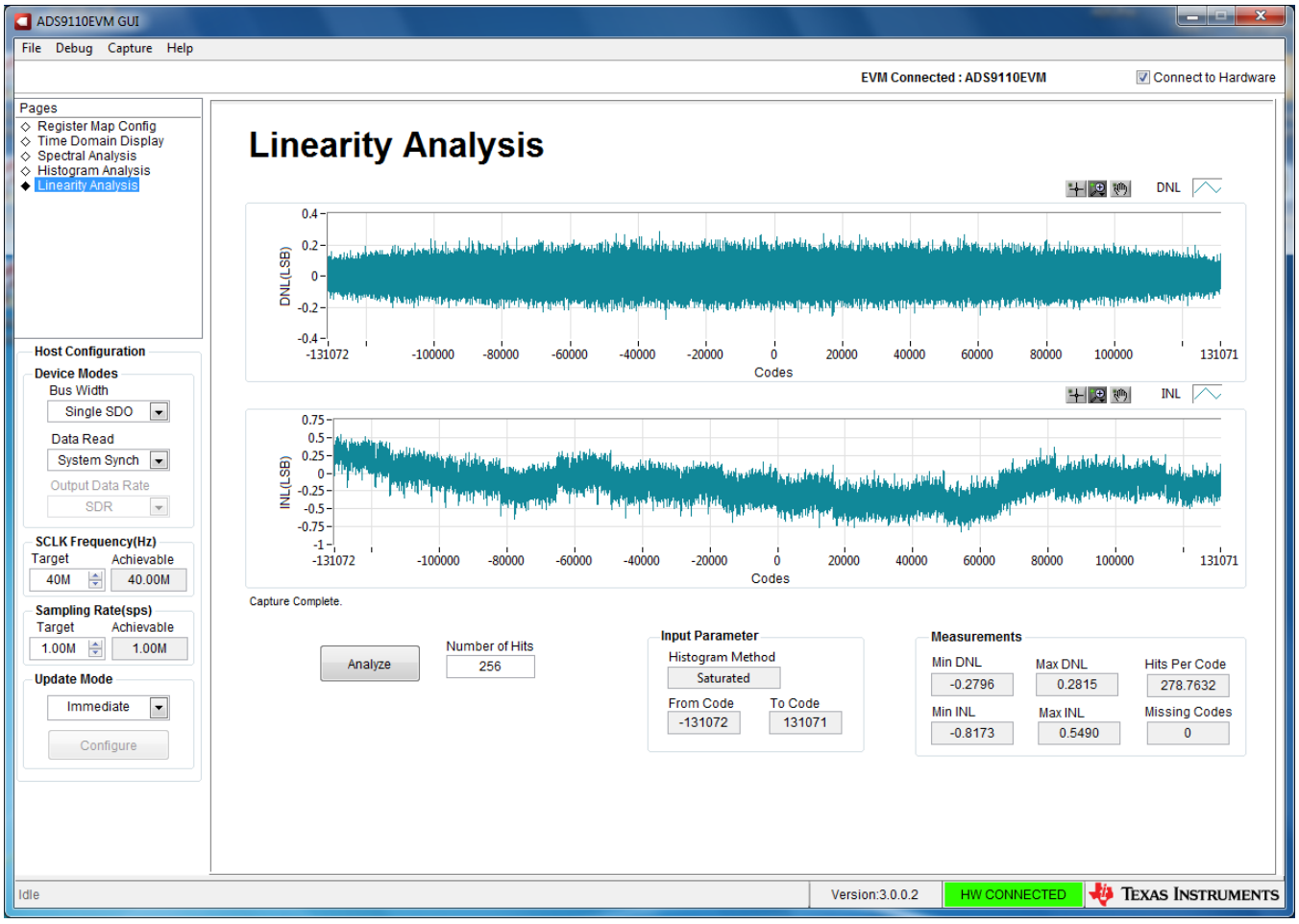


Figure 6-9. Linearity Analysis Tool

6.7 ADS8900BEVM Support for ADS8910B and ADS8920B Devices

This software also allows for the direct evaluation of the ADS8910B (18-bit) and ADS8920B (16-bit) devices by emulating their operation with the ADS8900B (20-bit) device. Update the EEPROM file for either the ADS8910B or the ADS8920B in order for the GUI to operate in these modes. First, install a jumper on JP5 so the EEPROM properly updates. If a jumper is not applied across JP5, an error message appears and the EEPROM does not load. Click on the *Load EEPROM* option in the *Tools* tab at the top of the GUI window and (as shown in Figure 6-10) a separate window appears, asking for a device to be selected. After loading the new EEPROM file, the ADS8910B or ADS8920B can now be evaluated using the ADS8900B.

Because the ADS8900B has a resolution of 20 bits, emulating a device with a lower resolution results in the software clocking out the number of bits of the device being emulated. For example, if the ADS8920B (which has a resolution of 16 bits) is being emulated, the software discards the last four LSBs and only clocks out 16 bits of data. When a device with a lower resolution is being emulated, the AC performance characteristics (such as SNR and THD) match the lower resolution devices.

Note

When running an emulation for the ADS8910B or ADS8920B using an ADS8900B, source synchronous mode cannot be used. Source synchronous mode is enabled by setting SDO mode to multiSPI. If source synchronous mode is selected when emulating a device, an error occurs and the software enters a nonworking state. A power cycle and software reset is required to recover functionality.

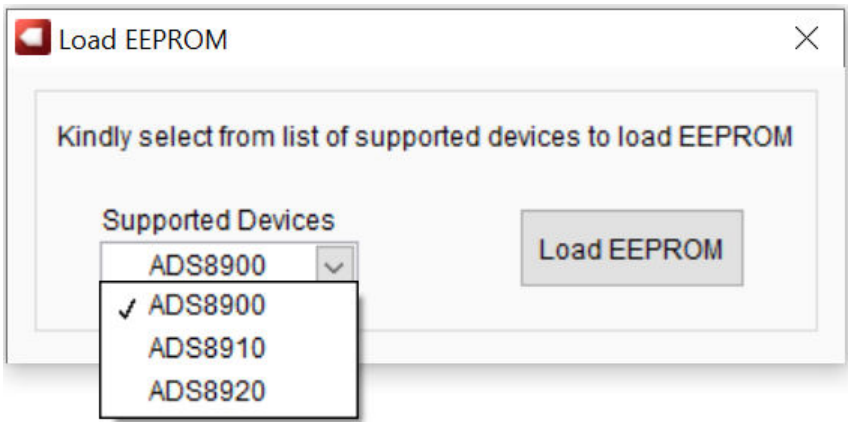


Figure 6-10. Load EEPROM

For direct evaluation of the ADS8910B or ADS8920B, replace the ADS8900B with an ADS8910B or ADS8920B. After loading the correct EEPROM file, the EVM hardware and software properly communicates with the updated device. With a direct device replacement on the ADS8900BEVM, source synchronous mode can be used.

7 Bill of Materials, PCB Layout, and Schematics

This section provides the bill of materials (BOM), printed circuit board (PCB) layout, and schematics for the ADS8900BEVM.

7.1 Bill of Materials (BOM)

Table 7-1 lists the ADS8900EVM BOM.

Table 7-1. Bill of Materials

Designator	Qty	Value	Description	Part Number	Manufacturer
C1, C9, C14	3	1000pF	CAP, CERM, 1000 pF, 25 V,+/- 1%, C0G/NP0, 0603	C0603C102F3GACTU	Kemet
C2, C5, C7, C17, C18, C20, C21, C27	8	1uF	CAP, CERM, 1 µF, 16 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	CGA3E1X7R1C105K080AC	TDK
C3, C11, C19, C23, C25, C38, C39	7	0.1uF	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X7R, 0603	C0603X104K3RACTU	Kemet
C6	1	0.01uF	CAP, CERM, 0.01 µF, 25 V,+/- 1%, C0G/NP0, 0603	C0603C103F3GACTU	Kemet
C8	1	0.01uF	CAP, CERM, 0.01 µF, 50 V,+/- 1%, C0G/NP0, 0805	GRM2195C1H103FA01D	MuRata
C12	1	22uF	CAP, CERM, 22 µF, 10 V, +/- 20%, X7S, 0805	C2012X7S1A226M125AC	TDK
C13, C15, C16, C22, C24	5	10uF	CAP, CERM, 10 uF, 10 V, +/- 10%, X7R, 0805	GCM21BR71A106KE22L	MuRata
C26, C28	2	47uF	CAP, CERM, 47 uF, 25 V, +/- 20%, X5R, 1206_190	C3216X5R1E476M160AC	TDK
D1	1	Green	LED, Green, SMD	APT2012LZGCK	Kingbright
H1– H4	4		MACHINE SCREW PAN PHILLIPS 4-40	PMSSS 440 0025 PH	B&F Fastener Supply
H5	1		CABLE USB A MALE-B MICRO MALE 1M (Kit Item - Include with assembled board)	102-1092-BL-00100	CNC Tech
H6– H9	4		3/16 Hex Female Standoff	1891	Keystone
H10, H11	2		Machine Screw Pan PHILLIPS M3	RM3X4MM 2701	APM HEXSEAL
H12, H13	2		ROUND STANDOFF M3 STEEL 5MM	9774050360R	Wurth Elektronik
H14	1		PHI-EVM Controller Kitting Item Edge #6591636 (Kit Item - Include with assembled board)	PA007	Used in BOM report
J1	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	QTH-030-01-L-D-A	Samtec
J2, J3	2		Connector, End launch SMA, 50 ohm, SMT	142-0701-801	Cinch Connectivity
J4	1		Header, 100mil, 8x2, Gold, TH	TSW-108-07-G-D	Samtec
JP1– JP4	4		Header, 100mil, 3x1, Gold, SMT	TSM-103-01-L-SV	Samtec
JP5	1		Header, 2.54 mm, 2x1, Gold, R/A, SMT	878980204	Molex
R1, R49, R50	3	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	RC0603FR-0710KL	Yageo

Table 7-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Part Number	Manufacturer
R2, R4–R7, R9, R11, R12, R14, R18–R21, R23, R24, R26, R28, R38, R42, R46–R48	22	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3GEY0R00V	Panasonic
R3, R10, R22, R25	4	1.00k	RES, 1.00 k, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0603	ERA3AEB102V	Panasonic
R8, R13, R15, R17	4	4.99	RES, 4.99, 1%, 0.1 W, 0603	RC0603FR-074R99L	Yageo
R16	1	1.00	RES, 1.00, 1%, 0.1 W, 0603	RC0603FR-071RL	Yageo
R27, R33	2	100	RES, 100, 1%, 0.1 W, 0603	RC0603FR-07100RL	Yageo
R29, R34	2	0	RES, 0, 5%, 0.1 W, 0603	RC0603JR-070RL	Yageo
R30, R35, R37	3	20.0k	RES, 20.0 k, 0.1%, 0.1 W, 0603	RG1608P-203-B-T5	Susumu Co Ltd
R31	1	215k	RES, 215 k, 1%, 0.1 W, 0603	RC0603FR-07215KL	Yageo
R32	1	499	RES, 499, 0.1%, 0.1 W, 0603	RG1608P-4990-B-T5	Susumu Co Ltd
R36	1	0.22	RES, 0.22, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3RQFR22V	Panasonic
R39	1	0.1	RES, 0.1, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3RSFR10V	Panasonic
SH-J1, SH-J2	2	1x2	Shunt, 100mil, Flash Gold, Black	SPC02SYAN	Sullins Connector Solutions
TP11–TP13, TP15	4		Test Point, Compact, SMT	5016	Keystone
TP14, TP16	2		Test Point, Miniature, SMT	5015	Keystone
U1	1		20-Bit, 1-MSPS, SAR ADC with Internal Reference Buffer, Internal LDO & multiSPI(TM) Digital Interface, RGE0024H (VQFN-24)	ADS8900BRGER	Texas Instruments
U2	1		Low Noise, Precision, 150MHz, Fully Differential Amplifier, DGK0008A (VSSOP-8)	THS4551IDGKR	Texas Instruments
U3	1		3 µVpp/V Noise, 3 ppm/°C Drift Precision Series Voltage Reference, DGK0008A (VSSOP-8)	REF5050AIDGKT	Texas Instruments
U4	1		Precision, Low Noise, Low Iq Operational Amplifier, 2.2 to 5.5 V, -40 to 125 degC, 5-pin SOT23 (DBV5), Green (RoHS & no Sb/Br)	OPA376AIDBVT	Texas Instruments
U5	1		36V, 1A, 4.17µVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)	TPS7A4700RGWR	Texas Instruments
U7	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	BR24G32FVT-3AGE2	Rohm
C4, C10	0	1000pF	CAP, CERM, 1000 pF, 25 V,+/- 1%, C0G/NP0, 0603	C0603C102F3GACTU	Kemet

Table 7-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Part Number	Manufacturer
C29	0	0.22uF	CAP, CERM, 0.22 uF, 25 V, +/- 5%, X7R, 0603	C0603C224J3RAC7867	Kemet
C30	0	4.7uF	CAP, CERM, 4.7 uF, 16 V, +/- 10%, X5R, 0805	EMK212BJ475KG-T	Taiyo Yuden
C31, C35	0	22uF	CAP, CERM, 22 uF, 10 V, +/- 20%, X7S, 0805	C2012X7S1A226M125AC	TDK
C32	0	0.47uF	CAP, CERM, 0.47 uF, 35 V, +/- 10%, X5R, 0805	GMK212BJ474KG-T	Taiyo Yuden
C33, C34, C37	0	10uF	CAP, CERM, 10 uF, 10 V, +/- 10%, X7T, 0603	ZRB18AD71A106KE01L	MuRata
C36	0	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0603	C0603X104K3RACTU	Kemet
FID1–FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A
R40	0	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	RC0603FR-0710KL	Yageo
R41	0	4.7	RES, 4.7, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	ERJ-6GEYJ4R7V	Panasonic
R43, R44	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3GEY0R00V	Panasonic
R45	0	0.22	RES, 0.22, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3RQFR22V	Panasonic
TP1, TP5, TP9, TP10	0		Test Point, Miniature, Yellow, TH	5004	Keystone
TP3	0		Test Point, Miniature, Red, TH	5000	Keystone
TP8	0		Test Point, Miniature, Black, TH	5001	Keystone
U6	0		Low Noise Negative Bias Generator, 8-pin Mini SOIC, Pb-Free	LM7705MM/NOPB	Texas Instruments

7.2 PCB Layout

Figure 7-1 shows the EVM PCB layout.

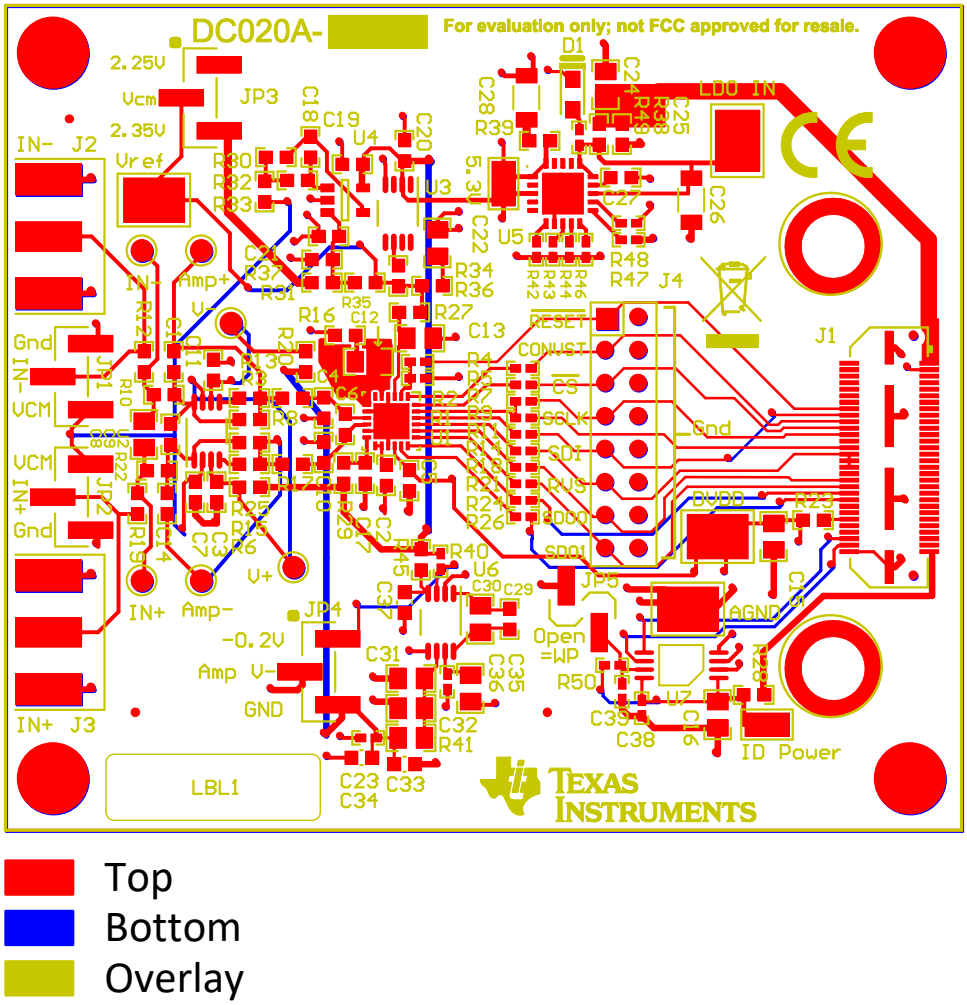


Figure 7-1. ADS8900EVM PCB Layout

7.3 Schematics

Figure 7-2 through Figure 7-3 illustrate the EVM schematics.

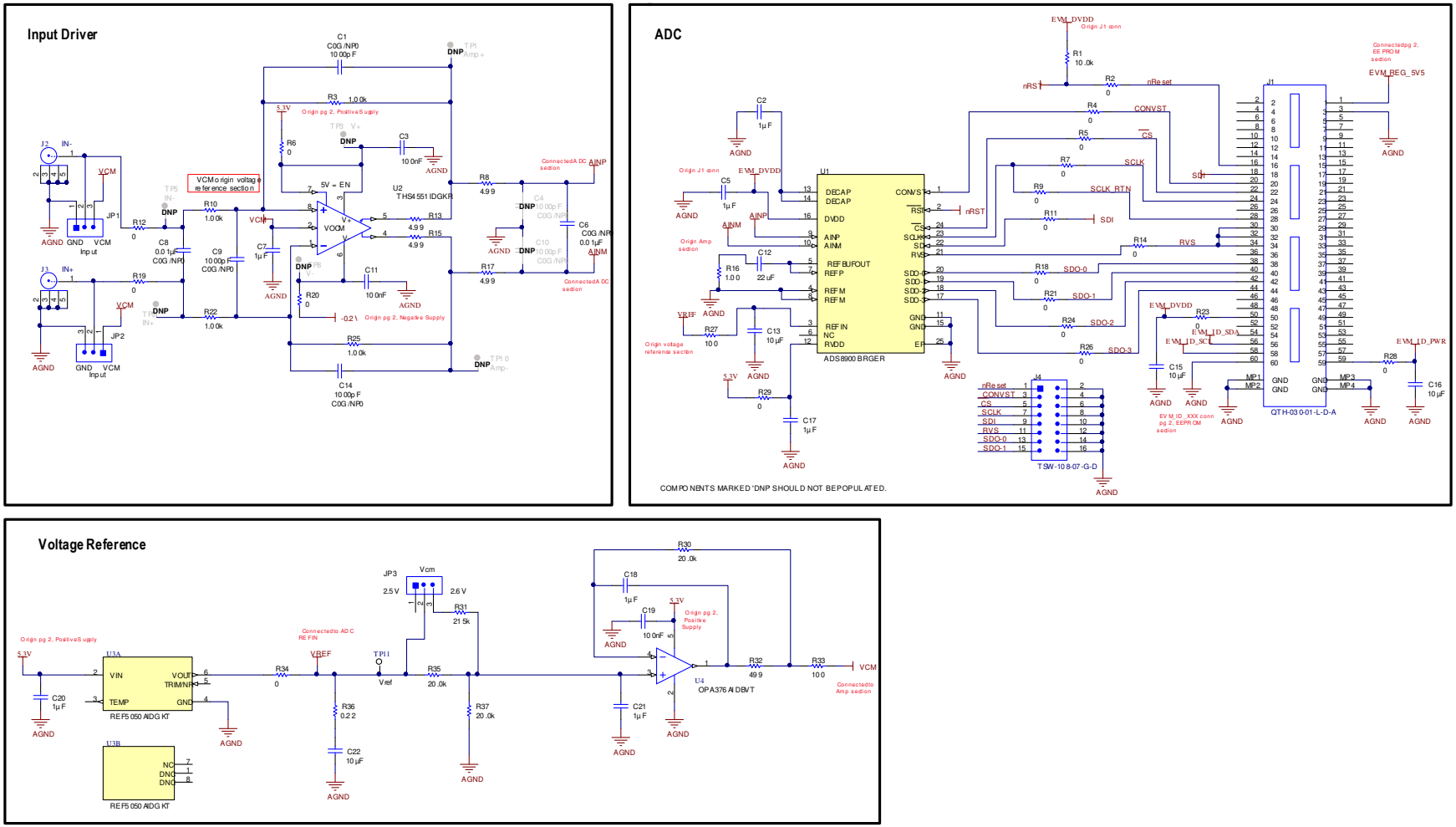
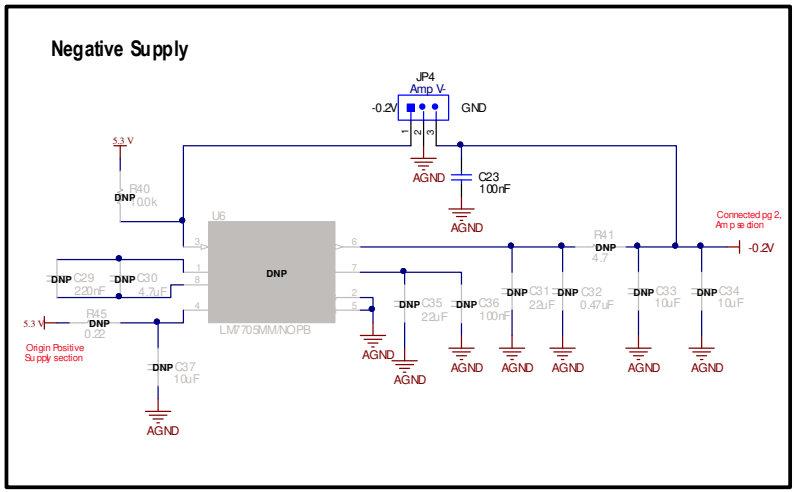
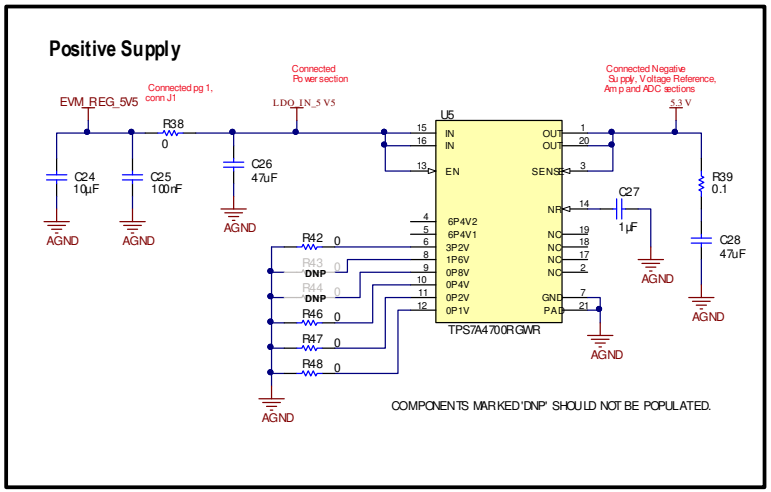
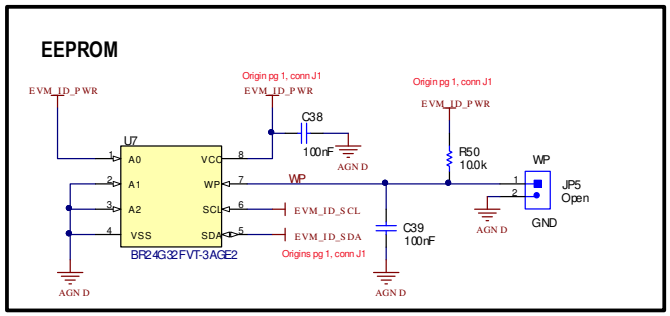


Figure 7-2. Schematic Diagram (Page 1) of the ADS8900EVM PCB







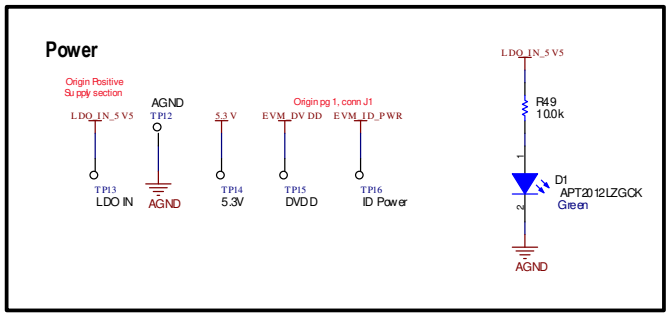


Figure 7-3. Schematic Diagram (Page 2) of the ADS8900EVM PCB

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2021) to Revision C (August 2021)	Page
• Moved *Related Documentation* table to *EVM Overview* section	3
• Added discussion of ADS8910 and ADS8920 ADC to first bullet of *ADS8900EVM-PDK Kit Features* section	3
• Added tools tab information to *EVM GUI Global Input Parameters* figure	18
• Added note and *Launch PSI* figure to *Spectral Analysis Tool* section	21
• Added *ADS8900BEVM Support for ADS8910B and ADS8920B Devices* section	25

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