DAC8775EVM User's Guide

This user's guide describes the characteristics and use of the DAC8775 evaluation board (EVM). It also discusses how to setup and configure the software and hardware for proper operation. Throughout this document, the terms DAC8775EVM, evaluation board, evaluation module, and EVM are synonymous with the DAC8775EVM.

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Trademarks

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1 Overview

The DAC8775 is a four-channel (quad) 16-bit precision digital-to-analog converter (DAC). Each output can be configured to produce a current in output ranges of 0 to 20 mA, 0 to 24 mA, 3.5 to 23.5 mA, or ±24 mA. Each channel can also be configured for voltage output in ranges of 0 to 5 V, 0 to 6 V, 0 to 10 V, 0 to 12 V, ±5 V, ±6 V, ±10 V, or ±12 V. The DAC8775 includes integrated buck-boost converters for each channel to generate all necessary power supplies from a single external supply. The buck-boost converter features various operating modes that can be used to enhance power dissipation and thermal performance. The DAC8775 features additional peripherals including: HART input pins for coupling of FSK HART Voltage signals, slew-rate control for the analog outputs, and reliability features such as CRC, watchdog timer, and conditional alarms.

1.1 EVM Kit Contents

Table 1 details the contents of the EVM kit. Contact the nearest Texas Instruments Product Information Center or visit the Texas Instruments E2E Community (http://E2E.ti.com) if any component is missing.

Table 1. Contents of DAC8775EVM Kit

ITEM NO	ITEM	QTY	DESCRIPTION OR USE
1	DAC8775EVM PCB	1	EVM hardware
2	USB Extension Cable	1	Connects PC USB port to SM-USB-DIG USB connector
3	SM-USB-DIG Platform	1	Platform used for digital communication from PC to EVM

1.2 Related Documentation From Texas Instruments

The following documents provide information regarding Texas Instruments integrated circuits used in the assembly of the DAC8775EVM. This user's guide is available from the TI website under the literature number SBAU248. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions may be available from the TI website at http://www.ti.com/, or by calling the Texas Instruments Literature Response Center at 1-800-477-8924 or the Product Information Center at 1-972-644-5580. When ordering identify the document by both title and literature number.

Table 2. Related Documentation

ITEM NO	LITERATURE NUMBER
DAC8775 product data sheet	SLVSBY7
REF5050 product data sheet	SBOS410
SM-USB-DIG platform user's guide	SBOU098

2 EVM Hardware Overview

This section discusses the overall system setup for the EVM. A personal computer (PC) runs the software that communicates with the SM-USB-DIG platform, which provides the power and digital signals used to communicate with the EVM board. Connectors on the EVM board allow the user to connect the required external power supplies for the configuration under test. The SM-USB-DIG must be connected to the DAC8775EVM with the Texas Instruments logo facing up.

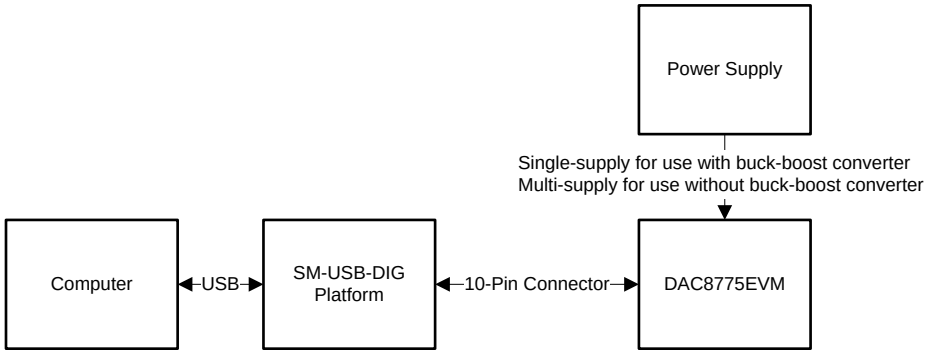

Figure 1. DAC8775EVM Hardware Setup

2.1 EVM Board Block Diagram

A block diagram of the EVM board setup is shown in Figure 2. This board provides test points for the SPI, power, reference, ground, analog outputs, !LDAC, CLR, ALARM, and RESET signals. The EVM allows the user to select the internal buck-boost converter or external power supplies as sources for each channel's positive and negative supplies rails. The EVM also allows the user to select the internal reference, onboard REF5050 reference, or external reference to provide the reference voltage to the DAC8775.

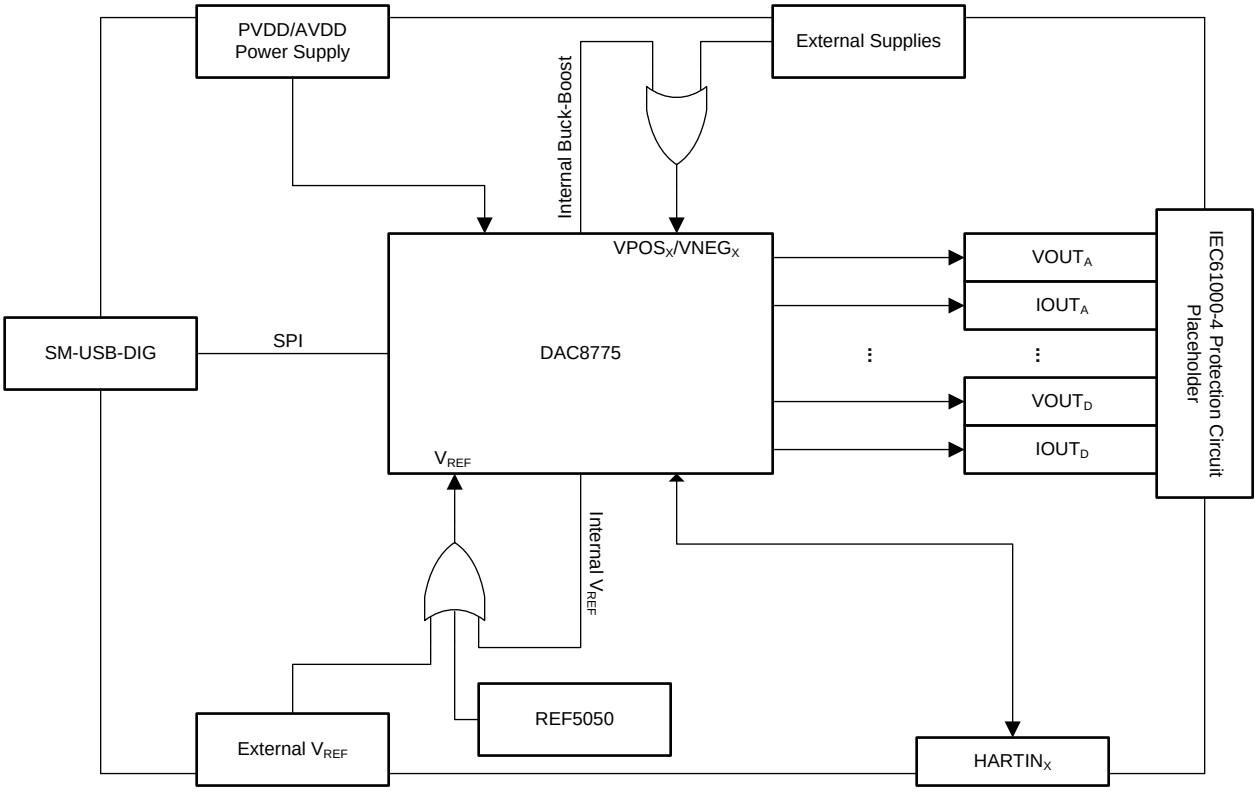

Figure 2. DAC8775EVM Block Diagram

2.2 Electrostatic Discharge Warning

Many of the components on the EVM are susceptible to damage by electrostatic discharge (ESD). Users are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

2.3 Jumper Summary

Table 3 summarizes all of the EVM jumper functionality.

Table 3. EVM Jumper Summary

JUMPER LABEL	DEFAULT	POSITION	FUNCTION
JP1	1-2	1-2	Selects DC/DC Channel A to supply VPOSA
		2-3	Selects PVDD/AVDD to supply VPOSA
JP2	1-2	1-2	Selects DC/DC Channel A to supply VNEGA
		2-3	Selects AVSS to supply VNEGA
JP3	1-2	1-2	Selects DC/DC Channel B to supply VPOSB
		2-3	Selects PVDD/AVDD to supply VPOSB
JP4	1-2	1-2	Selects DC/DC Channel B to supply VNEGB
		2-3	Selects AVSS to supply VNEGB
JP5	1-2	1-2	Selects DC/DC Channel C to supply VPOSC
		2-3	Selects PVDD/AVDD to supply VPOSC
JP6	1-2	1-2	Selects DC/DC Channel C to supply VNEGC
		2-3	Selects AVSS to supply VNEGC
JP7	1-2	1-2	Selects DC/DC Channel D to supply VPOSD
		2-3	Selects PVDD/AVDD to supply VPOSD
JP8	1-2	1-2	Selects DC/DC Channel D to supply VNEGD
		2-3	Selects AVSS to supply VNEGD
JP9	Not installed	Installed	Connects the SM-USB-DIG supply to DVDD
		Not installed	Disconnects the SM-USB-DIG supply from DVDD
JP10	1-2	1-2	Selects the DAC8775 internal reference
		2-3	Selects the REF5050 external reference
JP11	Not installed	Installed	Disables internal DVDD LDO
		Not installed	Enables internal DVDD LDO
JP12	2-3	1-2	Issues a clear command to the DAC8775
		2-3	No operation
JP13	Not installed	Installed	Selects the external DVDD
		Not installed	Disconnects the external DVDD
JP14	Not installed	Installed	Issues a hardware reset to the DAC8775
		Not installed	No operation
JP15	Installed	Installed	Select asynchronous update mode
		Not installed	Select synchronous update mode
JP16	Installed	Installed	VSENSEPA is shorted to VOUTA on-board
		Not installed	VSENSEPA is shorted to VOUTA off-board
JP17	Installed	Installed	VSENSEPB is shorted to VOUTB onboard
		Not installed	VSENSEPB is shorted to VOUTB off-board
JP18	Not installed	Installed	Loads VOUTA/IOUTA with a short to GND
		Not installed	Unloads VOUTA/IOUTA of the short to GND
JP19	Installed	Installed	Loads VOUTA/IOUTA with a 250-Ω resistor
		Not installed	Unloads VOUTA/IOUTA of the 250-Ω resistor
JP20	Not installed	Installed	Loads VOUTA/IOUTA with a 625-Ω resistor
		Not installed	Unloads VOUTA/IOUTA of the 625-Ω resistor

Table 3. EVM Jumper Summary (continued)

JUMPER LABEL	DEFAULT	POSITION	FUNCTION
JP21	Not installed	Installed	Loads VOUTA/IOUTA with a 1-kΩ resistor
		Not installed	Unloads VOUTA/IOUTA the 1-kΩ resistor
JP22	Not installed	Installed	Loads VOUTB/IOUTB with a short to GND
		Not installed	Unloads VOUTB/IOUTB of the short to GND
JP23	Not installed	Installed	Loads VOUTB/IOUTB with a 250-Ω resistor
		Not installed	Unloads VOUTB/IOUTB of the 250-Ω resistor
JP24	Not installed	Installed	Loads VOUTB/IOUTB with a 625-Ω resistor
		Not installed	Unloads VOUTB/IOUTB of the 625-Ω resistor
JP25	Not installed	Installed	Loads VOUTB/IOUTB with a 1-kΩ resistor
		Not installed	Unloads VOUTB/IOUTB the 1-kΩ resistor
JP26	Installed	Installed	VSENSENA is shorted to GND onboard
		Not installed	VSENSENA is shorted to GND off-board
JP27	Installed	Installed	VSENSENB is shorted to GND onboard
		Not installed	VSENSENB is shorted to GND off-board
JP28	Installed	Installed	When HARTIN_A is not in use, AC couple to GND
		Not installed	When HARTIN_A is in use, disconnect from GND
JP29	Installed	Installed	When HARTIN_B is not in use, AC couple to GND
		Not installed	When HARTIN_B is in use, disconnect from GND
JP30	Installed	Installed	VSENSEPC is shorted to VOUTA onboard
		Not installed	VSENSEPC is shorted to VOUTA off-board
JP31	Installed	Installed	VSENSEPD is shorted to VOUTB onboard
		Not installed	VSENSEPD is shorted to VOUTB off-board
JP32	Not installed	Installed	Loads VOUTC/IOUTC with a short to GND
		Not installed	Unloads VOUTC/IOUTC of the short to GND
JP33	Not installed	Installed	Loads VOUTC/IOUTC with a 250-Ω resistor
		Not installed	Unloads VOUTC/IOUTC of the 250-Ω resistor
JP34	Not installed	Installed	Loads VOUTC/IOUTC with a 625-Ω resistor
		Not installed	Unloads VOUTC/IOUTC of the 625-Ω resistor
JP35	Not installed	Installed	Loads VOUTC/IOUTC with a 1-kΩ resistor
		Not installed	Unloads VOUTC/IOUTC the 1-kΩ resistor
JP36	Not installed	Installed	Loads VOUTD/IOUTD with a short to GND
		Not installed	Unloads VOUTD/IOUTD of the short to GND
JP37	Not installed	Installed	Loads VOUTD/IOUTD with a 250-Ω resistor
		Not installed	Unloads VOUTD/IOUTD of the 250-Ω resistor
JP38	Not installed	Installed	Loads VOUTD/IOUTD with a 625-Ω resistor
		Not installed	Unloads VOUTD/IOUTD of the 625-Ω resistor
JP39	Not installed	Installed	Loads VOUTD/IOUTD with a 1-kΩ resistor
		Not installed	Unloads VOUTD/IOUTD the 1-kΩ resistor
JP40	Installed	Installed	VSENSENC is shorted to GND onboard
		Not installed	VSENSENC is shorted to GND off-board
JP41	Installed	Installed	VSENSEND is shorted to GND onboard
		Not installed	VSENSEND is shorted to GND off-board
JP42	Installed	Installed	When HARTIN_C is not in use, AC couple to GND
		Not installed	When HARTIN_C is in use, disconnect from GND
JP43	Installed	Installed	When HARTIN_D is not in use, AC couple to GND
		Not installed	When HARTIN_D is in use, disconnect from GND

2.4 Powering the EVM

This section describes the various power configurations that can be used by the EVM.

2.4.1 PVDD_X/AVDD Supply

The PVDD_X, the buck-boost converter supplies, and AVDD, the analog supply, of the DAC8775 are connected to the same power net labeled PVDD/AVDD on the DAC8775EVM. Terminal block J2, shown in Figure 3, allows for external voltage sources to be connected to the PVDD/AVDD supply. The PVDD/AVDD supply must be provided regardless of whether the buck-boost converter is in use or not.

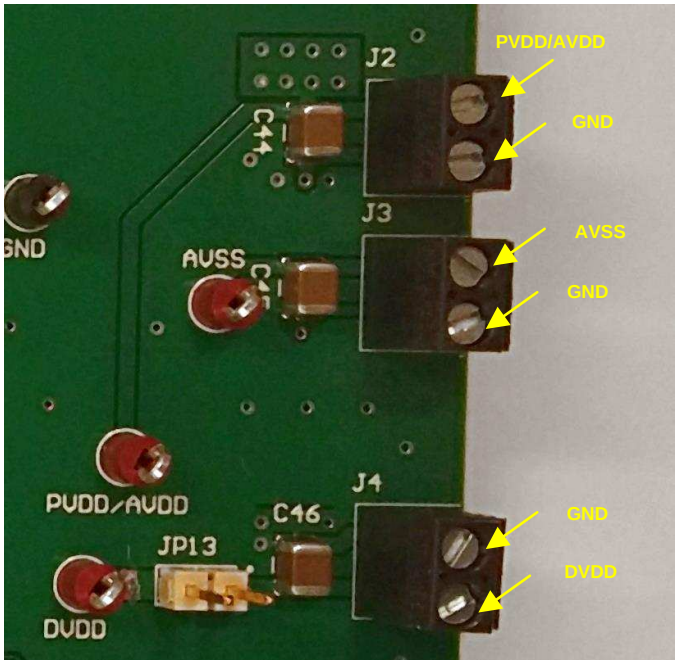

Figure 3. PVDD/AVDD, AVSS, and DVDD Supply Connections

2.4.2 VPOS_X and VNEG_X Supplies

VPOS_X, the positive supply for the output signal chain, and VNEG_X, the negative supply for the output signal chain, may be powered by the DAC8775 internal buck-boost converters or by off-board supply voltages.

WARNING

Permanent device damage may occur if externally supplying VPOS_X or VNEG_X while the internal buck-boost supply is enabled.

When using the DAC8775 internal buck-boost converters to supply VPOS_X and VNEG_X, install JP1 through JP8 (or the two jumpers that correspond to the channel of interest) in the 1-2 position, or "inside" position, as indicated by Table 3.

When using external equipment to supply VPOS_X and VNEG_X, install JP1 through JP8 (or the two jumpers that correspond to the channel of interest) in the 2-3 position, or "outside" position, as indicated by Table 3. In this configuration, the VPOS_X supplies are connected to the PVDD/AVDD net and the VNEG_X supplies are connected to the AVSS net. If bipolar supplies are used, connect an appropriate negative supply voltage to AVSS through terminal block J3, as shown in Figure 3. If unipolar supplies are used, connect AVSS to ground through terminal block J3.

2.4.3 DVDD Supply

DVDD, the digital supply voltage, of the DAC8775 can be supplied by the SM-USB-DIG VDUT supply (pin 6 of J1), an external supply voltage through J4 (illustrated in Figure 3), or by the DAC8775 internal DVDD LDO. When using the SM-USB-DIG as the DVDD supply, uninstall jumper JP13 and install jumpers JP9 and JP11. To use an external supply voltage as the DVDD supply, install jumpers JP13 and JP11 and uninstall JP9. To use the DAC8775 internal LDO as the DVDD supply, uninstall jumpers JP9, JP13, and JP11.

In each DVDD supply configuration, take care to ensure that digital logic thresholds of the host and DAC8775 match and that the absolute maximum ratings of the DAC8775 are not violated.

2.5 EVM Features

This section describes some of the hardware features present on the EVM board.

2.5.1 Communication Test Points

The EVM board features test points for monitoring the communication between the SM-USB-DIG and the DAC8775. Test points are provided for the !LDAC, CLR, ALARM, RESET, SDIN, SCLK, !SYNC, and SDO pins of the DAC8775.

Figure 4. Digital Communication Test Points

The EVM design also allows external signals to be connected through these communication test points if the EVM is integrated into a custom evaluation setup or application specific prototype. Note that if the SM-USB-DIG platform is not used, DVDD must be configured to use the DAC8775 internal DVDD LDO or external supplies as described in Section 2.4.3.

2.5.2 Reference Voltage

The DAC8775 reference voltage can be supplied by the internal voltage reference, by the onboard REF5050, or by an external reference voltage.

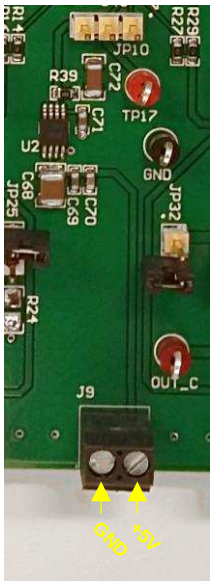

Figure 5. Onboard Reference Supply Connections

To use the internal reference voltage, place JP10 in the 1-2 position. To use the REF5050 reference voltage, place JP10 in the 2-3 position and connect a supply voltage for the REF5050 to J9, as shown in Figure 5. To use an external reference voltage, remove JP10 and the reference can be connected to the DAC8775EVM through the center post of JP10.

2.5.3 VOUT_X, VSENSEP_X, and VSENSEN_X

The VOUT_X pins can be access on terminal blocks J5, J6, J7, and J8 or by the OUT_A, OUT_B, OUT_C, or OUT_D test points. The VSENSEP_X and VSENSEN_X sense connections may be provided onboard or externally closer to the point of load through terminal blocks J5, J6, J7, or J8. To provide the VSENSEP_X connections onboard, install JP16, JP17, JP30, or JP31 based on the channel of interest. Similarly, to provide VSENSEN_X connections onboard, install JP26, JP27, JP40, or JP41. Removing these jumpers requires that the sense connections are made external to the EVM board. Figure 6 shows the arrangement of the output terminal blocks.

2.5.4 IOUT_X

The IOUT_X pins can be accessed on terminal blocks J5, J6, J7, or J8 or by the test points OUT_A, OUT_B, OUT_C, or OUT_D.

2.5.5 Onboard Output Loads

Four load choices are installed on the EVM board to evaluate the voltage and current outputs as well as the adaptive power management performance of the DAC8775. JP18, JP22, JP32, or JP36 are available to provide a short-circuit condition on the outputs. JP19, JP23, JP33, or JP37 provide a 250-Ω load on the outputs. JP20, JP24, JP34, or JP38 are available to provide a 625-Ω on the outputs. JP21, JP25, JP35, or JP39 provides a 1-kΩ load on the outputs.

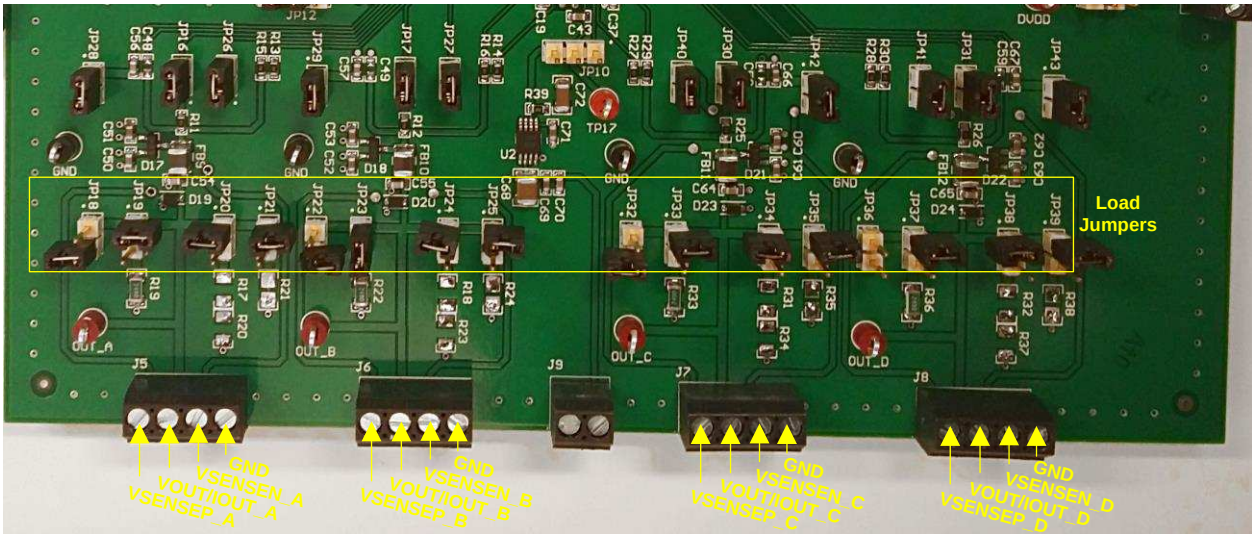

Figure 6. Output Terminal Block Connections and Load Jumpers

2.5.6 Applying HART Signals

JP28, JP29, JP42, and JP43 are available to couple external HART FSK communication signals onto the current outputs. When injecting the HART signal, remove JP28, JP29, JP42, or JP43 and apply the HART signal to pin 1. When a HART signal is not being injected, install JP28, JP29, JP42, or JP43, with AC coupling the HART pins to ground.

2.6 Connecting the SM-USB-DIG

To connect the EVM board and the SM-USB-DIG platform together, firmly slide the male and female ends of the 10-pin connectors together with the Texas Instruments logo of the SM-USB-DIG facing up as shown in Figure 7. Make sure that the two connectors are completely pushed together as loose connections may cause intermittent operation.

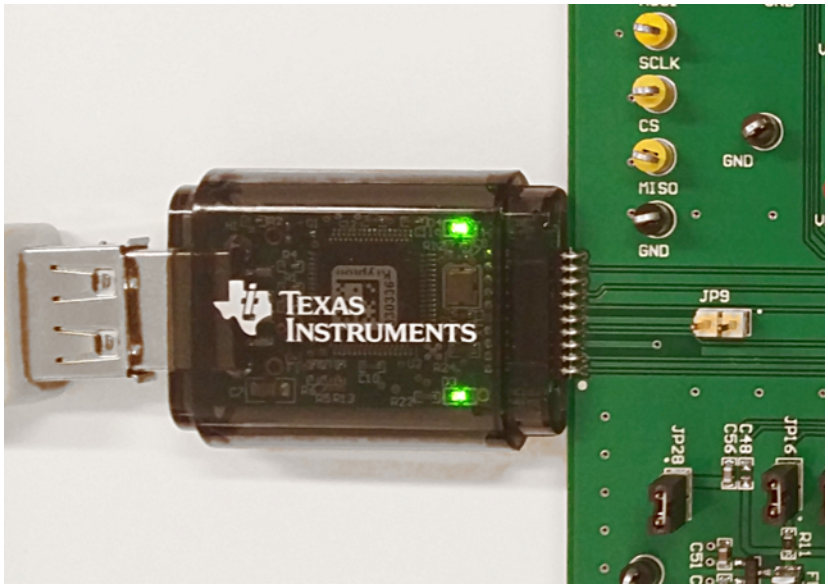

Figure 7. SM-USB-DIG Connection

2.7 Signal Definitions of J1 (10-Pin SM-USB-DIG Connector)

Table 4 shows the pin-out for the 10-pin connector used to communicate between the EVM and the SM-USB-DIG. Note that the I_2C communication lines (I2C_SCL and I2C_SDA1) are not used.

Table 4. SM-USB-DIG Connector

PIN ON J1	SIGNAL	DESCRIPTION
1	I2C_SCL	I_2C clock signal (SCL)
2	CTRL/MEAS4	GPIO: Control output or measure input
3	I2C_SDA1	I_2C data signal (SDA)
4	CTRL/MEAS5	GPIO: Control output or measure input
5	SPI_DOUT1	SPI data output (MOSI)
6	VDUT	Switchable DUT power supply: 3.3 V, 5 V, Hi-Z (disconnected). Note: When VDUT is Hi-Z, all digital I/Os are Hi-Z as well
7	SPI_CLK	SPI clock signal (SCLK)
8	GND	Power return (GND)
9	SPI_CS1	SPI chip-select signal (!CS)
10	SPI_DIN1	SPI data input (MISO)

3 EVM Software Setup

This section discusses how to install the EVM software.

3.1 Operating Systems for EVM Software

The EVM software has been tested on the Windows XP® and Windows 7® operating systems with United States and European regional settings. The software should also function on other Windows operating systems.

3.2 EVM Software Installation

The EVM software may be downloaded by following the instructions provided external to this document. To install the software, locate and extract the file named DAC8775.zip to a specific folder (for example, C:\DAC8775\) on the hard drive.

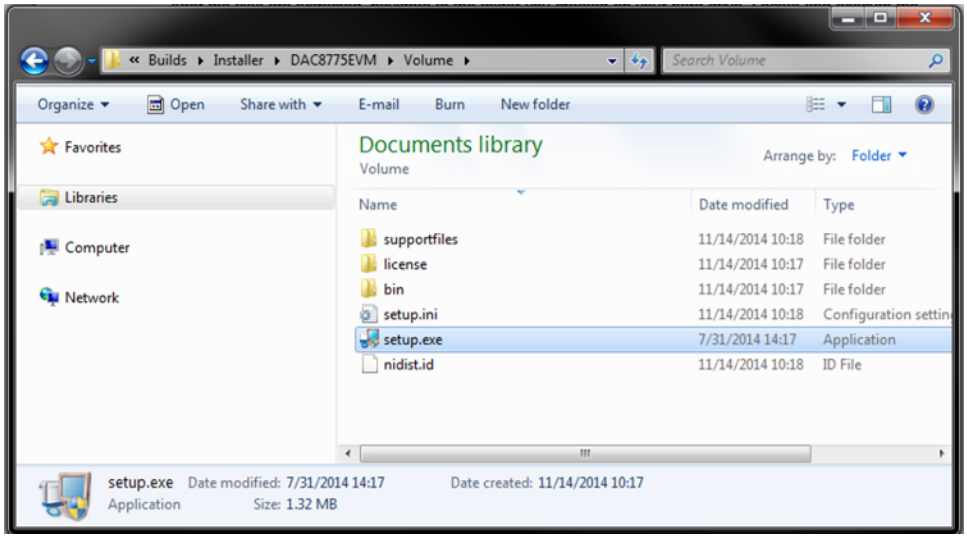

Figure 8. DAC8775EVM Installer

After the files are extracted, navigate to the folder created on the hard drive. Locate and execute the setup.exe file to start the installation. The DAC8775 software installer file then opens to begin the installation process.

After the installation process initializes, the user is given a choice of selecting the installation directory, usually defaulting to C:\Program Files(x86)\DAC8775EVM\ and C:\Program Files(x86)\National Instruments\.

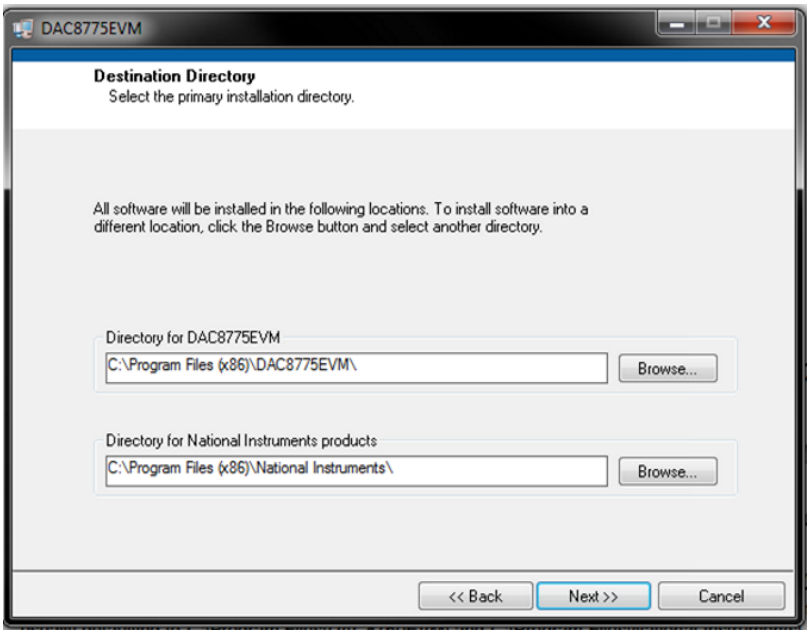

Figure 9. DAC8775EVM Install Path

After selecting the installation directory, two license agreements are presented that must be accepted.

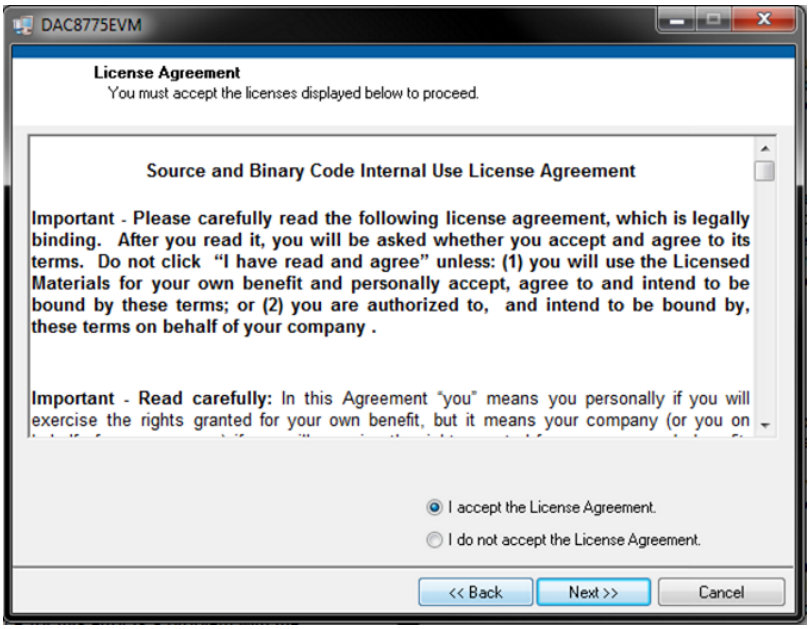

Figure 10. DAC8775EVM Software License Agreements

After accepting the Texas Instruments and National Instruments license agreements, the progress bar opens and shows the installation of the software. Once the installation process is completed, click Finish.

4 EVM Software Overview

This section describes the use of the EVM software. Figure 11 shows the front panel of the EVM GUI.

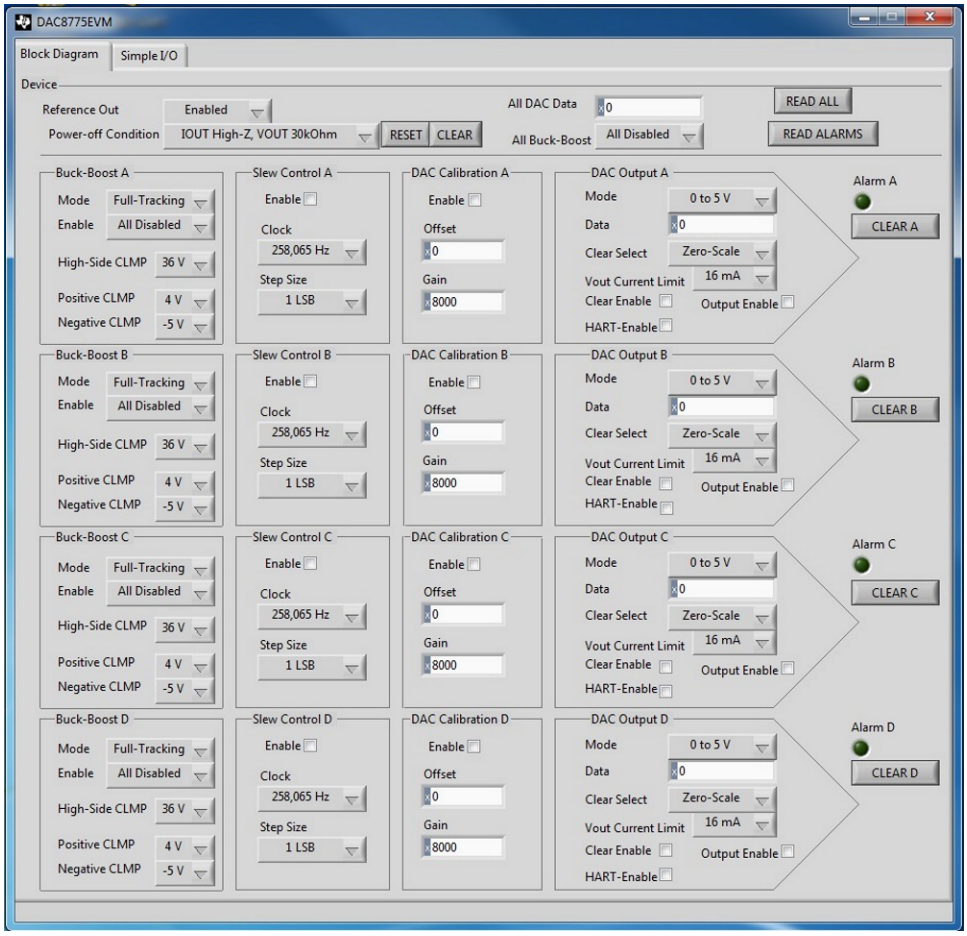

Figure 11. EVM GUI – Front Panel

4.1 Starting the EVM Software

The EVM software can be operated through the Windows start menu. From the start menu, select All Programs, and then select DAC8775EVM.

An error will appear if the PC cannot communicate with the EVM. If this error happens, first ensure that the USB cable is properly connected on both ends. This error can also occur if the USB cable is connected before the SM-USB-DIG platform power source. Another possible source for this error is a problem with the USB human interface driver on the PC. Make sure the device is recognized when the USB cable is plugged in, as indicated by a Windows-generated confirmation sound.

4.2 Reading From and Writing to Registers

The EVM software automatically reads from the DAC8775 when a reset or clear command is issued. To read from the device in other situations, press the READ ALL button on the EVM GUI. Write actions are carried out automatically when the value of any element on the GUI is changed.

4.3 Device Controls

This section describes the GUI controls for the internal reference, power-on conditions, clear, software reset, and DAC broadcast functionality.

4.3.1 Internal Reference

The internal reference can be enabled or disabled using the internal reference control on the EVM GUI. By default, the internal reference is disabled.

4.3.2 Power-On Condition

By default the power-on state of the current output is Hi-Z and the voltage output is 30 kΩ to ground after a clear or reset command. The power-on condition GUI control allows control of the voltage output power-on condition as either 30 kΩ to ground or Hi-Z.

4.3.3 Software Reset

The RESET button on the GUI issues a software reset to the DAC8775, restoring the default power-on register contents. The GUI immediately reads all of the registers of the device to synchronize the GUI and hardware. A hardware reset can be issued through JP14. If a hardware issue is issued the READ ALL button should be pressed to synchronize the GUI and hardware.

4.3.4 Software Clear

The CLEAR button on the GUI issues a clear command to the DAC8775, restoring the DAC data registers to full-scale or zero-scale based on each channel's clear select settings and clear enable settings. After a clear command is issued the GUI immediately reads the data registers of the device to synchronize the GUI and hardware. A hardware clear command can be issued through JP12. If a hardware clear is issued the READ ALL button should be pressed to synchronize the GUI and hardware.

4.4 DAC Controls

4.4.1 DAC Outputs

The DACs can be configured for voltage or current outputs of various spans through the Output Mode control on the GUI. The DAC output can be set to active or inactive by checking or removing the check from the Output Enable Boolean control on the GUI. Once an output range is selected and the output is enabled, the DAC output value can be controlled by writing values to the DAC Data control. The DAC Data control expects hexadecimal input formats. The small indicator on the left side of the DAC Data control can be used to change the input data format.

Output current drive can be programmatically limited for each of the voltage output modes through the V_{OUT} Current Limit control on the GUI. Take note that the actual current limit will be compliant to the values specified in the DAC8775 electrical characteristics table.

4.4.2 Clear Functionality

Each DAC output has a Clear Enable Boolean that is AND'd with the CLEAR command. If the Clear Enable Boolean is checked, the output channel will respond to a clear event; conversely, if the Boolean is unchecked, the output channel will not respond to a clear event. Each DAC can be programmed to clear to either zero-scale or full-scale. This behavior can be controlled by the Clear Select control on the GUI.

4.4.3 HART Inputs

The enable HART signals to be coupled to the current outputs through the onboard coupling path the HART-Enable Boolean control must be checked.

4.5 DAC Calibration Controls

Each DAC may use digital calibration to reduce offset and gain errors at each channel's output. By default the calibration features are disabled. To enable the calibration features, the Calibration Enable Boolean control must be checked. When the control is checked, offset and gain calibration may be controlled by the values written to each channels Offset Calibration and Gain Calibration controls, respectively, on the EVM GUI. For more information concerning the calibration features, please refer to the DAC8775 datasheet.

4.6 Slew-Rate Controls

The slew-rate of each channel may be controlled by the slew control registers for each channel. By default the slew-rate control features are disabled. To enable the slew-rate control features the Slew-Rate Ctl Enable Boolean control must be checked. When the control is checked, slew-rate step size and clock registers may be used to control the output's slew-rate through the Slew-Rate Ctl Step Size and Slew-Rate Ctl Clock respectively.

4.7 Buck-Boost Converter Controls

Each buck-boost converter can be configured through the EVM GUI. The Buck-Boost Mode control is used to select the operating mode of the buck-boost converter and the Buck-Boost Enable control is used to enable the positive, negative, or both arms of the buck-boost converter. When Buck-Boost Mode is set to Clamp Mode, the positive clamp and negative clamp controls are used to set each arm's output clamp.

5 EVM Documentation

This section contains the complete bill of materials and schematic diagram for the DAC8775EVM. Documentation information for the SDM-USB-DIG Platform can be found in the *SDM-USB-DIG Platform User's Guide* (SBOU136) available at www.TI.com.

5.1 EVM Board Schematic

Figure 12, Figure 13, and Figure 14 illustrate the DAC8775EVM board schematics.

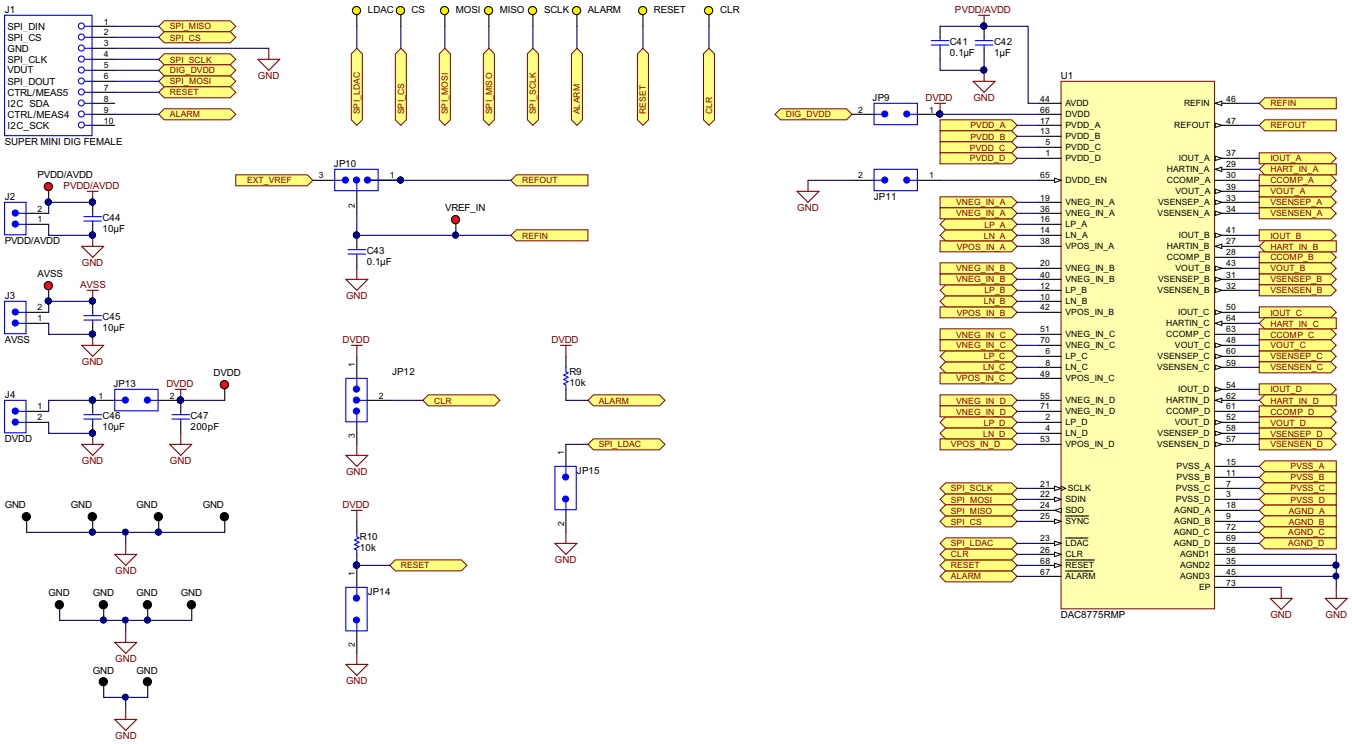

Figure 12. Device Schematic

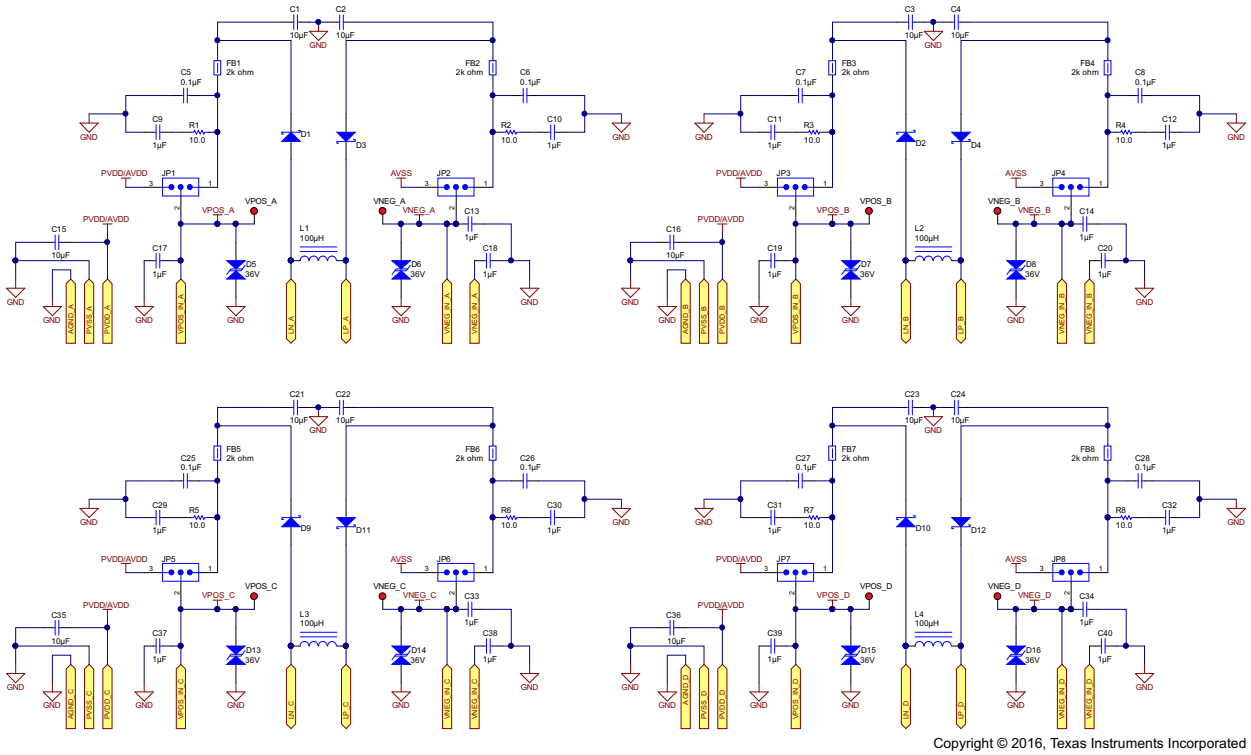

Figure 13. DC-DC Schematic

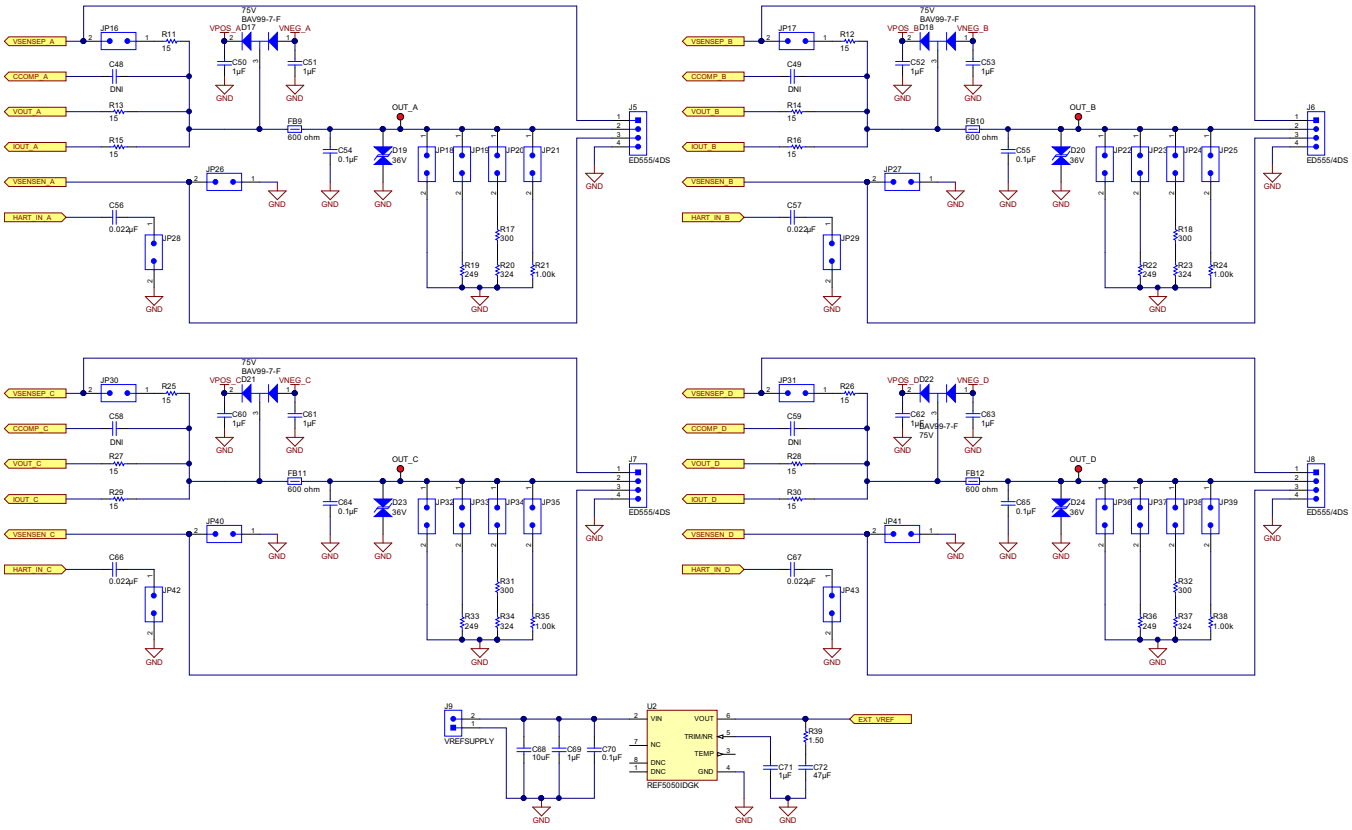

Figure 14. Outputs Schematic

5.2 EVM PCB Components Layout

Figure 15 shows the layout of the components for the EVM board.

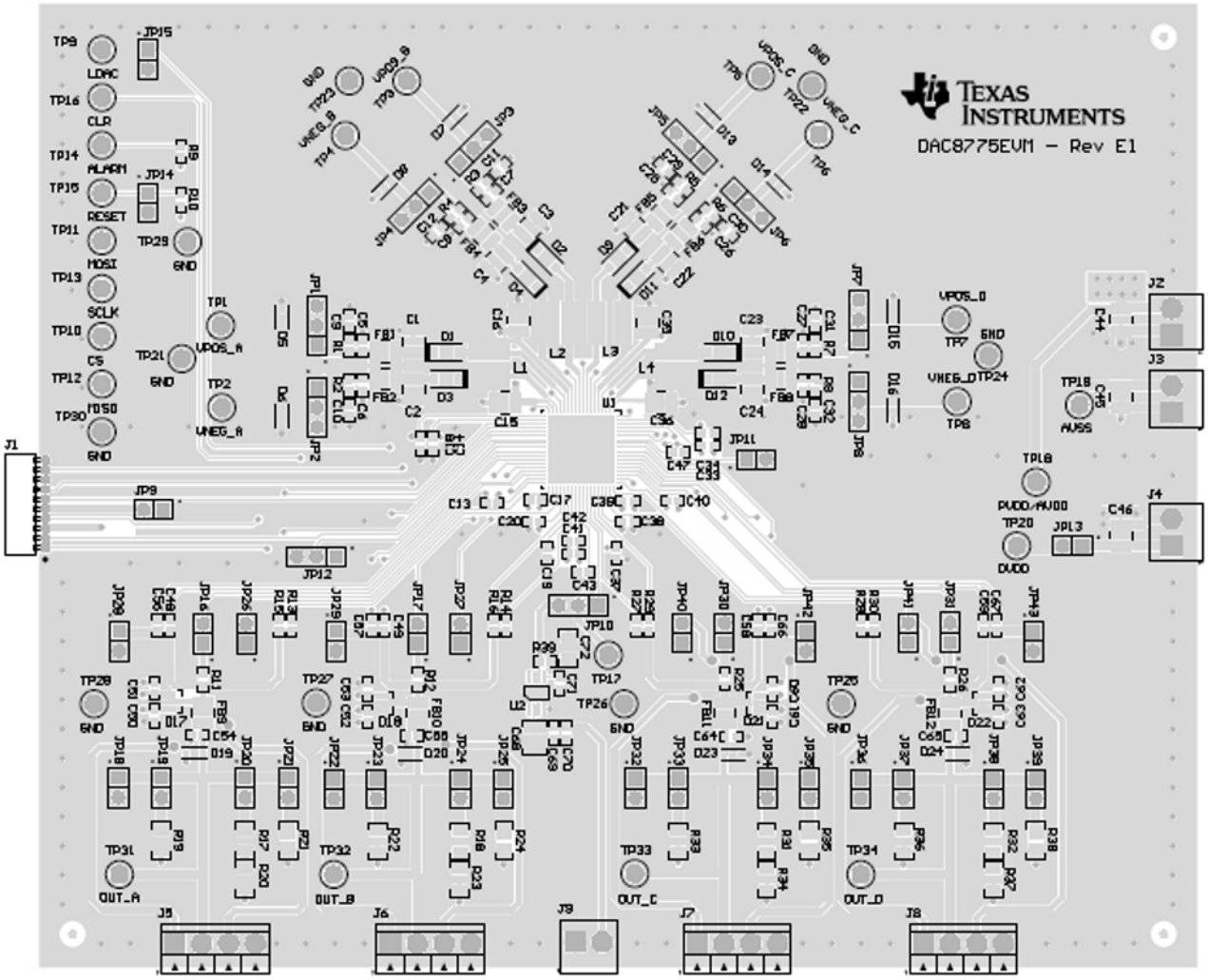

Figure 15. DAC8775EVM PCB Components Layout

5.3 EVM Board Bill of Materials

Table 5 lists the EVM board bill of materials.

Table 5. EVM Board Bill of Materials

QTY	DESIGNATOR	DESCRIPTION	PARTNUMBER	MANUFACTURER
1	!PCB1	Printed Circuit Board	PA005	Any
15	C1, C2, C3, C4, C15, C16, C21, C22, C23, C24, C35, C36, C44, C45, C46	CAP, CERM, 10uF, 50V, +/-10%, X7R, 1210 (H=2.5mm)	UMK325AB7106KM-T	Taiyo Yuden
15	C5, C6, C7, C8, C25, C26, C27, C28, C41, C43, C54, C55, C64, C65, C70	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	GRM188R71H104KA93D	MuRata
31	C9, C10, C11, C12, C13, C14, C17, C18, C19, C20, C29, C30, C31, C32, C33, C34, C37, C38, C39, C40, C42, C50, C51, C52, C53, C60, C61, C62, C63, C69, C71	CAP, CERM, 1uF, 50V, +/-10%, X7R, 0603	UMK107AB7105KA-T	Taiyo Yuden
1	C47	CAP, CERM, 200pF, 50V, +/-5%, C0G/NP0, 0603	GRM1885C1H201JA01D	MuRata
4	C48, C49, C58, C59	DNI		
4	C56, C57, C66, C67	CAP, CERM, 0.022uF, 50V, +/-10%, X7R, 0603	C1608X7R1H223K	TDK
1	C68	CAP CER 10UF 50V 20% X7R 1210	UMK325AB7106MM-T	Taiyo Yuden
1	C72	CAP, CERM, 47uF, 25V, +/-20%, X5R, 1206	C3216X5R1E476M160AC	TDK
8	D1, D2, D3, D4, D9, D10, D11, D12	Diode, Schottky, 60V, 1A, SOD-123	MBRX160-TP	Micro Commercial Components
12	D5, D6, D7, D8, D13, D14, D15, D16, D19, D20, D23, D24	Diode, TVS, Bi, 36V, 400W, SOD323, 2-Leads, Body 1.9x1.45mm, No Polarity Mark	CDSOD323-T36SC	Bourns
4	D17, D18, D21, D22	Diode, Switching, 75V, 0.3A, SOT-23	BAV99-7-F	Diodes Inc.
8	FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8	Ferrite Bead, 2000 ohm @ 100MHz, 1.2A, 1210 (H=2.5mm)	FB MH3225HM202NT	Taiyo Yuden
4	FB9, FB10, FB11, FB12	Ferrite Bead, 600 ohm @ 100MHz, 3A, 1210 (H=2.5mm)	FBMH3225HM601NT	Taiyo Yuden
1	J1	Receptacle, 50mil 10x1, R/A, TH	851-43-010-20-001000	Mill-Max
4	J2, J3, J4, J9	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	ED555/2DS	On-Shore Technology
4	J5, J6, J7, J8	Terminal Block, 6A, 3.5mm Pitch, 4-Pos, TH	ED555/4DS	On-Shore Technology
10	JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP10, JP12	Header, TH, 100mil, 3x1, Gold plated, 230 mil above insulator	TSW-103-07-G-S	Samtec, Inc.
33	JP9, JP11, JP13, JP14, JP15, JP16, JP17, JP18, JP19, JP20, JP21, JP22, JP23, JP24, JP25, JP26, JP27, JP28, JP29, JP30, JP31, JP32, JP33, JP34, JP35, JP36, JP37, JP38, JP39, JP40, JP41, JP42, JP43	Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	TSW-102-07-G-S	Samtec
4	L1, L2, L3, L4	Inductor, Shielded Drum Core, Ferrite, 100uH, 0.52A, 0.77 ohm, SMD	74408943101	Wurth Elektronik eiSos
8	R1, R2, R3, R4, R5, R6, R7, R8	RES, 10.0 ohm, 1%, 0.1W, 0603	CRCW060310R0FKEA	Vishay-Dale
2	R9, R10	RES, 10k ohm, 5%, 0.1W, 0603	CRCW060310K0JNEA	Vishay-Dale

Table 5. EVM Board Bill of Materials (continued)

QTY	DESIGNATOR	DESCRIPTION	PARTNUMBER	MANUFACTURER
12	R11, R12, R13, R14, R15, R16, R25, R26, R27, R28, R29, R30	RES, 15 ohm, 5%, 0.1W, 0603	CRCW060315R0JNEA	Vishay-Dale
4	R17, R18, R31, R32	RES, 300, 0.1%, 0.25 W, 1206	ERA-8AEB301V	Panasonic
4	R19, R22, R33, R36	RES, 249, 0.1%, 0.25 W, 1206	TNPW1206249RBEEA	Vishay-Dale
4	R20, R23, R34, R37	RES, 324, 0.1%, 0.25 W, 1206	ERA-8AEB3240V	Panasonic
4	R21, R24, R35, R38	RES, 1.00 k, 0.1%, 1 W, 1206 resistor	PHP01206E1001BST5	Vishay-Dale
1	R39	RES, 1.50 ohm, 1%, 0.1W, 0603	CRCW06031R50FKEA	Vishay-Dale
16	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP17, TP18, TP19, TP20, TP31, TP32, TP33, TP34	Test Point, Compact, Red, TH	5005	Keystone
8	TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16	Test Point, Compact, Yellow, TH	5009	Keystone
10	TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30	Test Point, Compact, Black, TH	5006	Keystone
1	U1	Quad-Channel, 16-Bit Programmable Current Output and Voltage Output Digital-to-Analog Converter with Adaptive Power Management, RMP0072A	DAC8775RMP	Texas Instruments
1	U2	Low-Noise, Very Low Drift, Precision Voltage Reference, DGK0008A	REF5050IDGK	Texas Instruments
1	U2	Low-Noise, Very Low Drift, Precision Voltage Reference, DGK0008A	REF5050IDGK	Texas Instruments

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