User's Guide

ADS8688EVM-PDK Evaluation Module

Data Acquisition Products

ABSTRACT

ADS8688EVM-PDK

This user's guide describes the operation and use of the ADS8688 evaluation module (EVM). The ADS8688 is a 16-bit, 500ksps, 8 channel multiplexed, single-supply, SAR ADC with bipolar input ranges. Operating on a single 5V the integrated analog front end can support ±10.24V input ranges with a ±20V over-voltage protection. The performance demonstration kit (PDK) eases EVM evaluation with additional hardware and software for computer connectivity through a universal serial bus (USB). The ADS8688EVM-PDK includes the ADS8688EVM as a daughter card, Precision Host Adaptor (PHI) digital controller, and a A-to-B USB cable. This user's guide covers circuit description, schematic diagram, and bill of materials for the ADS8688EVM daughter card.

Table 1-1. Related Documentation

Device	Literature Number
ADS8688	SBAS582
OPA320	SBOS513
TPS7A4700	SBVS204

Table of Contents

List of Figures

List of Tables

1 Trademarks

All trademarks are the property of their respective owners.

2 ADS8688EVM-PDK Overview

Table 1-1 lists the related documents that are available for download from Texas Instruments at

ADS8688EVM Features

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS8688 ADC
- USB powered—no external power supply is required
- The PHI controller that provides a convenient communication interface to the ADS8688 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output
- Easy-to-use evaluation software for 64-bit Microsoft Windows™7, Windows 8, and Windows 10 operating systems
- The software suite includes graphical tools for data capture, histogram analysis, and spectral analysis. This suite also has a provision for exporting data to a text file for post-processing. Fig
- Integrated 4.096-V voltage reference.
- Bipolar (±10.24 V, ±5,12 V, ±2.56 V) or unipolar (0 V to 10.24 V, 0 V to 5.12 V) input ranges for each channel.
- Onboard, second-order, Butterworth, low-pass filters for four channels.
- Onboard regulator for generating a ±15-V bipolar supply for second-order, Butterworth, low-pass filters.
- Capable of accepting a ±100-mV signal on the negative analog inputs (AIN_xGND).

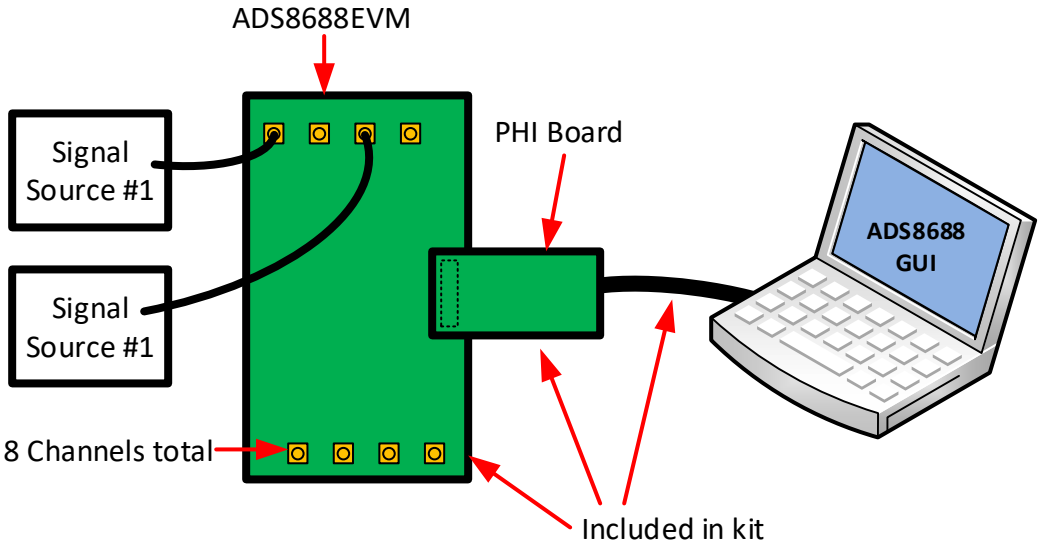

Figure 2-1. System Connection for Evaluation

ADS8688EVM Features:

- Eight input channels connected to external single ended signals source applied to SMA connectors or header
- Serial interface connects to the PHI controller via 60 pin connector (J3).
- Serial interface connects to the PHI controller via 60 pin connector (J2).
- All power for device from USB via PHI controller.
- Onboard ultra-low noise low-dropout (LDO) regulator generates 5.0V AVDD supply. Input to LDO from PHI controller.
- DVDD (3.3V) powered by PHI controller.

3 EVM Analog Interface

The ADS8688EVM is an evaluation module built to the TI Modular EVM system specifications. The EVM by itself has no microprocessor and cannot run software. Thus, the EVM is available as part of the ADS8688EVM-PDK kit that combines the ADS8688EVM as a daughter board with PHI controller using software as a graphical user interface (GUI).

3.1 ADC Analog Input Connections and Filter

The circuit shown in Figure 3-1 shows a typical analog input connection for the ADS8688 ADC. This circuit is reapeated eight times for all eight input channels. The resistor R01 can be used for input float detection but is not populated in the default configuration. The TVS diode D01, can be used for input protection, but is not populated. Refer to Video Series on Electrical Overstress. C01, R03, and R04 form the 79.5kHz low pass input the input filter for the ADC. R05 connects the negative input to ground. R05 can be removed and the negative input can be accessed in the header J6.

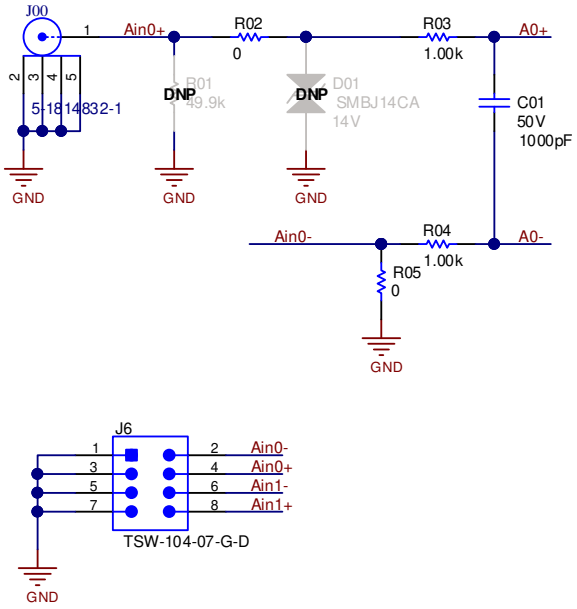

Figure 3-1. ADC Analog Input Connections and Filter

3.2 Voltage Reference, Aux Input, and Supply Decoupling

The circuit shown in Figure 3-2 illustrates the decoupling on AVDD, DVDD, and the reference IO. It is possible on the ADS8688 to use an external voltage reference, but typically the integrated internal reference is sufficient. In cases where you need to use an enthral voltage reference it can be connected via the REF test point. The capacitors for decoupling match the recomendations in the ADS8688 data sheet. The layout (see Figure 8-1) uses the shortest possible connections to the decouplign capacitors and connections the ground end to the GND plane using vias. The AUX input is a standard SAR input and does not have an analog front end. Thus, this input cannot accept high voltage input signals (Vin Full Scale = VREF = 4.096V). Furthermore, this input requires an external buffer amplifier U4 to achieve good settling.

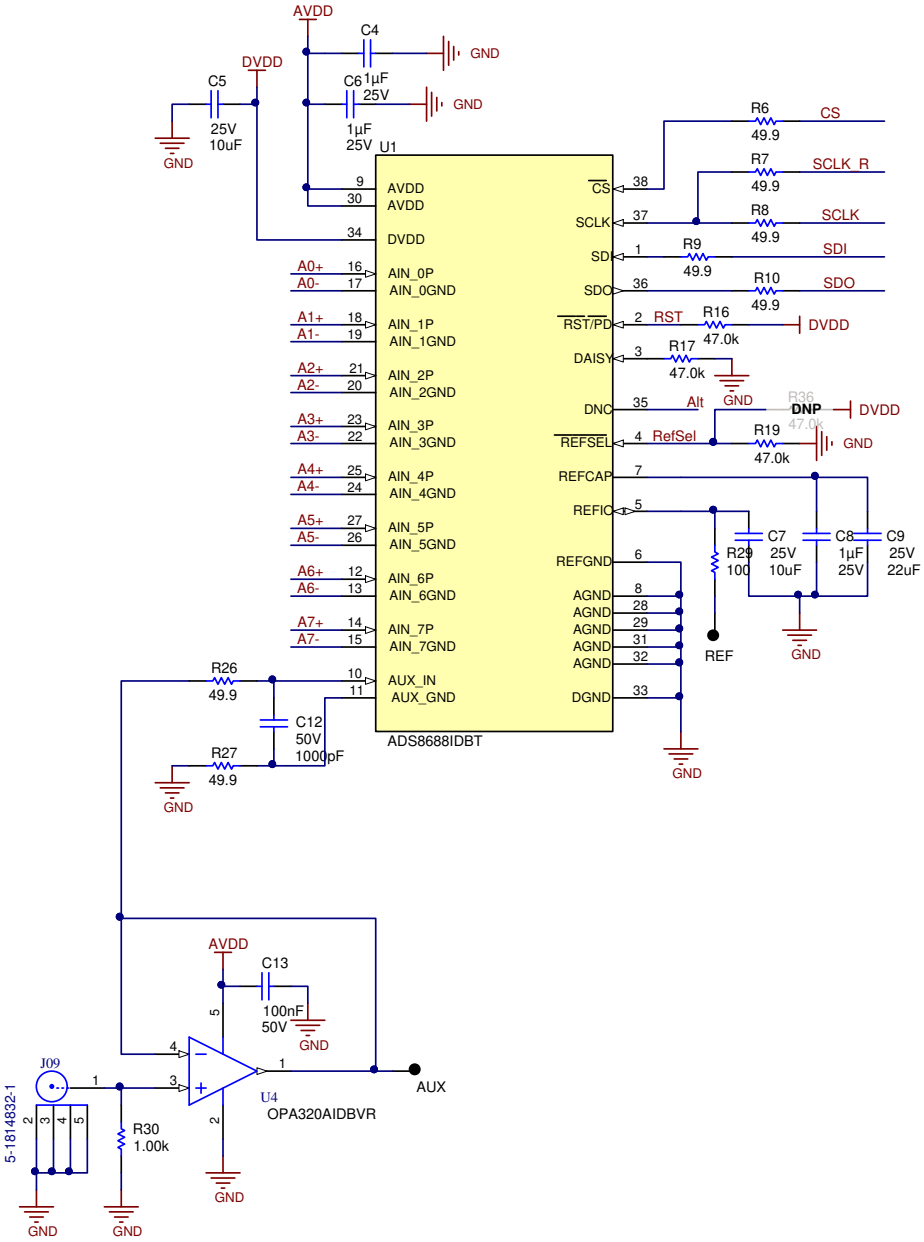

Figure 3-2. Voltage Reference, Aux Input, and Supply Decoupling

4 Digital Interface

As noted in Section 2, the EVM interfaces with the PHI and communicates with the computer over the USB. There are two devices on the EVM with which the PHI communicates: the ADS8688 ADC (over SPI) and the EEPROM (over I2C). The EEPROM comes pre-programmed with the information required to configure and initialize the ADS8688 platform. When the hardware is initialized, the EEPROM is no longer used.

4.1 Serial Interface (SPI)

As noted in Section 2, the EVM interfaces with the PHI and communicates with the computer over the USB. There are two devices on the EVM with which the PHI communicates: the ADS8688 ADC (over SPI) and the EEPROM (over I2C). The EEPROM comes pre-programmed with the information required to configure and initialize the ADS8688 platform. When the hardware is initialized, the EEPROM is no longer used.

4.2 I2C Bus for Onboard EEPROM

The circuit shown in Figure 4-1 is used with our EVM controller (PHI), for EVM identification. This circuit is not required by the ADS8688 for operation. The switch (S2) is a write protect and does not need to be changed for EVM operation.

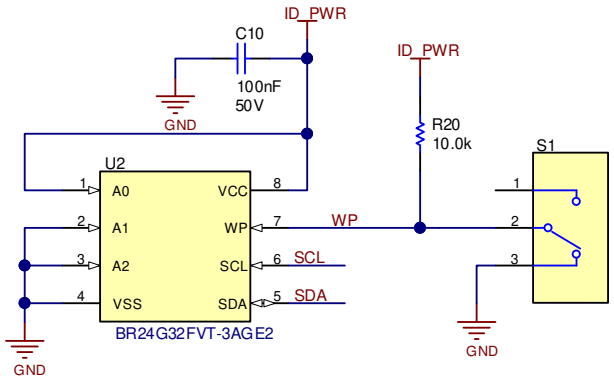

Figure 4-1. EEPROM for EVM ID

5 Power Supplies

The PHI provides multiple power-supply options for the EVM, derived from the USB supply of the computer. The EEPROM on the ADS8688EVM uses a 3.3-V power supply generated directly by the PHI. The EVM_REG_5V5 is a 5.5V supply from the PHI and is applied to the input of a low dropout regulator (LDO) to generate AVDD on the EVM. The analog supply of the ADC (AVDD = 5.0V) is powered by the TPS7A4700RGWR (U3). The ADC Digital supply (DVDD = 3.3V), is generated by the PHI. Two LEDs are connected to the AVDD, and DVDD supplies. These LEDs will illuminate after the software GUI loads and the PHI turns on its output power supplies.

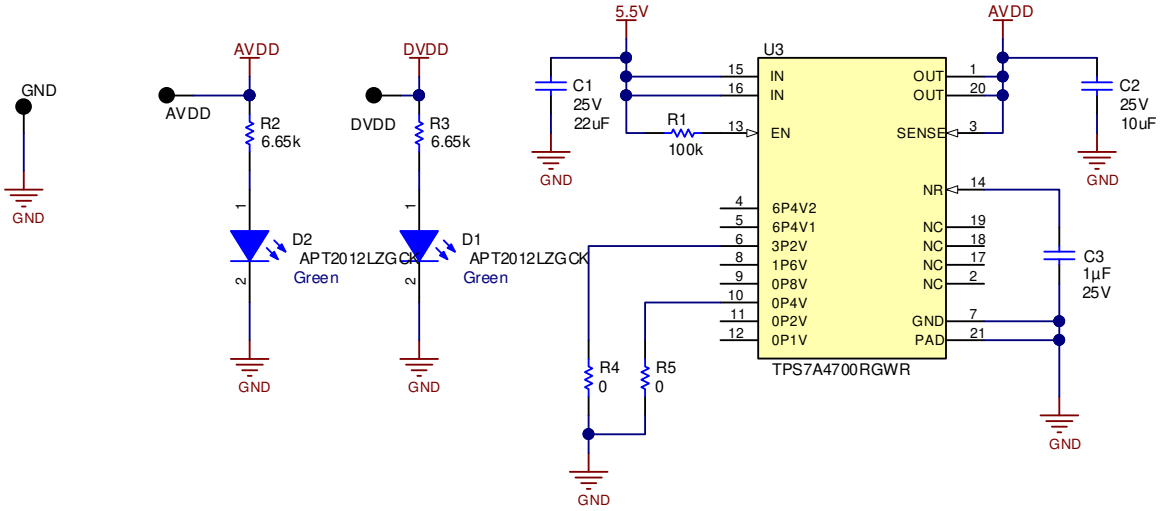

Figure 5-1. Power Supplies, Regulators, and Indicators

6 ADS8688 Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for properly operating the ADS8688EVM.

6.1 Software Installation

Download the latest version of the EVM GUI installer from the Tools and Software folder of the ADS8688EVM and run the GUI installer to install the EVM GUI software on your computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message may appear or the installer. The exe file can be deleted.

Accept the license agreements and follow the on-screen instructions shown in Figure 6-1 to complete the installation.

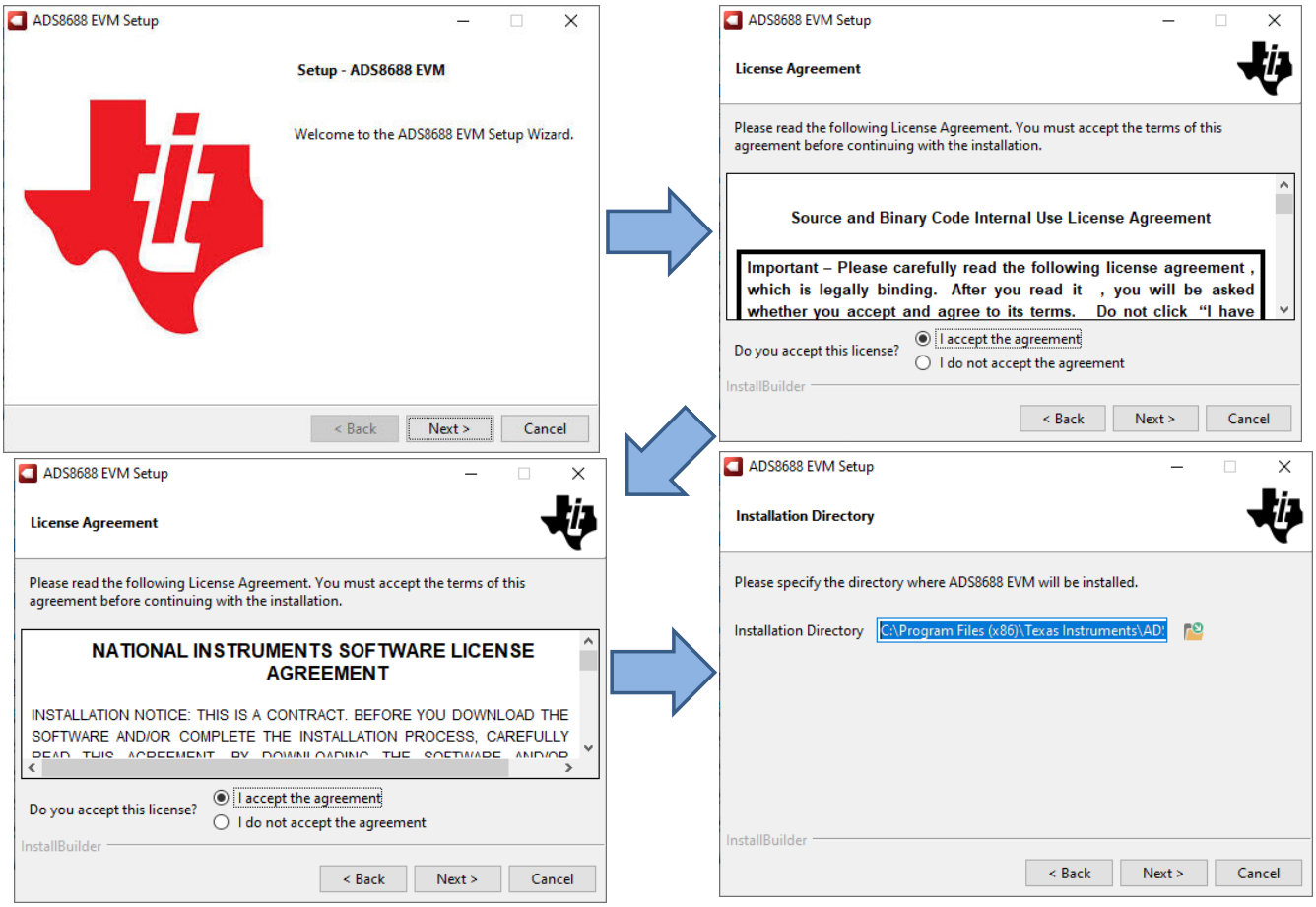

Figure 6-1. ADS8688 Software Installation Prompts

As a part of the ADS8688EVM GUI installation, a prompt with a Device Driver Installation (as shown in Figure 6-2) appears on the screen. Click Next to proceed.

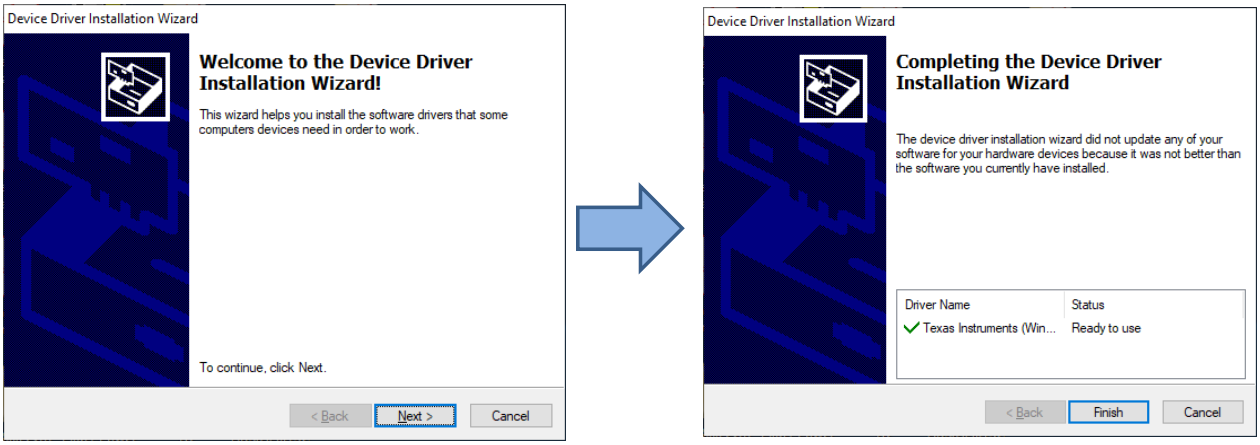

Figure 6-2. Device Driver Installation Wizard Prompts

The ADS8688EVM requires the LabVIEW™ run-time engine and may prompt for the installation of this software, as shown in Figure 6-3, if not already installed.

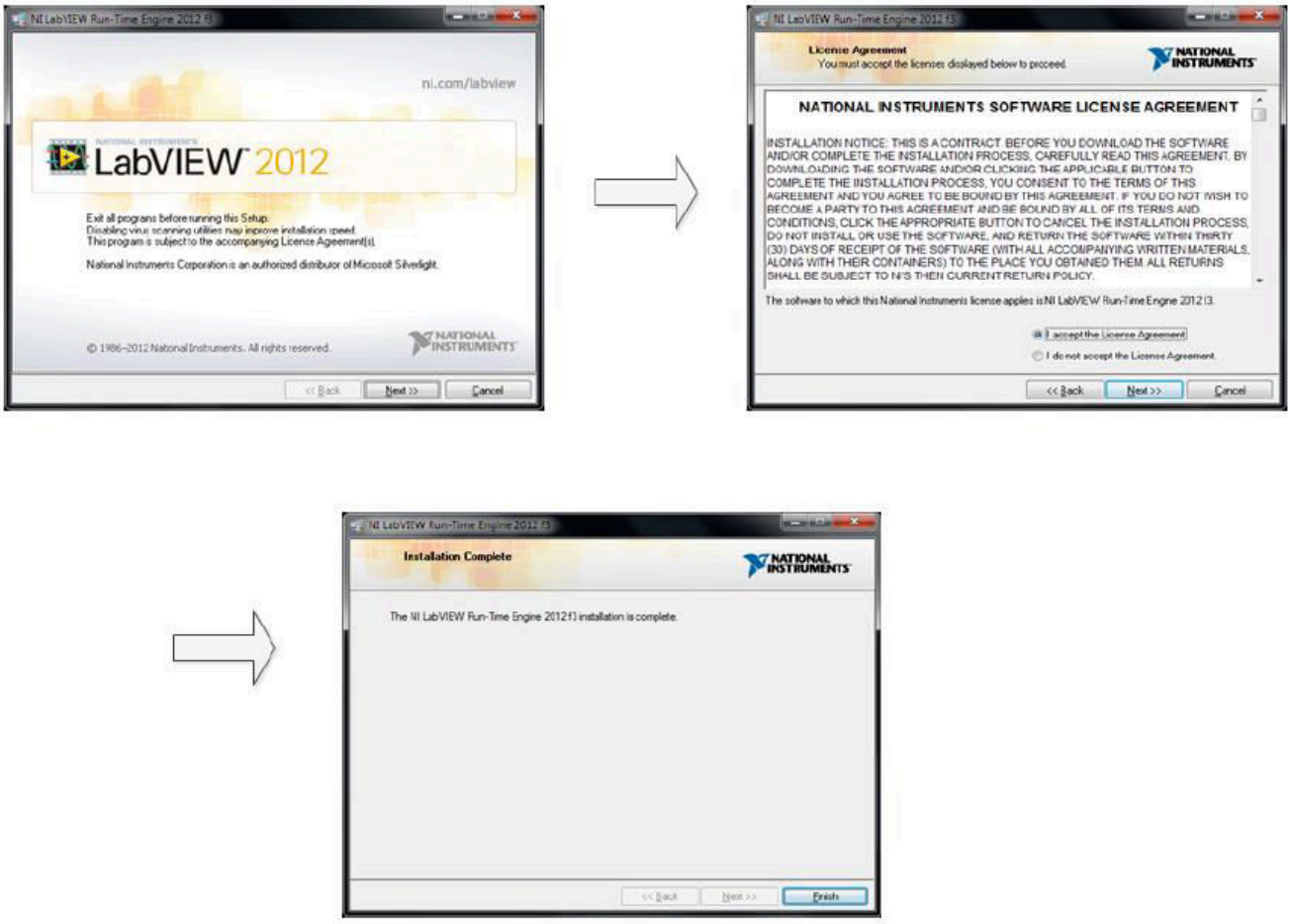

Figure 6-3. LabVIEW Run-Time Engine Installation

Verify that C:\Program Files (x86)\Texas Instruments\ADS8688EVM is as shown in Figure 6-4 after these installations.

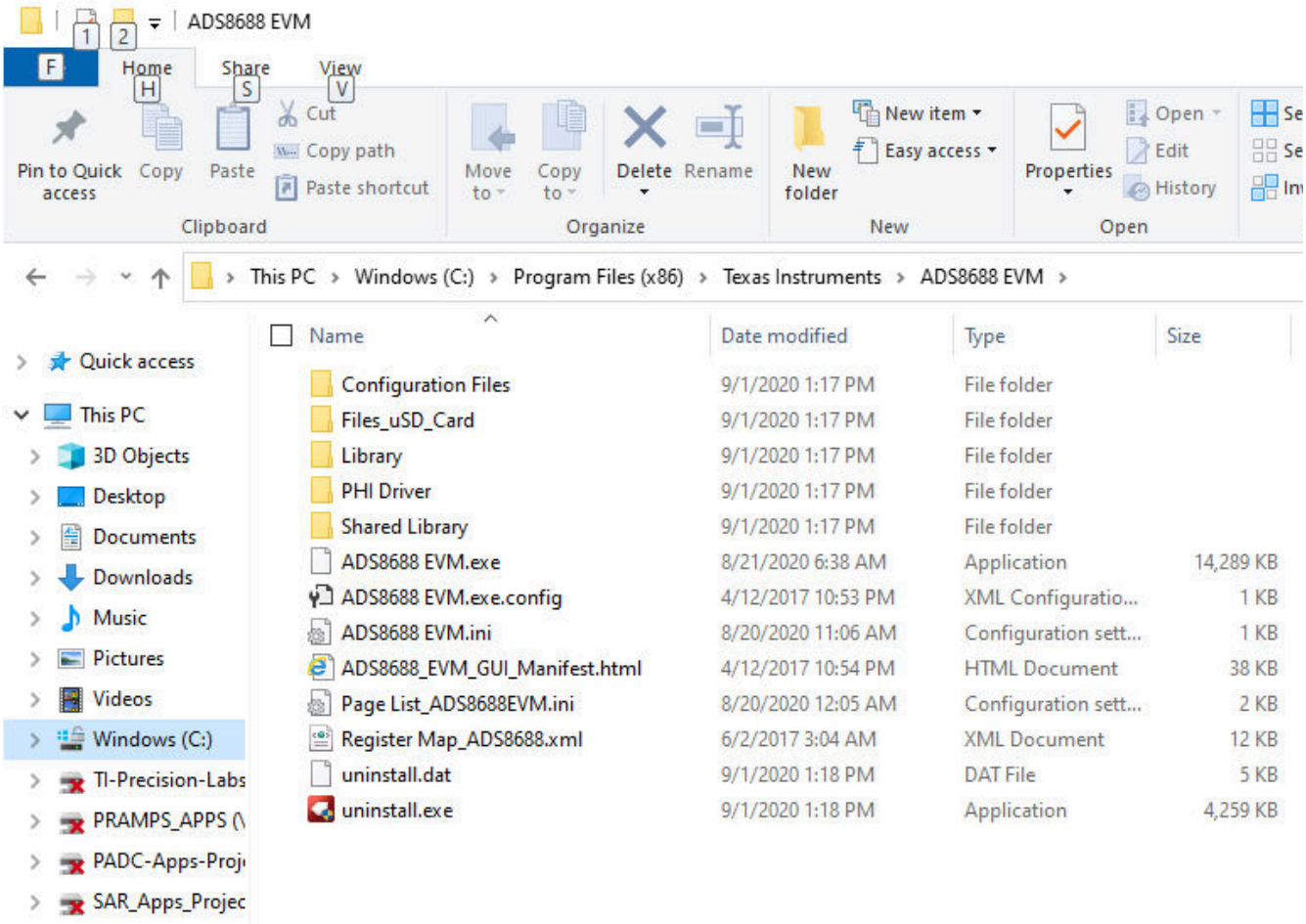

Figure 6-4. ADS8688EVM GUI Folder Post-Installation

7 EVM Operation

The following instructions are a step-by-step guide to connecting the ADS8688EVM to the computer and evaluating the performance of the ADS8688:

7.1 Connecting the Hardware

After installing the software connect the EVM as shown in Figure 7-1

1. Physically connect P2 of the PHI to J2 of the ADS8688EVM. Install the screws to assure a robust connection
2. Connect USB on PHI to the computer first
   - LED D5 on the PHI lights up, indicating that the PHI is powered up
   - LEDs D1 and D2 on the PHI start blinking to indicate that the PHI is booted up and communicating with the PC; Figure 7-1 shows the resulting LED indicators
3. Start the software GUI as shown in Figure 7-2. You will notice that the LEDs blink slowly as the FPGA firmware is loaded on the PHI. This will take a few seconds then the AVDD and DVDD power supplies will turn on.
4. Connect the signal generators to SMA inputs or headers (8 channels available). The input range is ±10.25V.

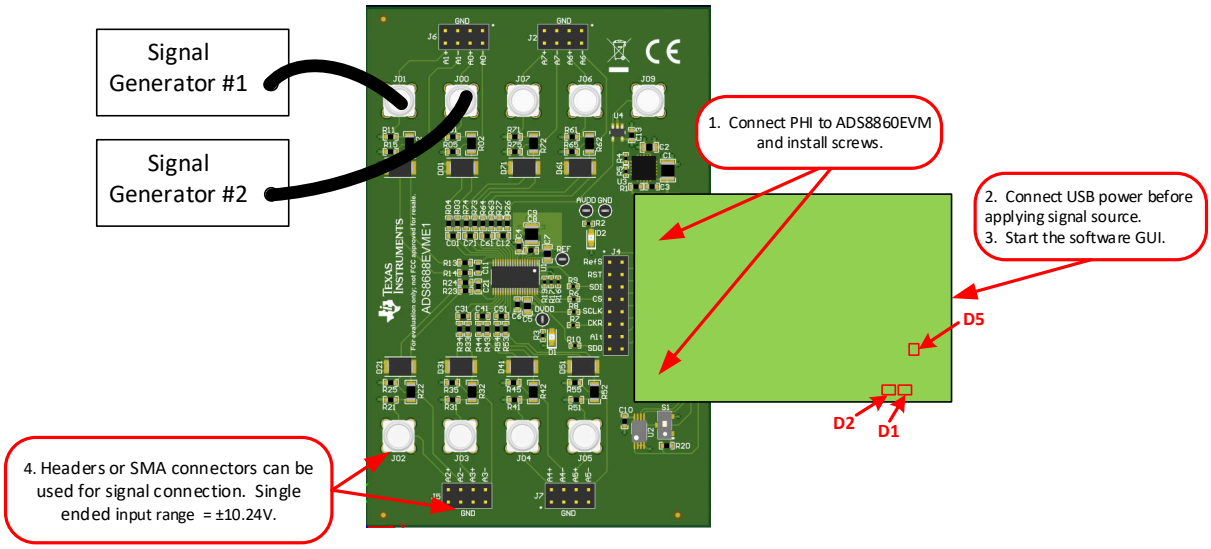

Figure 7-1. ADS8688EVM Hardware Setup and LED Indicators

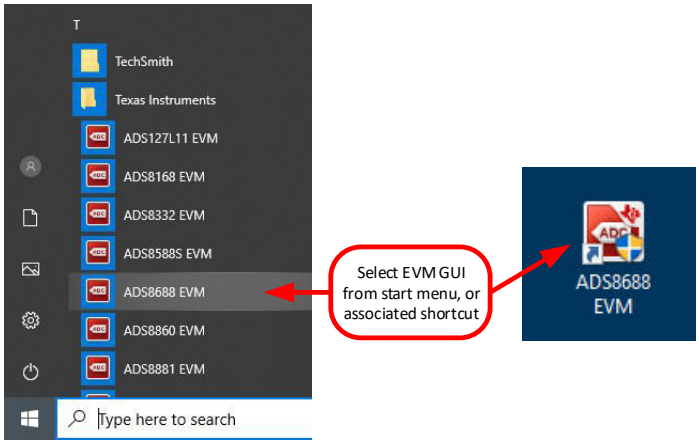

Figure 7-2. Launch the EVM GUI Software

7.2 Modifying Hardware and Using Software to Evaluate Other Devices in the Family

The ADS8688 is part of a family of related devices. This EVM hardware and software support the entire family because all the devices are pin-for-pin compatable. Table 7-1 lists other compatible devices in the family. The following procedure shows how to modify the hardware and software to evaluate the other devices in this family.

1. Desolder the ADS8688 and replace this device with the device you want to evaluate.
2. Enable the EEPROM for writing. This process is done by changing switch S2 to the top position using tweezers.Figure 7-3 details this process.
3. Connect the EVM and start the GUI as described in Section 7.1.
4. Use the *Tools* menu to *Load EEPROM* according to the device that is currently installed. When this procedure is successfully completed, you will see the status bar at the top of the software update according to the device installed on the hardware. For details, see Figure 7-4.

Table 7-1. Compatible Devices in the Family

Number of Channels	Resolution				
	12-Bit	14-Bit	16-Bit		18-Bit
4	ADS8664	ADS8674	ADS8684	ADS8684A	ADS8694
8	ADS8668	ADS8678	ADS8688	ADS8688A	ADS8698

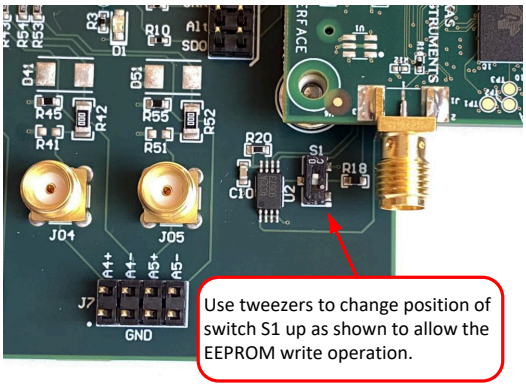

Figure 7-3. Enable EEPROM for Writing

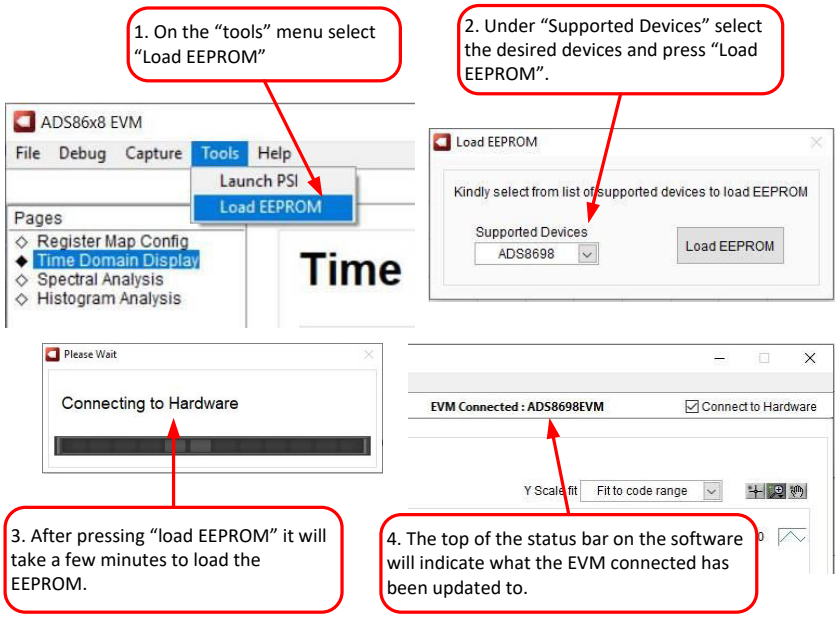

Figure 7-4. Configure EEPROM and Software for the New Device

7.3 EVM GUI Global Settings for ADC Control

Figure 7-5 shows that the EVM Global controls are located on the right hand side of the GUI. These controls choose the page display, SPI Mode, SCLK frequency, and sampling frequency.

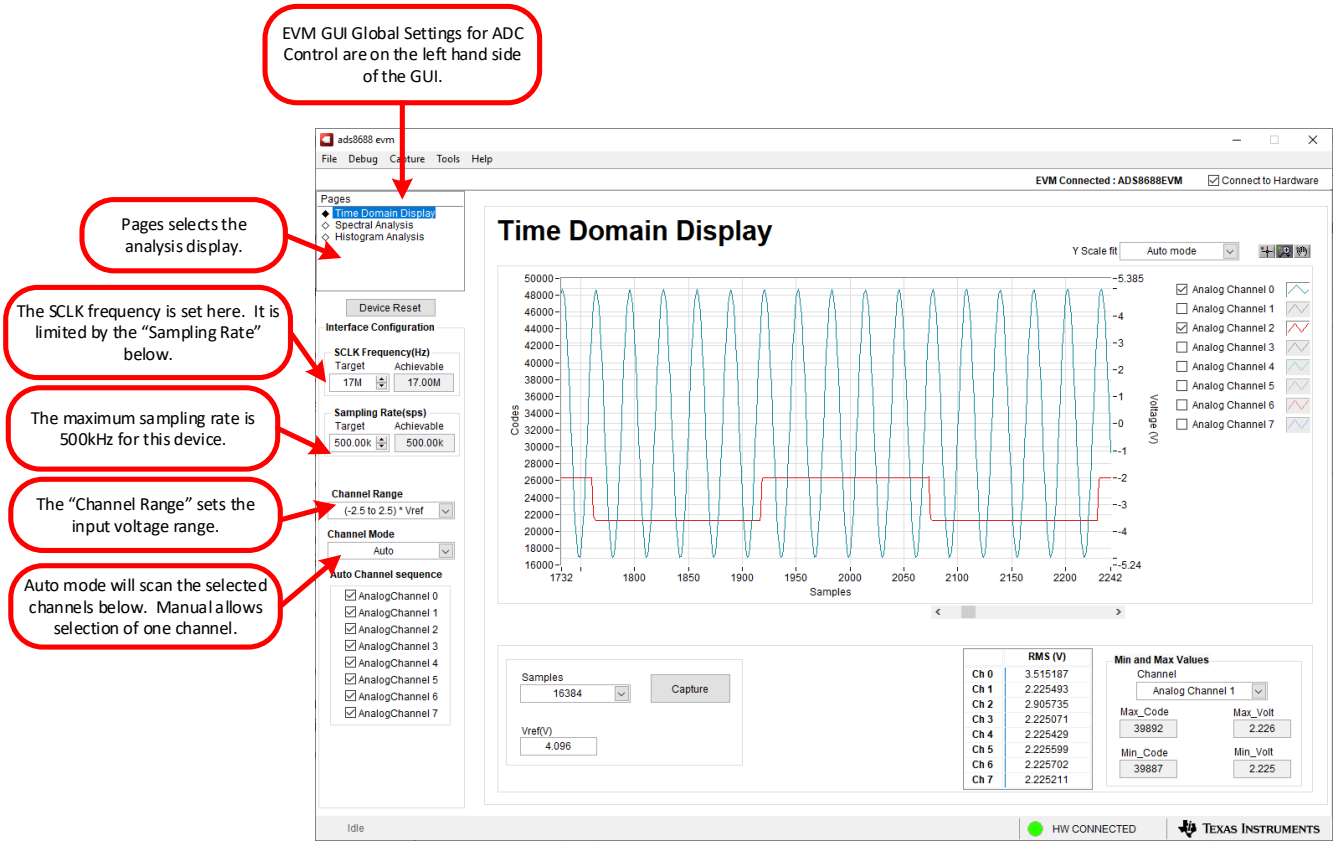

Figure 7-5. EVM GUI Global Input Controls

7.4 Time Domain Display

The time domain display tool allows visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or drive circuits. The user can trigger a capture of the data of the selected number of samples from the ADS8688EVM, as per the current interface mode settings indicated in Figure 7-6 by using the Capture button. The sample indices are on the x-axis and there are two y-axes showing the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the Analysis tools described in the subsequent sections causes calculations to be performed on the same set of data.

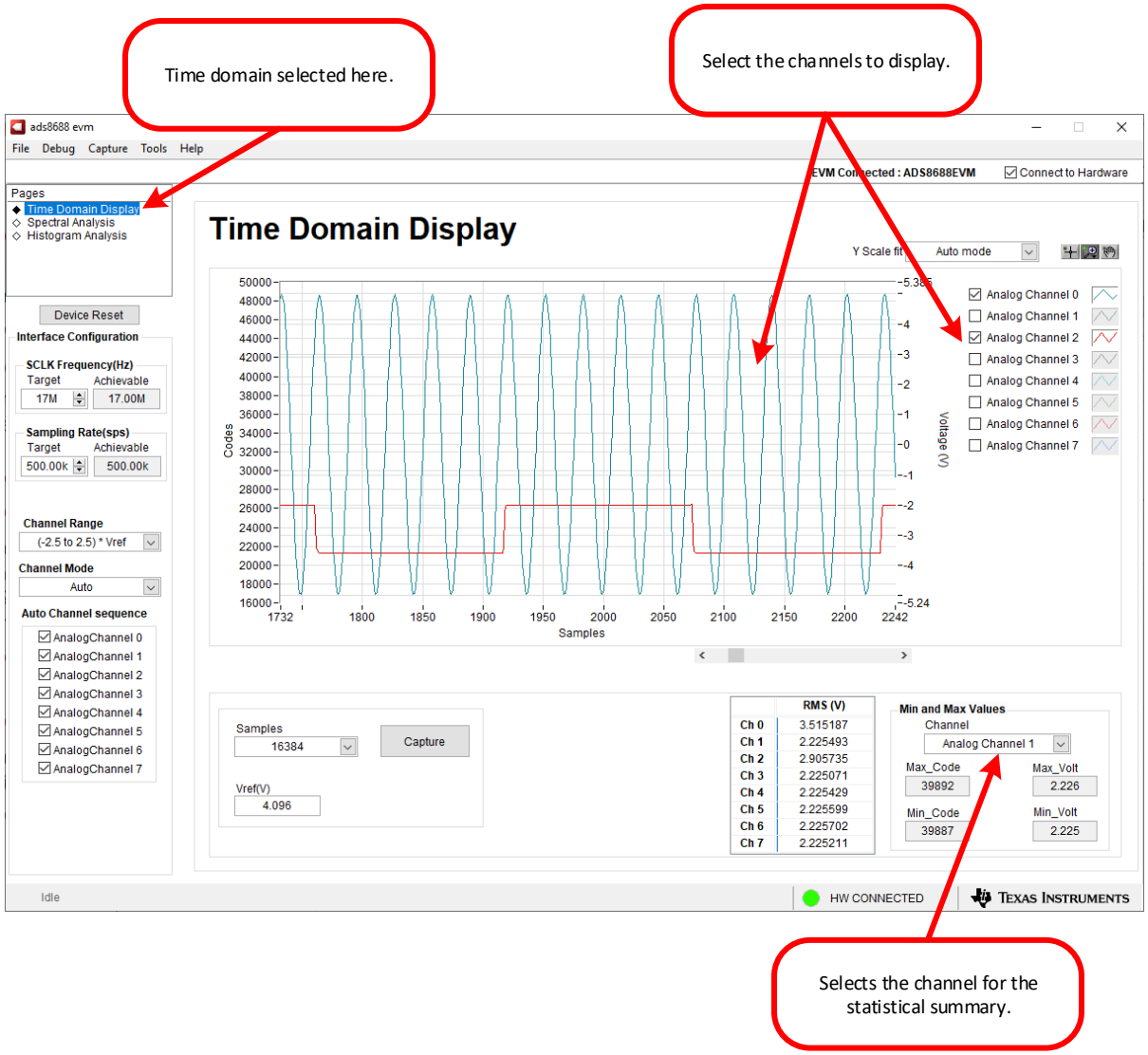

Figure 7-6. Time Domain Display Tool Options

7.5 Frequency Domain Display

The spectral analysis tool, shown in Figure 7-7, is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS8688 ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting. The FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-Term Blackman Harris window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. The None option corresponds to not using a window (or using a rectangular window) and is not recommended.

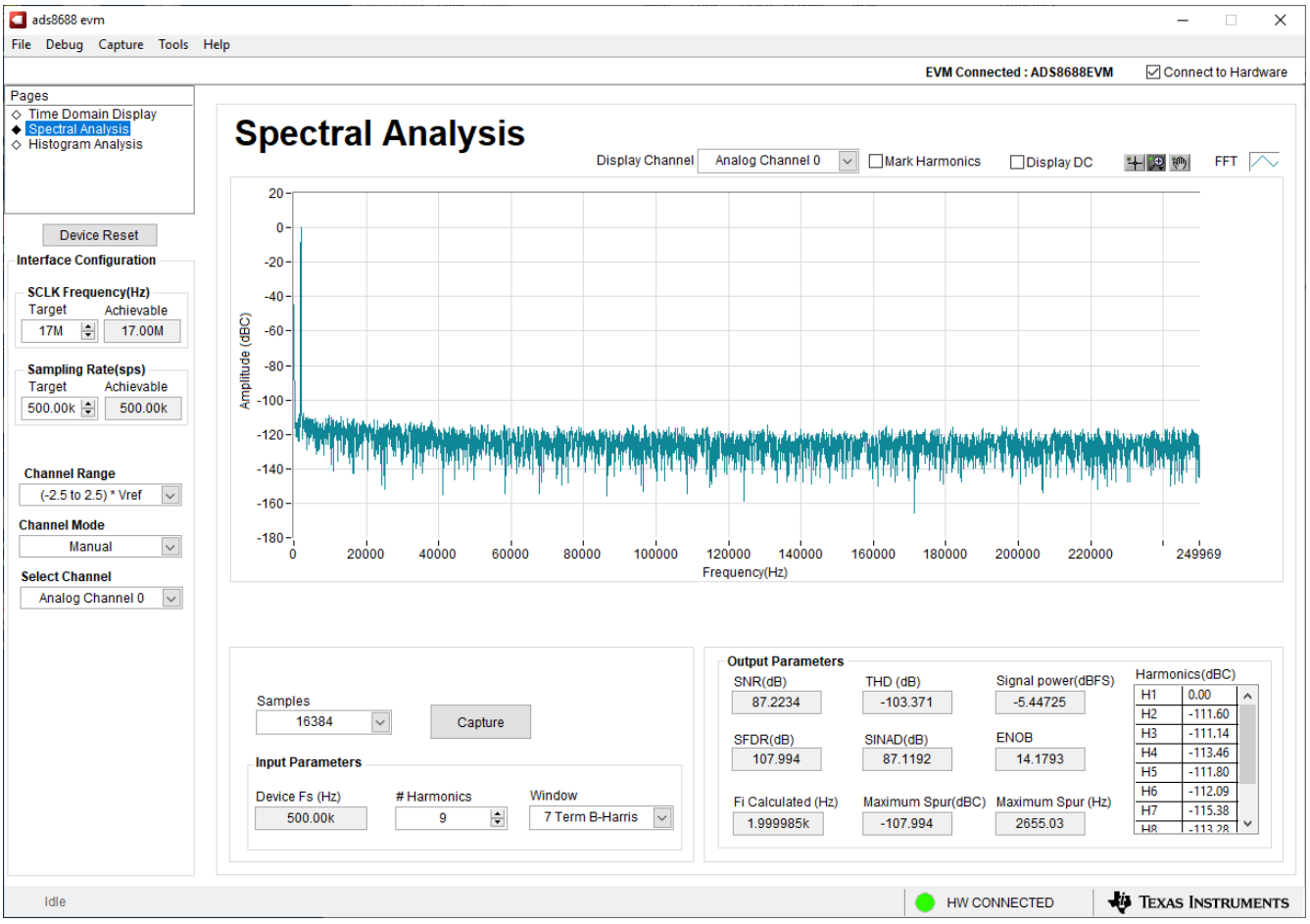

Figure 7-7. Spectral Analysis Tool

7.6 Histogram Display

Noise degrades ADC resolution and the histogram tool can be used to estimate effective resolution, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a DC input applied to a given channel. As shown in Figure 7-8, the histogram corresponding to a DC input is displayed on clicking the Capture button.

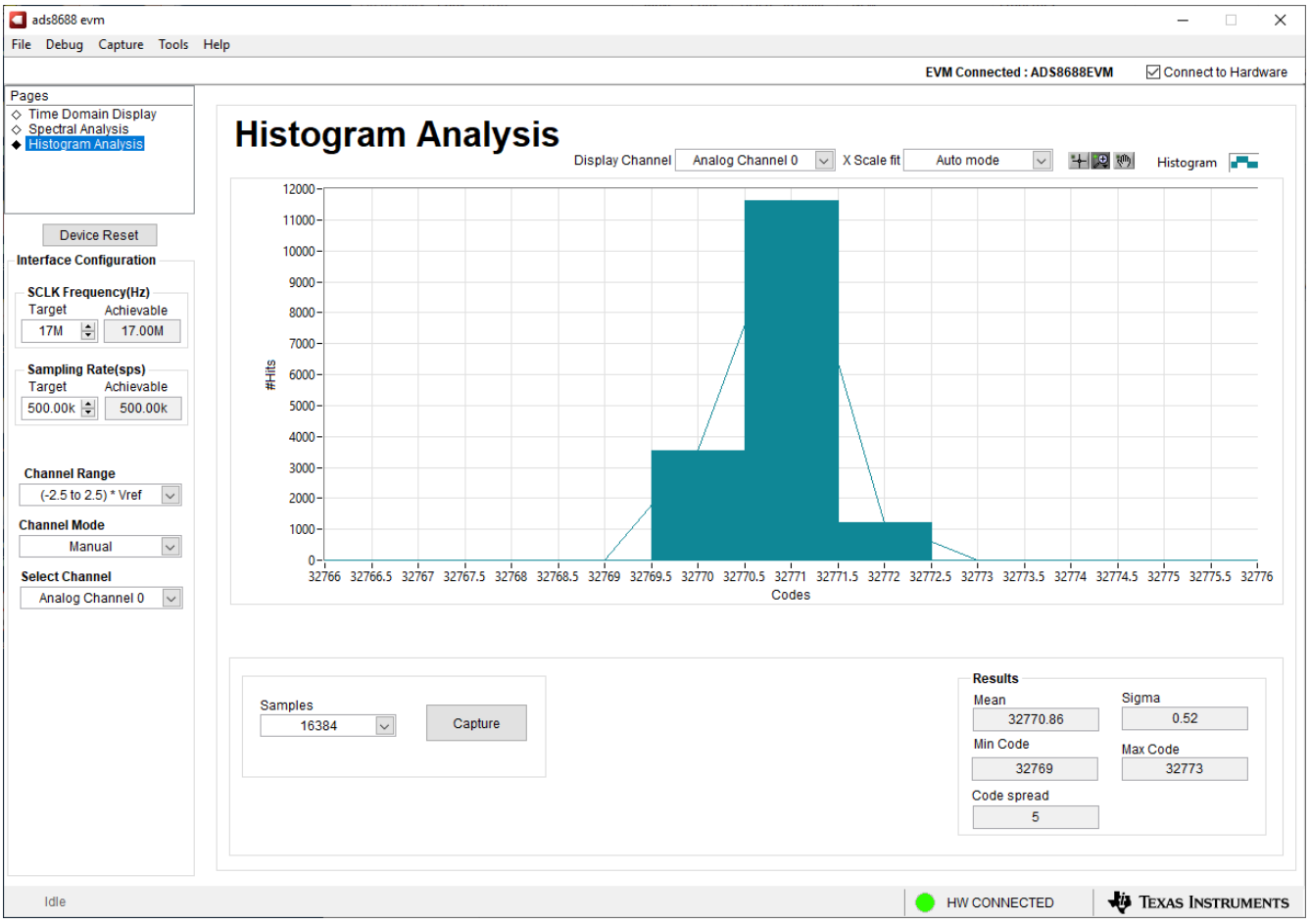

Figure 7-8. Histogram Analysis Tool

8 Bill of Materials, Schematics, and Layout

Schematics for the ADS8688EVM are appended to this user's guide. The bill of materials is provided in Table 8-1. Section 8.2 shows the PCB layouts for the ADS8688EVM.

8.1 Bill of Materials

Note

All components are compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, see www.ti.com.)

Table 8-1. ADS8688EVM Bill of Materials

Item #	Designator	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
1	!PCB1	1		ADS8688EVM	Any	Printed Circuit Board	
2	C1, C9	2	22uF	GRM32ER71E226KE15L	MuRata	CAP, CERM, 22 uF, 25 V, +/- 10%, X7R, 1210	1210
3	C01, C11, C12, C21, C31, C41, C51, C61, C71	9	1000pF	GRM1885C1H102FA01J	MuRata	CAP, CERM, 1000 pF, 50 V, +/- 1%, C0G/NP0, 0603	0603
4	C2, C5, C7	3	10uF	CL21A106KAFN3NE	Samsung Electro-Mechanics	CAP, CERM, 10 uF, 25 V, +/- 10%, X5R, 0805	0805
5	C3, C4, C6, C8	4	1uF	C0603C105K3RACTU	Kemet	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	0603
6	C10, C13	2	0.1uF	GRM188R71H104KA93D	MuRata	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	0603
7	D1, D2	2	Green	APT2012LZGCK	Kingbright	LED, Green, SMD	LED_0805
8	H1, H2	2		RM3X4MM 2701	APM HEXSEAL	Machine Screw Pan PHILLIPS M3	
9	H3, H4, H5, H6	4		SJ-5303 (CLEAR)	3M	Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon
10	H7, H8	2		9774050360R	Wurth Elektronik	ROUND STANDOFF M3 STEEL 5MM	ROUND STANDOFF M3 STEEL 5MM
11	J00, J01, J02, J03, J04, J05, J06, J07, J09	9		5-1814832-1	TE Connectivity	SMA Straight PCB Socket Die Cast, 50 Ohm, TH	SMA Straight PCB Socket Die Cast, TH
12	J2, J5, J6, J7	4		TSW-104-07-G-D	Samtec	Header, 100mil, 4x2, Gold, TH	4x2 Header
13	J3	1		QTH-030-01-L-D-A-K-TR	Samtec	Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT
14	J4	1		TSW-108-07-G-D	Samtec	Header, 100mil, 8x2, Gold, TH	8x2 Header
15	R1	1	100k	CRCW0603100KFKEA	Vishay-Dale	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603
16	R2, R3	2	6.65k	CRCW04026K65FKED	Vishay-Dale	RES, 6.65 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402

Table 8-1. ADS8688EVM Bill of Materials (continued)

Item #	Designator	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
17	R02, R12, R22, R32, R42, R52, R62, R72	8	0	ERJ-8GEY0R00V	Panasonic	RES, 0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	1206
18	R03, R04, R13, R14, R23, R24, R33, R34, R43, R44, R53, R54, R63, R64, R73, R74	16	1.00k	RG1608P-102-B-T5	Susumu Co Ltd	RES, 1.00 k, 0.1%, 0.1 W, 0603	0603
19	R4, R5	2	0	RC0402JR-070RL	Yageo America	RES, 0, 5%, 0.063 W, 0402	0402
20	R05, R15, R18, R25, R35, R45, R55, R65, R75	9	0	CRCW06030000Z0EA	Vishay-Dale	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603
21	R6, R7, R8, R9, R10	5	49.9	CRCW040249R9FKED	Vishay-Dale	RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
22	R16, R17, R19	3	47.0k	RC0402FR-0747KL	Yageo America	RES, 47.0 k, 1%, 0.0625 W, 0402	0402
23	R20	1	10.0k	RC0603FR-0710KL	Yageo	RES, 10.0 k, 1%, 0.1 W, 0603	0603
24	R26, R27	2	49.9	RC0603FR-0749R9L	Yageo	RES, 49.9, 1%, 0.1 W, 0603	0603
25	S1	1		CAS-120TA	Copal Electronics	Switch, Slide, SPDT 100mA, SMT	Switch, 5.4x2.5x2.5mm
26	TP1, TP2, TP3, TP4	4		5001	Keystone	Test Point, Miniature, Black, TH	Black Miniature Testpoint
27	U1	1		ADS8688IDBT	Texas Instruments	16-Bit, 500-kSPS, 8-Channel, Single-Supply, SAR ADCs with Bipolar Input Ranges, DBT0038A (TSSOP-38)	DBT0038A
28	U2	1		BR24G32FVT-3AGE2	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8
29	U3	1		TPS7A4700RGWR	Texas Instruments	36V, 1A, 4.17μVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)	RGW0020A
30	U4	1		OPA320AIDBVR	Texas Instruments	Precision, 20 MHz, 0.9 pA Ib, RRIO, CMOS Operational Amplifier, 1.8 to 5.5 V, -40 to 125 degC, 5-pin SOT23 (DBV5), Green (RoHS & no Sb/Br)	DBV0005A
31	D01, D11, D21, D31, D41, D51, D61, D71	0	14V	SMBJ14CA	Littelfuse	Diode, TVS, Bi, 14 V, SMB	SMB
32	FID1, FID2, FID3	0		N/A	N/A	Fiducial mark. There is nothing to buy or mount.	N/A
33	R01, R11, R21, R31, R41, R51, R61, R71	0	49.9k	CRCW060349K9FKEA	Vishay-Dale	RES, 49.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603

8.2 Board Layout

Figure 8-1 shows the PCB layout for the ADS8688EVM.

Note

The board layouts is not to scale. This figure is intended to show how the board is laid out and is not intended to be used for manufacturing ADS8688EVM PCBs.

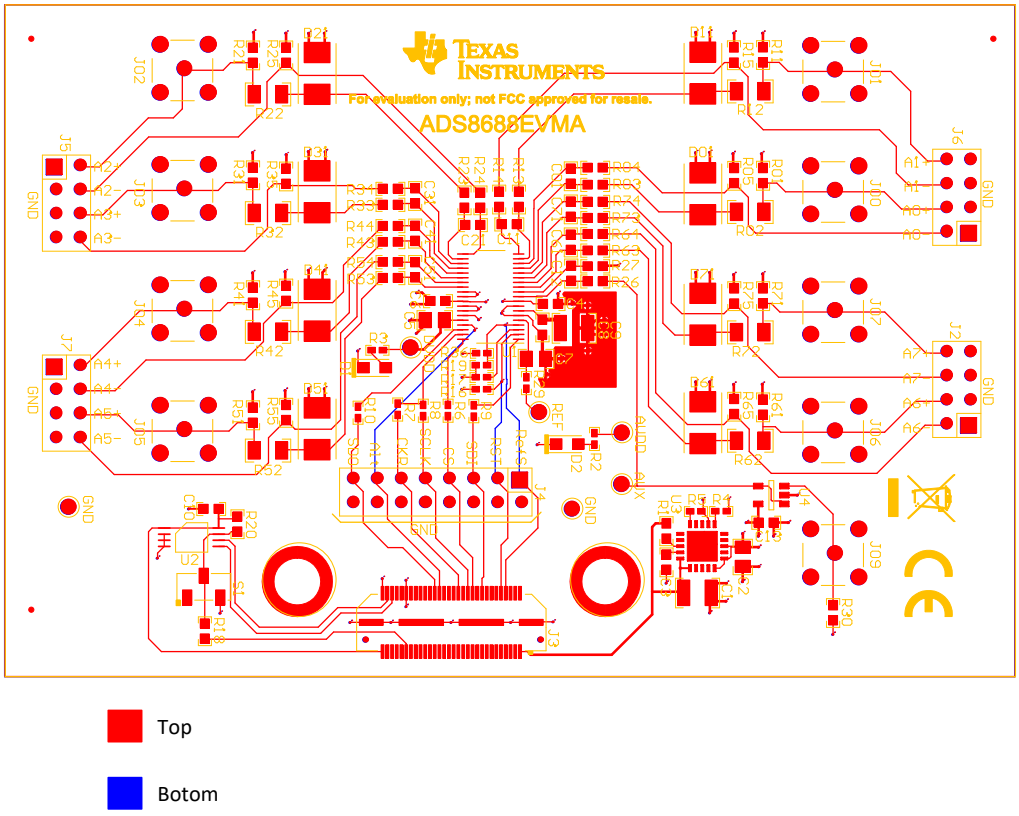

Figure 8-1. ADS8688EVM PCB

8.3 Schematic

Figure 8-2 shows the input filter, terminal block, and SMA connections.

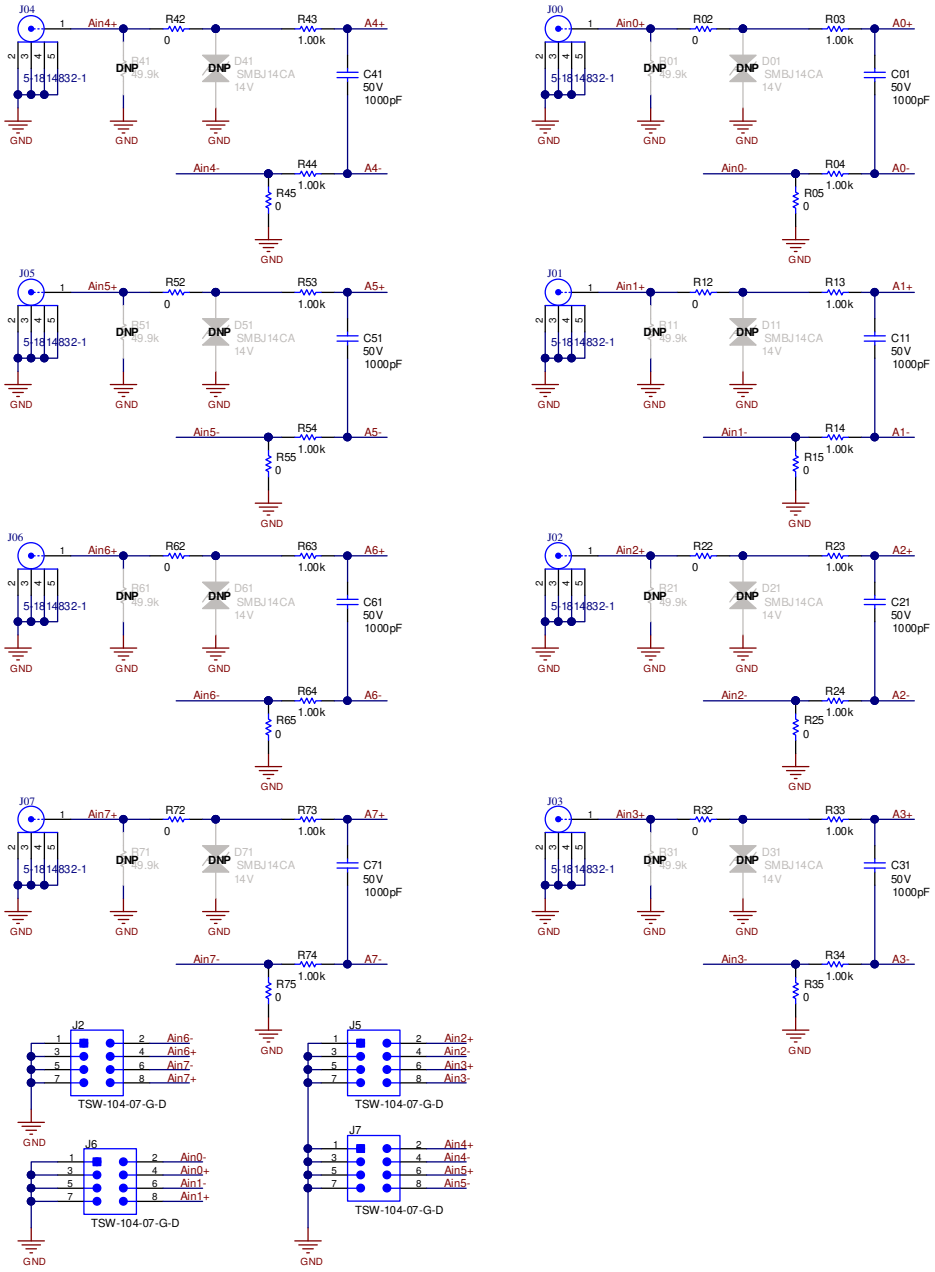

Figure 8-2. Input Filter

Figure 8-3 shows the input filter, terminal block, and SMA connections.

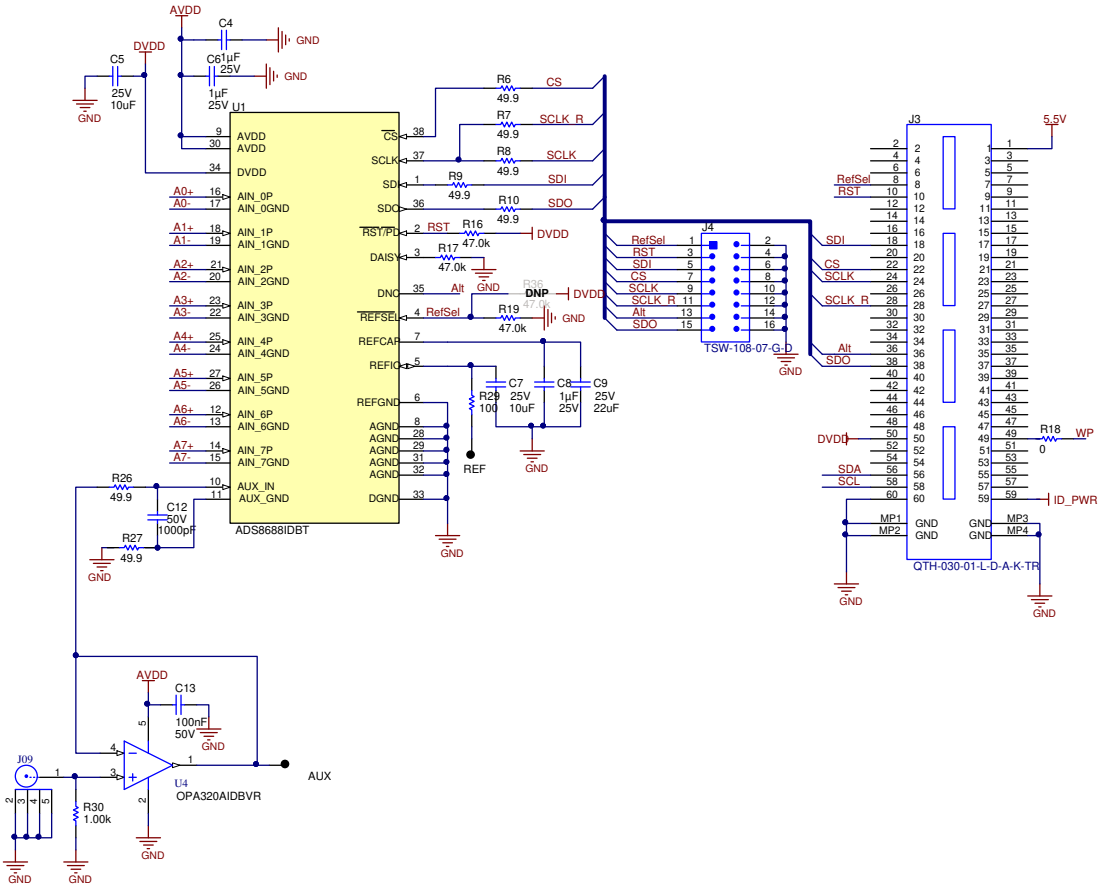

Figure 8-3. ADC and Digital Interface

Figure 8-4 shows power and EEPROM connections.

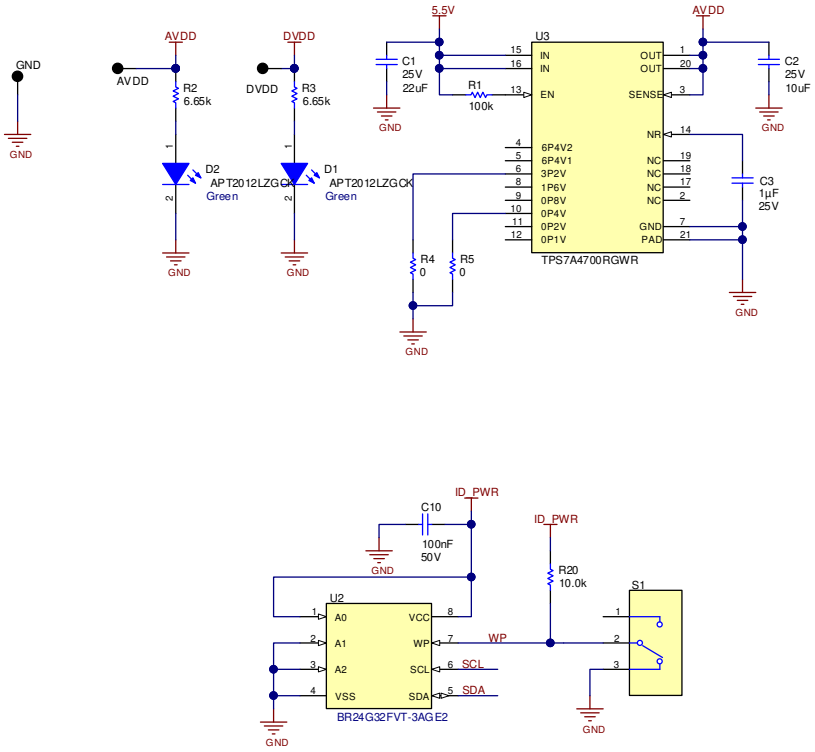

Figure 8-4. Power and EEPROM

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2020) to Revision C (March 2021)	Page
• Changed *ADS8688EVM-PDK* figure	1
• Updated the numbering format for tables, figures and cross-references throughout the document	3
• Changed *Voltage Reference, Aux Input, and Supply Decoupling* figure	5
• Added *Modifying Hardware and Using Software to Evaluate Other Devices in the Family* section	12
• Changed *Board Layouts* section to show a PCB layer image instead of a top and a bottom image	19
• Changed *ADC and Digital Interface* figure	20

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