Application Brief

PLC Analog Input Front-End Architectures

Analog input (AIN) modules are the most diversified among PLC modules. The current market trend is quite demanding when it comes to AIN: high channel count is required at small footprint, high precision is required at lowest cost, high-speed conversion and high accuracy at low power. More features and programmability come in combination with higher reliability and extended diagnostic features.

Trying to cope with such demands requires a good overview of the different performance specifications of AIN modules. Figure 1 lists and classifies AIN specifications into different classes according to which aspect of performance they relate.

Input Signal

- Input Type: I, V, R, RTD, TC, …
- Input Range
  - V: 0-5 V, 0-10 V, ±5 V, ±10 V
  - I : 4-20 mA, 0-20 mA, ±20 mA
- Common Mode Range: e.g. ±30
- Maximum Current (I)
- HART Support (I)

Interface

- Connection: 2/3 Terminal
- Single-ended / differential input
- Number of Channels: 1,2,4,8,16
- Input Resistance (V)
- Burden Resistance (I)
- Channel/Group Isolation

Accuracy

- Offset/Gain/Linearity Error
- Thermal Deviation
- Total Unadjusted Error (TUE)

Precision

- Resolution (Quantization Error)
- Noise Error, ENOB, Repeat Accuracy
- 50/60/400 Hz rejection
- Common Mode Rejection
- Channel to Channel Crosstalk

Speed

- Conversion time (per channel)
- Scan time (all channels)
- Bandwidth and Settling time
- Oversampling, Averaging, timestamp

Reliability and Protection

- Operating Temperature Range
- Isolation Voltage
- Overvoltage input protection
- Surge protection
- Reverse Polarity (I)
- Supply OV/UV
- Supply reverse polarity

Diagnostics and Fault Detection

- Broken Wire
- Short Circuit
- Over Temperature
- Voltage Over-range
- No Supply Voltage
- Common Mode Error

Figure 1. AIN Module Specification

The large number of specifications and the diversity of the module applications cannot be addressed by a single architecture. That is why many AIN module implementations achieve optimum cost per given target performance.

To have a common ground of architectural exploration, some parameters are fixed throughout this document. This product overview addresses:

- Voltage or current only modules
- Modules with 8 channels
- Differential input (with single-ended described as a subset)
- High-input impedance

This approach leaves less parameters to consider and reduces the number of variations.

Analog Input Module Structure

The *Analog input module end-equipment* application page on www.ti.com provides a rich source of information about TI solutions for PLC analog input. The page supports the generic structure of the AIN module as shown Figure 2.

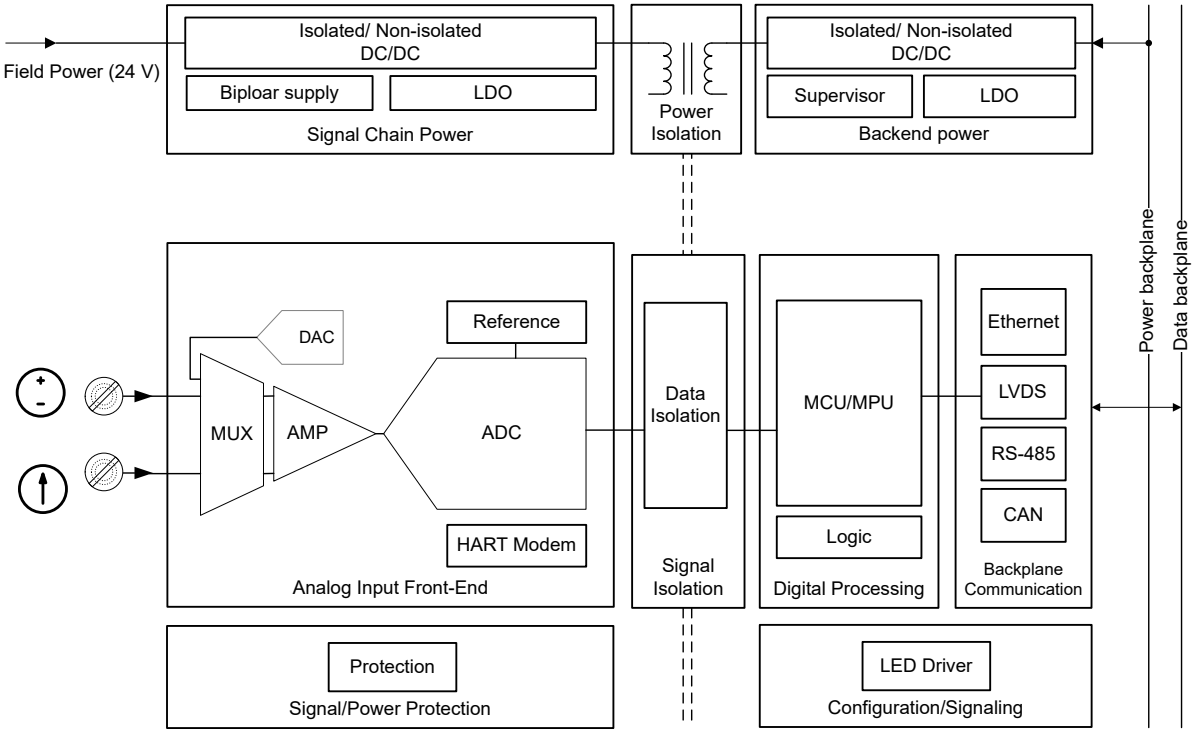

Figure 2. Analog Input Module Structure

This document focuses on the fact that the differences between AIN modules lies mainly in the analog front-end subsystem.

Resolution and **conversion time** are the two basic specifications that generally determine the choice of AIN architecture. The resolution refers to the number of distinguished analog input levels represented as ADC codes, and conversion time is the time required to convert a single channel into digital code. Resolution and conversion time essentially determine the core device in the front-end, namely the analog-to-digital converter (ADC).

Cycle time is another important specification of AIN modules. Cycle time refers to the time required to convert all input channels. If the channels are converted sequentially (like in multiplexed systems), the cycle time equals the number of channels multiplied by the conversion time (tCycle = N × tConv; where N is the number of channels). If the channels are converted in parallel (like in simultaneous-sampling (**simsam**) systems), then (tCycle = tConv).

How Fast Should the ADC for the AIN Module be?

Typical industrial and process signals sampled by the analog input modules are slow in nature with limited bandwidth. Some inputs like pressure can experience fast transitions and these transitions need to be captured by the controller, in those cases a wider bandwidth can be defined. Although input bandwidth is generally limited, this is deceptive causing the designer to think that ADCs are slow. The large number of channels and the averaging requirements can call for a higher ADC sampling rate.

Consider an example where a designer wants to select a single-channel ADC for a multiplexed, 8-channel AIN module. Assume no averaging is required, and a channel bandwidth of only 2 kHz, so 4 kSPS per channel is required. Because there are 8 channels in sequence, a higher sampling rate (throughput) is needed from the

ADC with a minimum of 32 kSPS. The conversion time per channel (tConv = 1 / 32 kSPS) = 31.25 µs). Note that the cycle time in this case is tCycle = 8 × tConv = 252 µs.

This example illustrate that starting with a humble requirement of 2-kHz bandwidth per channel ended up in requiring an ADC throughput of 32 kSPS, and 31.25 µs of conversion time. If higher bandwidth, or more samples per channels are required for averaging, the throughput requirement of the ADC increases.

Multichannel Front-End Architectures

There are essentially four different architectures for the multichannel analog front-end of an analog input module. These modules differ in how high a common-mode voltage they can support, and how many ADC cores they have, as well as their level of integration.

1. **Channel-Channel** isolated architecture supports the highest common-mode voltage range among all architectures. However, channel-channel requires separate front-end, ADC, isolated power, and signal isolation per channel, resulting in higher cost, and typically larger area.
2. **Simultaneous-sampling** (simsam) ADC achieves the shortest cycle-time among all architectures. Simsam is also essential when synchronization between channels is needed like sampling the 3 phases of a power line or 3 axes of vibration sensor.
3. **Multichannel ADC with Integrated MUX**: this module is usually the optimum cost for certain performance. Multichannel ADC with Integrated MUX typically enables faster scan time compared to external MUX architecture.
4. **External MUX** can be the lowest-cost multichannel design also offering some flexibility in device selection. Figure 3 shows how this architecture needs more design effort, the MUX and driver outputs experience very large transients, so the settling time is the limiting factor of the conversion time of such architecture.

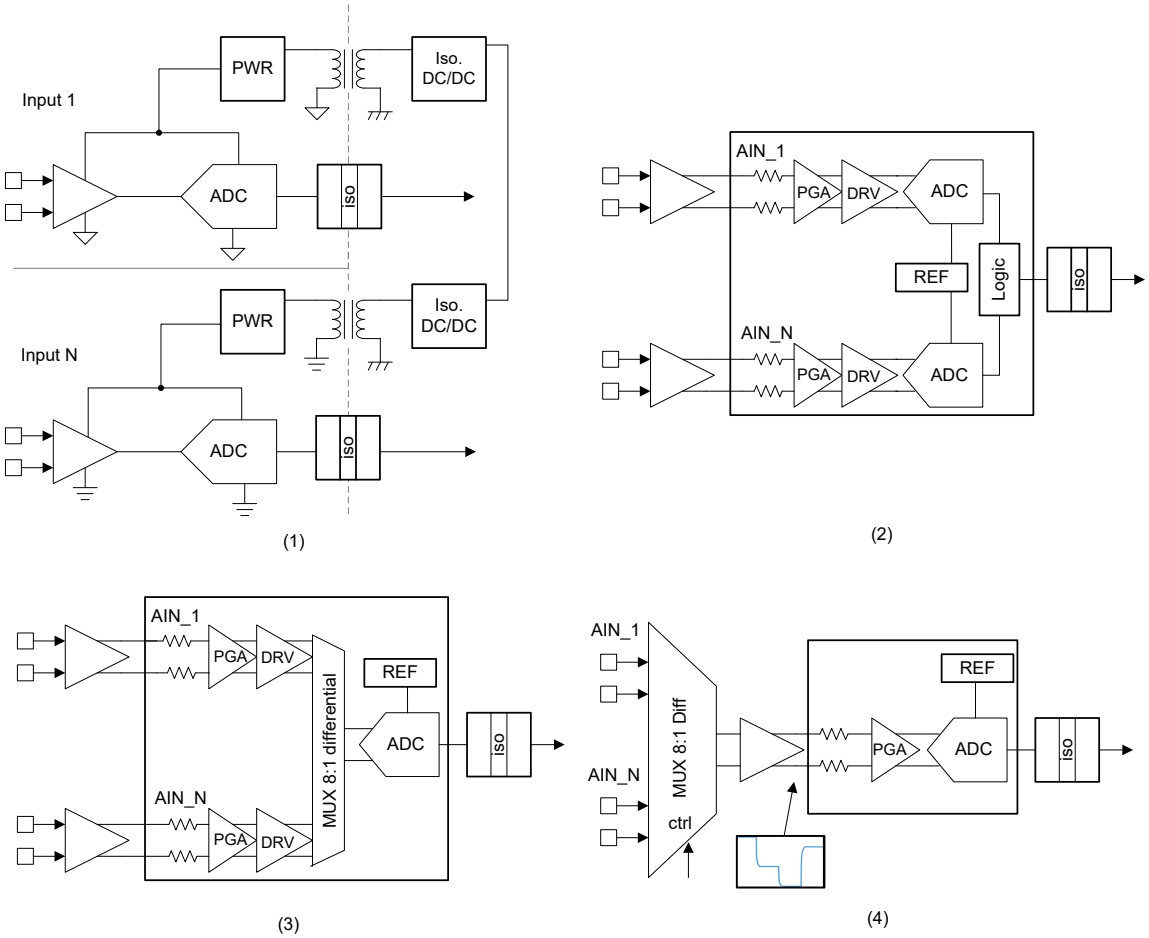

Figure 3. Multichannel Front-End Types

Table 1 summarizes the main differences between those architectures.

Table 1. Architecture Comparison

	Channel-Channel Isolated	Simsam	Integrated MUX	External MUX
Common-Mode Voltage Range	Very high	Moderate	Moderate	Moderate
Isolation	> 500-V isolation between channels	No isolation between channels	No isolation between channels	No isolation between channels
Input Amplifiers	If required, one per channel	If required, one per channel	If required, one per channel	Only one after MUX
ADC	Single channel, more choices	High sampling rate ADC	High sampling rate ADC	Single channel, high sampling rate
Cost	Highest cost/area AFE/ADC/ power per channel	High cost	Medium cost	Low cost
Benefits	Highest isolation, and reliability	Very short cycle time. Synchronous	Premium cost and performance	Lost cost, and power. Flexible

Multiplexed Architectures

This product overview focuses on the multiplexed architectures. Multiplexed architectures present the majority of the PLC input modules. For the sake of simplicity, this document considers high-input impedance types of modules and first discusses differential inputs and later refers to corresponding single-ended front-end.

Figure 4 shows different architecture on two orthogonal scales, one for resolution (12 bits to 24 bits), and the other for conversion time (200 µs conversion time down to 2 µs). The designs can be clustered into medium resolution (up to 16 bits) implemented using successive approximation register (SAR) ADCs, and high resolution (between 16 and 24 bits) relying mostly on DS ADCs.

Each group of designs (medium or high resolution) can be further divided according to the conversion time as Figure 4 shows. Each architecture is indicated by a reference number (1 to 8) discussed in Architecture 1: Single-Ended, High-Voltage SAR through Architecture 8: Simsam Delta Sigma.

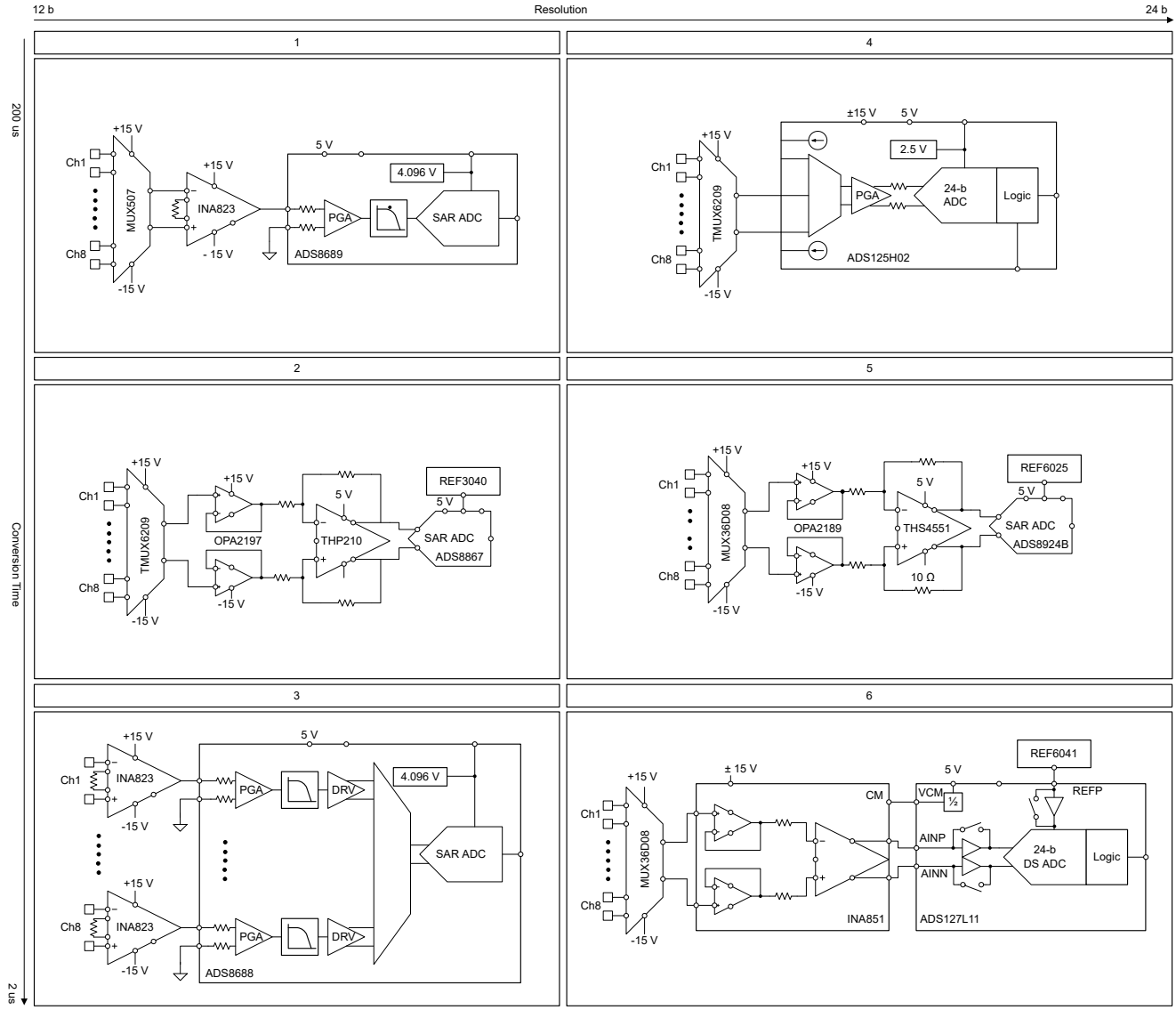

Figure 4. Multiplexed Architectures Selection Diagram

Architecture 1: Single-Ended, High-Voltage SAR

The first architecture is based on the high-voltage input 100-kSPS SAR ADS8689, which integrates a programmable gain amplifier (PGA) and a voltage reference. The ADC is single-ended with 1-MΩ input impedance so a precision instrumentation amplifier (INA) is used to convert the differential input signal to a single-ended output signal, and provide high-input impedance. A low-leakage differential MUX507 precedes the INA to support 8 channels. No input scaling is needed because the ADS8689 can support up to ±12-V inputs directly.

The settling time of both the INA and the integrated PGA/filter makes this architecture an excellent choice for a minimum conversion time of 80 µs to 120 µs according to the resolution required. The higher sampling rate of the ADS8681 or ADS8685 devices can improve noise performance through averaging.

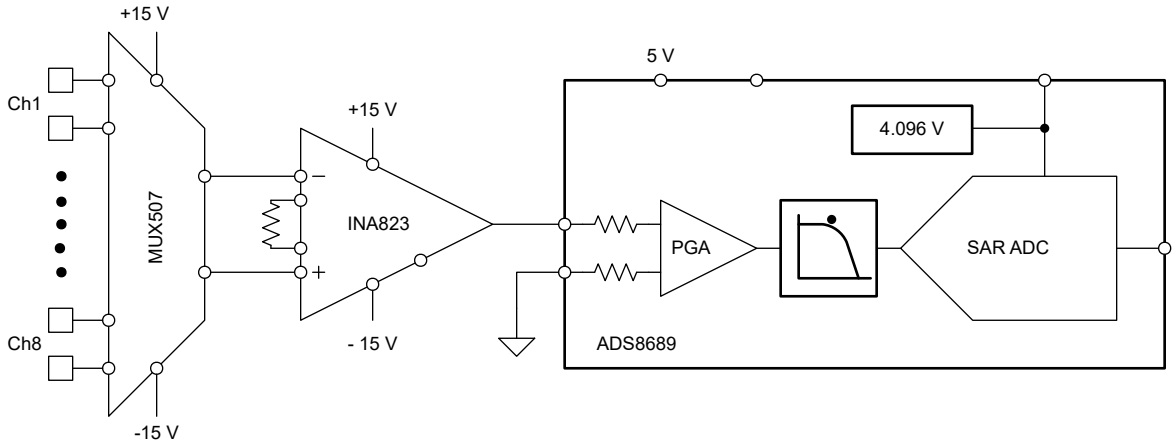

Figure 5. Architecture 1

An alternative to the INA823 is the INA188 device, which offers lower noise and offset error at the expense of lower bandwidth and higher I_Q. The criteria for selecting the INA is low offset and gain drift, high CMRR, low noise, high slew-rate, and bandwidth.

Table 2. INA823 and INA188 Comparison

AMP	Noise 1-kHz (nV/√Hz)	V_{OS} (µV)	Drift (µV/C)	I_Q (mA)	Bandwidth (MHz)	Features
INA823	21	100	1.2	0.18	1.9	Overvoltage protection
INA188	12.5	55	0.2	1.4	0.6	Zero drift

The ADS86xx is a single-input ADC with resolution from 12 to 18 bits and sampling speeds from 100 kSPS to 1 MSPS, which gives great flexibility in system implementation. Note that the higher sampling frequency does not improve the conversion time, but higher sampling speed can be used to average multiple samples per channel and improve the effective number of bits (ENOB).

In multiplexed SAR architecture, two factors are crucial to determine the shortest achievable conversion time: (1) the settling time of the front-end including any amplifiers to the required accuracy, and (2) the settling time of the ADC input buffer, especially if the buffer has limited bandwidth. Both factors dominate the final speed rather than the ADC throughput capability.

Table 3. Device Comparison

SPS	12b	14b	16b	18b
100k			ADS8689	ADS8699
500k	ADS8665	ADS8675	ADS8685	ADS8695
1M	ADS8661	ADS8671	ADS8681	ADS8691

Regarding number of channels, other MUX options can be used for 4 channels. There is also the option to use fault-protected MUX to simplify input protection. The criteria for selecting a MUX is low off-state leakage < 0.2 µA to keep input impedance high, low on-state leakage to reduce error for current measurements, low cross-talk, and low output capacitance to reduce settling time.

Table 4. Differential MUX Selection

# Channels	36 V	> 36 V and Protected
4	TMUX6209, MUX36D04, MUX509	TMUX7309F, TMUX8109
8	MUX36D08, MUX507	

For modules with single-ended inputs, a single-ended MUX followed by an amplifier is required. The amplifier must have a high slew rate to support fast-settling, as well as relatively low offset-drift to reduce errors. The following list shows the amplifiers that fulfill these requirements:

- OPA145
- OPA172
- OPA182
- OPA189
- OPA196
- OPA197
- OPA991
- OPA992

Regarding MUX selection, Table 5 shows the available options for single-ended front-end designs.

Table 5. Single-Ended MUX Selection

# Channels	36 V	> 36 V and Protected
4	TMUX6104	TMUX7309F, TMUX8109
8	TMUX6208, MUX36S08, MUX508	TMUX7208, TMUX7308F, TMUX8108
16	MUX36S16, MUX506	

For detailed design schematics and performance of such architecture, see the *Cost-Optimized, High-Performance Front-End Design for Analog Input Modules* application note.

Architecture 2: Differential, Low-Voltage SAR

To achieve a shorter conversion time, the ADS886x family of differential SAR is selected. The ADC does not have an input filter, so this ADC can achieve a short settling time. This architecture requires an external voltage reference (for example, REF3040) and fully differential driver (for example, THP210). The differential driver has no high-impedance input, so op-amp buffers (for example, OPA2197) are used in front of the driver. The differential MUX TMUX6209 enables 8-channel input when two are used in parallel.

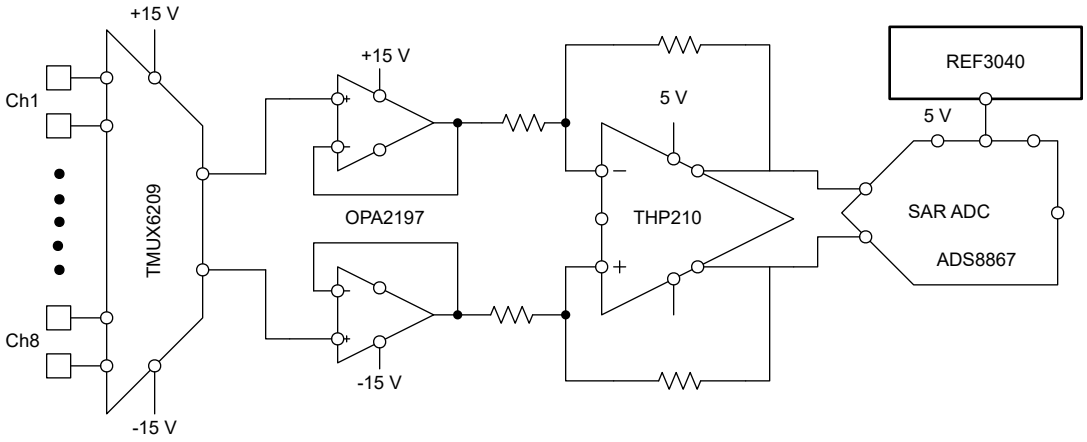

Figure 6. Architecture 2

The ADS88xx family includes devices of 16 and 18 bits, and sample rates up to 1 MSPS, as Table 6 shows.

Table 6. ADS88xx Family Characteristics

SPS	100 kSPS	400 kSPS	680 kSPS	1 MSPS
16b	ADS8867	ADS8865	ADS8863	ADS8861
18b	ADS8887	ADS8885	ADS8883	ADS8881

This device family works over the temperature span of –40°C to 85°C.

Other amplifier options are shown in Table 7. Note that lower drift generally comes with higher current consumption.

Table 7. Buffer Amplifier Options Comparison

AMP	Noise 1-kHz (nV/$\sqrt{Hz}$)	V_{OS} (µV)	Drift (µV/C)	I_Q (mA)	Bandwidth (MHz)	Slew Rate (V/µs)
OPA2197	5.5	100	0.5	1.3	10	20
OPA2145	7.5	150	0.5	0.47	5.5	20
OPA2189	5.8	2.5	0.0035	1.7	14	20

The REF30xx family of voltage references also offers 2.5 V (REF3025) and 3.3 V (REF3033) if the signal chain requires those levels instead of 4.096 V offered by REF3040.

The TIPD151 reference design demonstrates such architecture and the TIPD169 is another example for the single-ended implementation.

Architecture 3: Integrated-Multiplexer SAR

The shortest conversion time using a SAR ADC can be achieved by choosing a device with an integrated multiplexer: ADS8688, a 16-bit, 500-kSPS, 8-channel SAR ADC with ±10-V input. For differential inputs, INA823 or INA188 can be used as high-impedance differential-to-single-ended converter at a gain of 1.

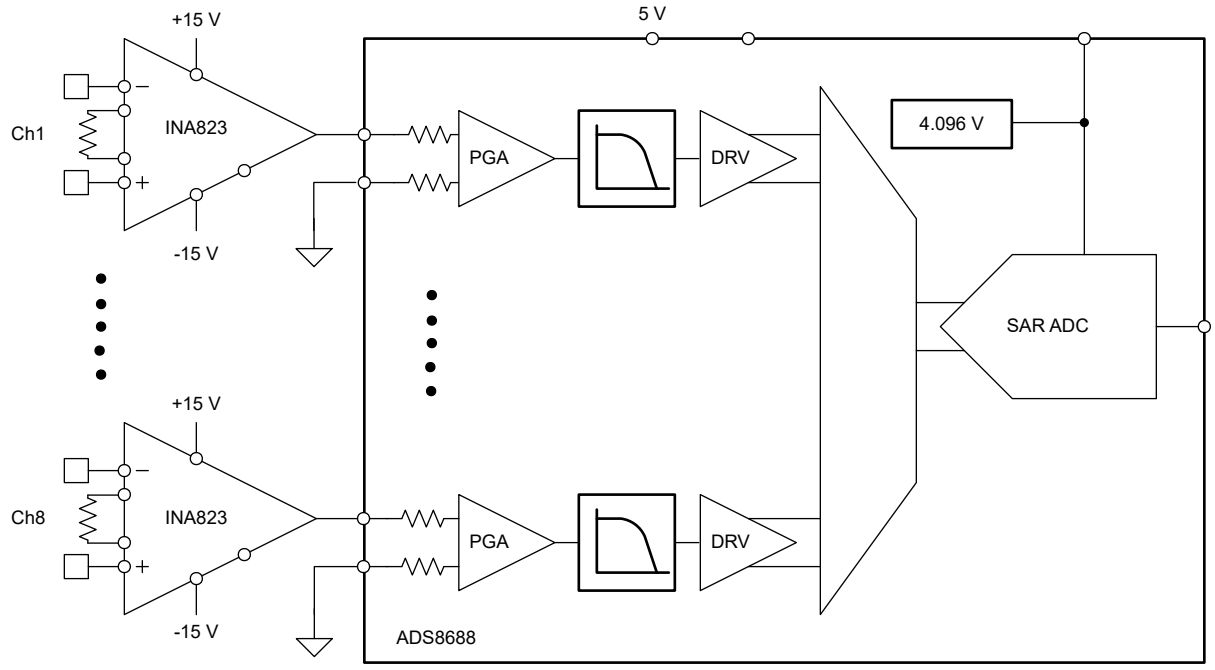

Figure 7. Architecture 3

The ADS8688 offers conversion times as short as 2 µs per channel. Additionally, the ADS8688 is part of the ADS86xx device family that includes different resolution and channel count options.

Table 8. ADS86xx Family Characteristics

	12b	14b	16b	18b
8 Channel	ADS8668	ADS8678	ADS8688	ADS8698
4 Channel	ADS8664	ADS8674	ADS8684	ADS8694

The TIDA-01214 and TIDA-00170 reference designs are two examples of such architecture.

Architecture 4: High-Voltage Delta Sigma

The ADS125H02 is a 24-bit, 40-kSPS, 2-channel delta-sigma ADC that supports input signals up to ±20 V. This device is used in architecture 4 in addition to the TMUX6209 to implement an 8-channel, high-resolution analog input front-end.

This ADC has a digital filter where the latency limits the minimum multiplexed conversion time to 200 µs. An integrated PGA and dual-excitation current sources allow this architecture to support temperature input (RTD and TC inputs) creating a universal analog input module.

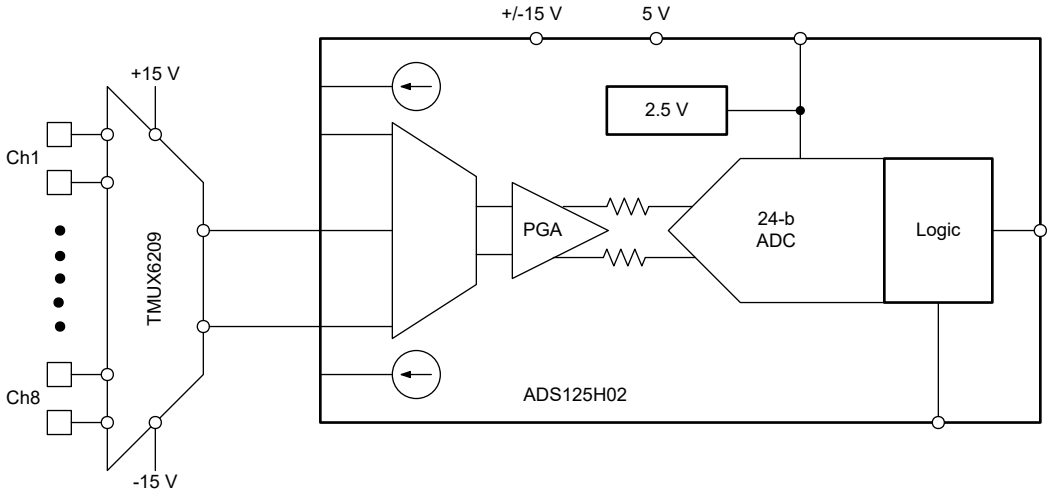

Figure 8. Architecture 4

Alternative differential or single-ended multiplexers are listed in Table 4 and Table 5.

Using delta-sigma converters in multiplexed architectures needs attention from the designer to the ADC latency parameter, or the digital settling time. When switching between channels, older samples of the previous channel need to be flushed out of the digital filter, which requires multiple clock cycles. The ADS125H02 converter has a minimum of 0.179-ms latency when running at 40 kSPS which means a minimum conversion time of around 180 µs to 200 µs, this translates to a maximum of 5.58-kSPS throughput of the converter when used in multiplexed mode.

See the *Four-channel, differential input, DAQ front-end circuit with configurable voltage and current inputs* circuit design document and the *Simplifying a ±10 V PLC Analog Input Module Signal Chain Using the ADS125H02* application brief for details of the design steps of this architecture.

Architecture 5: High-Resolution SAR

This architecture is similar to architecture 3 using the higher resolution SAR ADC ADS8924B, higher-performance, fully-differential driver THS4551, OPA2189 buffer op amp, and low-leakage differential MUX MUX36D08.

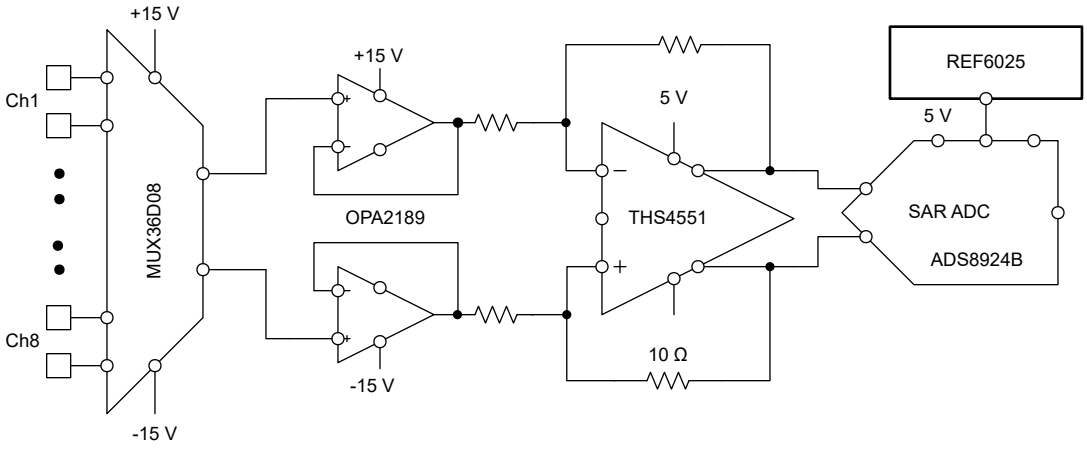

Figure 9. Architecture 5

The ADS89xxB family has multiple devices running from 250 kSPS to 1 MSPS:

Table 9. ADS89xxB Family Characteristics

SPS	250 kSPS	500 kSPS	1 MSPS
16b	ADS8924B	ADS8922B	ADS8920B
18b	ADS8914B	ADS8912B	ADS8910B
20b	ADS8904B	ADS8902B	ADS8900B

The TIDA-01057 reference design shows the front-end design of this architecture.

Architecture 6: High-Speed Delta Sigma

When high-resolution is needed with short conversion time down to 10 µs, the ADS127L11, 24-bit, 1-MSPS, 1-channel delta-sigma ADC is used in combination with the MUX36D08 and INA851. The INA851 is a precision 35-µV offset, 22-MHz BW, 3.2-nV/√Hz input noise, 37 V/µs slew-rate, first-in-class fully-differential INA. A 4.096, 5-ppm REF6041 voltage reference enables this highly-linear signal-chain to achieve high SNR.

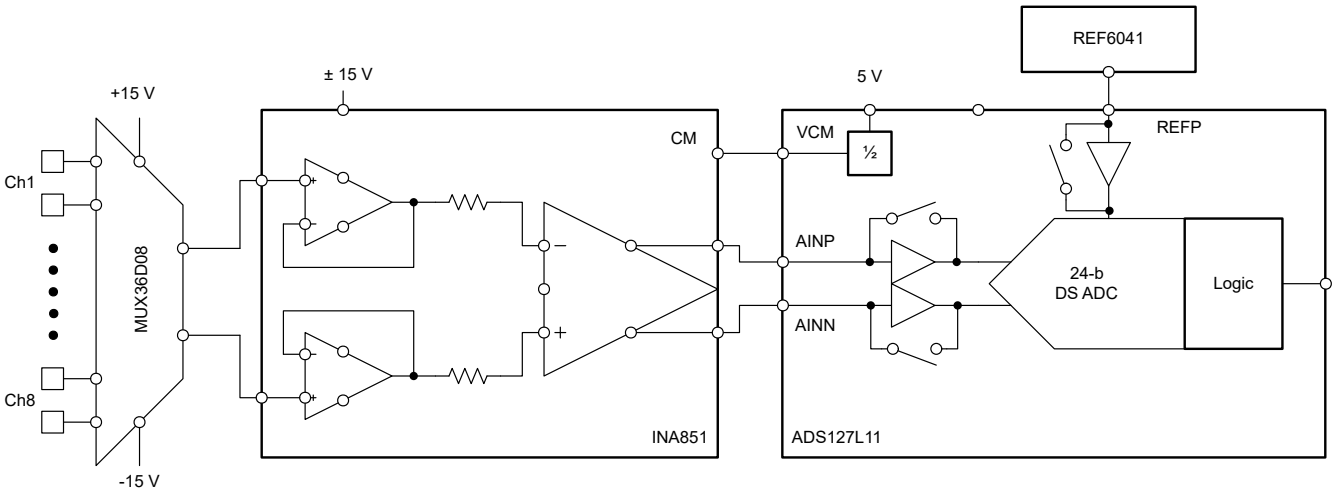

Figure 10. Architecture 6

Similar to other architectures with external multiplexers, differential and single-ended MUX alternatives are available according to the number of channels. Refer toTable 4 and Table 5.

Alternative to the INA851 are the programmable gain amplifiers PGA855 . Another alternative is a dual high slew-rate op amp like the OPA2189 followed by a differential amplifier such as the THS4551 similar to Architecture 5: High-Resolution SAR.

Other options for voltage reference include the 2.5 V REF6025, and the high performance REF70 family.

See the *THP210 and ADS127L11 Performance* application note for some aspects of front-end design for this architecture.

Simultaneous-Sampling Architectures

Although a multiplexed input architecture can achieve relatively fast conversion time, some applications require a very short cycle time or simultaneous sampling of the inputs. In these cases, multiple ADCs converting in parallel are necessary. Multiple ADCs can be separate devices or multiple ADC cores in one chip.

Architecture 7: Simsam SAR

One option to design a medium-resolution system is to use an ADS8588, which is a 16-bit, 500-kSPS, 8-channel simsam SAR ADC with integrated front-end and 2.5-V reference. An INA such as the INA823 is used to convert the differential input signals to single-ended outputs for the ADC, while also providing high input impedance.

The ADS8588 also integrates a digital averaging filter that can increase the SNR by averaging, at the expense of decreased throughput.

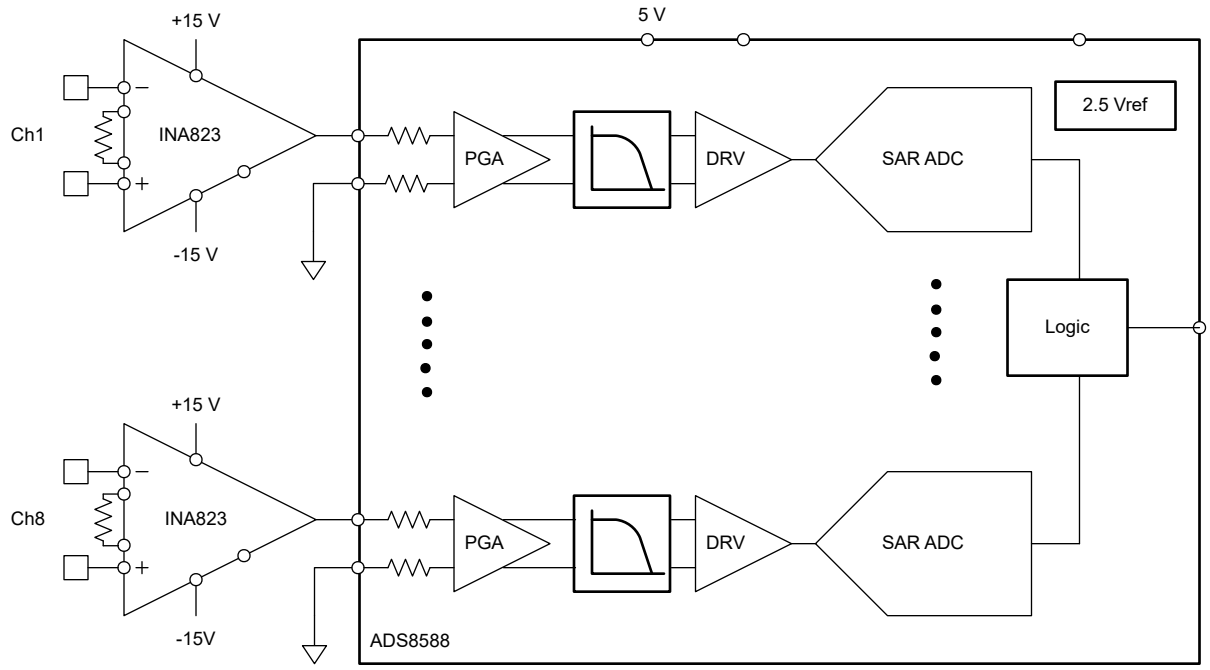

Figure 11. Architecture 7

The ADS85xx is a family of simsam SAR ADCs offering a resolution from 14b to 18b, different number of channels 4 to 8, and speed from 200kSPS to 500 kSPS as shown in Table 10.

Table 10. ADS85xx Family Characteristics

Device	Bits	kSPS	Number of Channels	Device	Bits	kSPS	Number of Channels
ADS8578S	14	200	8	**ADS8584S**	16	330	4
ADS8586S	16	250	6	**ADS8588H**	16	500	8
ADS8588S	16	200	8	**ADS8598H**	18	500	8
ADS8598S	18	200	8				

See the TIDA-00834 reference design for more information about this architecture.

Architecture 8: Simsam Delta Sigma

For applications that require higher-resolution simultaneous sampling, choose a delta-sigma ADC such as the ADS131A04. This 24-bit, 128-kSPS, 4-channel simultaneous sampling ADC integrates a voltage reference and can be used for 4-channel designs. However, the ADS131A04 requires a driver amplifier because this device has low-input impedance. A fully-differential amplifier such as the THS4561 is used to drive the ADC inputs and scale the input signal to the full-scale level (±4 V). A dual op-amp buffer such as the OPA2145 is used to drive the THS4561 to achieve high-input impedance.

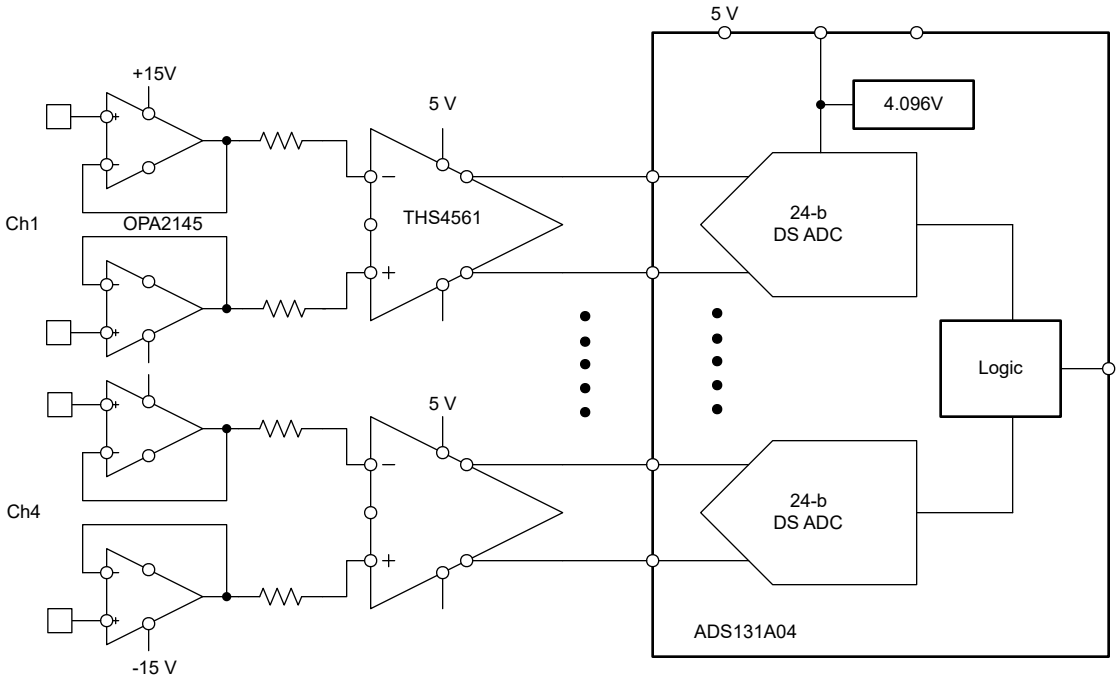

Figure 12. Architecture 8

The TIDA-00835 reference design is one example of the simsam delta-sigma architecture.

Comparing the AIN Architectures

Having different architectures helps module designers optimize performance versus cost based on target requirements. The different architectures mainly differ in what conversion time and cycle time can be achieved as well as the resolution. Table 11 summarizes the differences and also gives an estimation of the relative cost indicated as a horizontal bar made of stars, assuming all are differential and N channels.

Table 11. AIN Architecture Comparison

	Arch. 1	Arch. 2	Arch. 3	Arch. 4	Arch. 5	Arch. 6	Arch. 7	Arch. 8
tConversion minimum (µs)	80 – 120	25 – 100	2	200	10 – 25	10	2 – 5	10
tCycle minimum (µs)	N × tConv	N × tConv	N × tConv	N × tConv	N × tConv	N × tConv	2 – 5	10
Resolution (bit)	12 – 18	12 – 18	12 – 18	24	16 – 20	24	14 – 18	24
Cost	*	**	****	**	***	****	*****	******

This overview does not cover several features of AIN modules that influence the front-end design, which are covered in other literature. These features include:

- Support of high common-mode voltage
- Support of two-terminal V/I input
- Designing for bipolar ±10-V input with single 5-V supply

Device Selection

The following list covers the relevant parameters of front-end components when designing multiplexed input.

- For **multiplexers**, low off-state leakage increases input impedance. Low on-state leakage reduces error in current input. High input absolute maximum voltage simplifies protection and allows for higher common-mode voltage. Low cross-talk reduces conversion error. While low output capacitance reduces settling time in case of a high sampling rate and a large number of channels. Typically, on-state impedance does not play an important role in case of high-Z channels.
- For **amplifiers**, low-offset drift is important for high-resolution channels. Look for zero-drift, MUX-ready amplifiers. Low noise is also important for high-resolution system (18b or higher) to increase ENOBs. Some amplifiers have overvoltage protection which simplifies protection. For short conversion times, high slew-rate and wide-bandwidth are required.
- For **instrumentation amplifiers**, low offset-drift and gain-drift are required because INAs are hard to compensate with calibration. High CMRR and low noise improves ENOBs. High slew rate and wide bandwidth are required for short conversion times, and overvoltage protection is a plus to simplify channel input protection.

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