Application Brief

Fast Enable Amplifier With Fail-Safe Input ESD

A common design goal in a battery-powered application is reducing power consumption of the analog signal chain, typically consisting of a sensor, an amplifier, and an analog-to-digital converter (ADC). Sensors can be left *always on* because of their longer latencies at power-up. For ADCs, the power consumption is often dominated by the conversion cycle and it is common to operate ADC in burst mode to facilitate a shorter conversion cycle to lower power consumption. Now there are two amplifier choices for reducing the power consumption, these amplifiers are discussed in detail in this document.

The primary choice usually is to select an amplifier with lower quiescent current (power) and keep the amplifier on during the entire ADC acquisition and conversion cycles. While this can look attractive at first, the main trade-off here is that these low-power amplifiers tend to have a higher thermal noise floor and higher output impedance which affects precision and output drive, respectively. Table 1 shows the typical data for some low-power amplifiers.

Table 1. Always ON, Low-Power Amplifier Specifications

Generic Part Number	Quiescent Current I_{Q_ON} (µA)	Bandwidth (MHz)	Thermal Noise Floor at 1 kHz (nV / √Hz)	Low Frequency Integrated Noise 0.1 to 10 Hz (μV_{p-p})	Output Impedance at 1 kHz (kΩ)
TLV8801	0.45	0.006	450	12	90
TLV8541	0.50	0.008	264	8.6	8
TLV379	4	0.090	83	2.8	28
TLV9041	10	0.350	66	6.5	7

As Table 1 shows, the lower the quiescent current of an amplifier, the higher is the thermal noise floor. This higher thermal noise can be acceptable if the signal frequency is well under 100 Hz as the low-frequency noise of these amplifiers becomes more dominant than the thermal noise floor. If the signal frequency is higher than 1 kHz, a slightly better secondary choice is to use an amplifier with a lower thermal noise floor and shutdown functionality to improve signal-to-noise ratio as well as maintain lower power. The lower power can be achieved by periodically enabling the amplifier to make a measurement, when required, while disabling the amplifier for the remainder of the time. The amplifier must be enabled just before the end of the ADC acquisition cycle to get a settled signal in time for the beginning of the ADC conversion cycle. This technique of using shutdown amplifiers to make periodic measurements is referred to as duty-cycling.

Table 2. Duty-Cycle Amplifiers: TLV90x1S vs OPAx310S Specifications

Generic Part Number	Bandwidth (MHz)	Enable time (µs)	Quiescent Current enable mode - I_{Q_ON} (µA)	Quiescent Current disable mode - I_{Q_SHDN} (µA)	Thermal Noise Floor at 1 kHz (nV / √Hz)
TLV9001S	1	70	60	0.500	27
TLV9061S	10	10	538	0.500	10
OPA310S	**3**	**1**	**165**	**0.265**	**13**

The quiescent current of an amplifier in enable, disable modes and the enable, disable times are the key specifications that dictate the average power consumption when duty-cycling an amplifier. Table 2 shows that the enable time of these shutdown amplifiers is inversely proportional to the bandwidth. The OPA310S is a clear exception to the trend. This device achieves a much lower enable time of 1 µs at a 3-MHz bandwidth while consuming lower quiescent current of 165 µA when enabled and 265 nA when disabled. Along with lower

thermal noise floor of 13 nV / √Hz, this makes the OPAx310S an excellent choice for systems implementing duty-cycling techniques for power savings.

For higher power savings, it is important to lower the amplifier ON time which consequently reduces the duty cycle (%) to lower the average quiescent current. The lower average quiescent current directly lowers energy consumption leading to a longer battery life. Table 3 summarizes the minimum duty-cycle values that can be achieved with these amplifiers assuming a measurement must be taken every 1 ms with 0.01% accuracy. The total ON time of the amplifier is the summation of the time it takes to turn on the amplifier and the time it takes for the output to settle to ADC accuracy (assumed to be 0.01% in this case).

Equation 1 through Equation 3 describe the total ON time, total OFF time, and minimum duty cycle (D).

$$\text{Total ON time } (\mu s) = \text{Enable time } (\mu s) + \text{Settling time } 0.01\% \ (\mu s) \quad (1)$$

$$\text{Total OFF time } (\mu s) = 1000 \ (\mu s) + \text{Total ON time } (\mu s) \quad (2)$$

$$\text{Minimum Duty Cycle, } D(\%) = \frac{\text{Total ON time } (\mu s)}{1000 \ (\mu s)} \times 100 \quad (3)$$

Table 3. Duty Cycle Comparison: TLV90x1S vs OPA310S

Generic Part Number	Enable time (µs)	Settling time 0.01% (µs)	Total ON time (µs)	Total OFF time (µs)	Minimum Duty Cycle (D) (%)
TLV9001S	70	3	73	927	7.30
TLV9061S	10	1	11	989	1.10
OPA310S	**1**	**1.6**	**2.6**	**997.4**	**0.26**

The OPA310S (which has faster enable time and settling time) helps to achieve an overall lower total ON time leading to shorter duty cycle in comparison to other duty-cycled amplifiers. Table 4 outlines the average current consumption while meeting the 0.01% settling time requirements across 1-ms time frame along with the thermal noise floor, which is the performance parameter.

$$\text{Average Quiescent Current in 1 ms } (\mu A) = I_{Q\_ON} \times \frac{D}{100} + I_{Q\_OFF} \times \left(1 - \frac{D}{100}\right) \quad (4)$$

Table 4. All Amplifiers Quiescent Current Comparison

Type	Generic Part Number	Average Quiescent Current in 1 ms (µA)	Thermal Noise Floor at 1 kHz (nV / √Hz)
Always ON	TLV8541	0.50	265
Always ON	TLV9041	10	66
Duty Cycled	TLV9001S	4.84	27
Duty Cycled	TLV9061S	6.41	10
Duty Cycled	**OPA310S**	**0.69**	**13**

In comparison to the duty-cycled TLV9061, the OPA310S achieves 89% lower quiescent current for just 3 nV / √Hz of increase in the thermal noise floor. In comparison to the always on TLV8541, the OPA310S achieves 95% lower noise for just 0.19 µA increase in the average quiescent current. These improvements make the OPAx310S family a good fit for power-conscious applications that require a certain degree of noise performance. These comparisons above are for static power consumption because the dynamic power consumption can vary depending on the amplifier output load in an application. The above comparisons hold true as long as the dynamic power consumption is smaller when compared to static power consumption.

The OPAx310S devices also offer better reliability and avoid faults or failures when interfacing to sensors. These sensors commonly require a different power-supply voltage in comparison to the amplifier, thus mandating a careful power sequencing. If done incorrectly, this potentially leads to sensor loading at the input of the amplifier and faulty signals at the output of the amplifier. This is where the fail-safe input ESD structure of the OPAx310S can help in comparison to the traditional input ESD structure of most amplifiers which is shown in Figure 1.

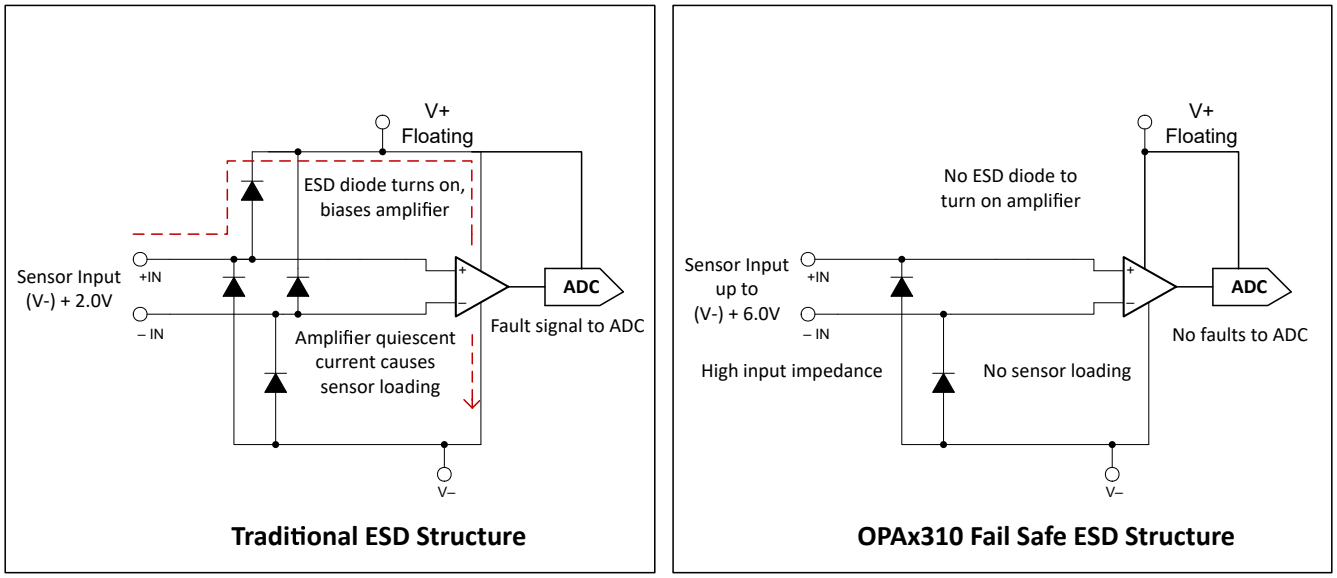

Figure 1. ESD Structure Comparison

An amplifier with a traditional input ESD structure has ESD protection diodes from inputs to the positive rail. With this structure, any input signal presenting from the sensor before the presence of the power supply of the amplifier can potentially turn on and forward bias the ESD protection diode between the IN and V+ pins. This, in turn, leads to the sensor output voltage acting as a power-supply voltage and providing quiescent current for the amplifier (also called back powering). This can cause heavy loading of the sensor at the amplifier input and subsequently produce a fault signal at the amplifier output.

The OPAx310S is different from the TLV90xxS in that the OPAx310S does not have any protection ESD diodes from the IN to the V+ pins. During power sequencing, this avoids possible sensor loading at the amplifier input and a possible fault signal at the amplifier output. In fact, the OPAx310S inputs when driven by sensor can go as high as 6 V from V– regardless of what the voltage is on the V+ pin. Further, the OPAx310S device achieves a robust ESD performance of 8-kV HBM (Human body model) and 1.5-kV CDM (Charged-device model) with these fail-safe inputs.

A detailed set of measurements of this robust behavior is found in the *Op Amp ESD Protection Structures* application report. Thus, the fast enable time paired with the fail-safe ESD structure of the OPAx310S family makes the devices a great choice to pair with the high-output impedance sensors and burst mode ADCs. The OPAx310S family is available in single, dual, and quad channels with and without shutdown. Table 5 shows the device options with the shutdown feature included.

Table 5. OPAx310S Shutdown Device Options

Device	Channel	Package Type and Pin	Package Size
OPA4310SIRTER	4	WQFN-16	3.00 mm × 3.00 mm
OPA2310SIRUGR	2	X2QFN-10	1.50 mm × 2.00 mm
OPA310SIDCKR	1	SC70-6	1.25 mm × 2.00 mm
OPA310SIDBVR	1	SOT-23-6	1.60 mm × 2.90 mm

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