24-Bit Analog-to-Digital Converter for Bridge Sensors

Check for Samples: ADS1231

FEATURES

- **Complete Front-End for Bridge Sensors**
- **Internal Amplifier, Gain of 128**
- **Internal Oscillator**
- **Low-Side Power Switch for Bridge Sensor**
- **Low Noise: 35nVrms**
- **Selectable Data Rates: 10SPS or 80SPS**
- **Simultaneous 50Hz and 60Hz Rejection at 10SPS**
- **Input EMI Filter**
- **External Voltage Reference up to 5V for Ratiometric Measurements**
- **Simple, Pin-Driven Control**
- **Two-Wire Serial Digital Interface**
- **Supply Range: 3V to 5.3V**
- **Package: SOIC-16**
- **Temperature Range: –40°C to +85°C**

APPLICATIONS

- **Weigh Scales**
- **Strain Gauges**
- **Load Cells**
- **Industrial Process Control**

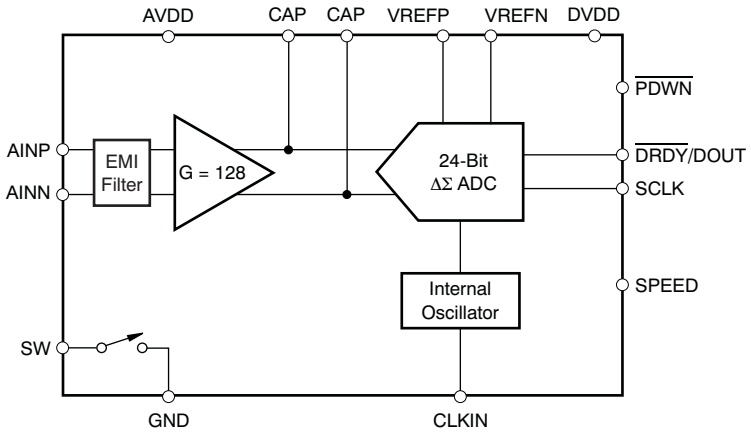
DESCRIPTION

The ADS1231 is a precision, 24-bit analog-to-digital converter (ADC). With an onboard low-noise amplifier, onboard oscillator, precision third-order 24-bit delta-sigma (ΔΣ) modulator, and bridge power switch, the ADS1231 provides a complete front-end solution for bridge sensor applications including weigh scales, strain gauges, and load cells.

The low-noise amplifier has a gain of 128, supporting a full-scale differential input of ±19.5mV. The ΔΣ ADC has 24-bit resolution and is comprised of a third-order modulator and fourth-order digital filter. Two data rates are supported: 10SPS (with both 50Hz and 60Hz rejection) and 80SPS. The ADS1231 can be put in a low-power standby mode or shut off completely in power-down mode.

The ADS1231 is controlled by dedicated pins; there are no digital registers to program. Data are output over an easily-isolated serial interface that connects directly to the MSP430 and other microcontrollers.

The ADS1231 is available in an SO-16 package and is specified from –40°C to +85°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		ADS1231	UNIT
AVDD to GND		–0.3 to +6	V
DVDD to GND		–0.3 to +6	V
Input current		100, momentary	mA
		10, continuous	mA
Analog input voltage to GND		–0.3 to AVDD + 0.3	V
Digital input voltage to GND		–0.3 to DVDD + 0.3	V
ESD(2)	Human body model (HBM) JEDEC standard 22, test method A114-C.01, all pins	±2000	V
	Charged device model (CDM) JEDEC standard 22, test method C101, all pins	±500	V
Maximum junction temperature		+150	°C
Operating temperature range		–40 to +85	°C
Storage temperature range		–60 to +150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) CAUTION: ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS1231 SOIC (D) 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	79.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	37.5	
θ_{JB}	Junction-to-board thermal resistance	37.1	
ψ_{JT}	Junction-to-top characterization parameter	5.6	
ψ_{JB}	Junction-to-board characterization parameter	36.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

Minimum/maximum limit specifications apply from –40°C to +85°C. Typical specifications at +25°C.
All specifications at AVDD = DVDD = VREFP = +5V, V_{CM} = 2.5V and VREFN = GND, unless otherwise noted.

PARAMETER		CONDITIONS	ADS1231 MIN	ADS1231 TYP	ADS1231 MAX	UNIT
ANALOG INPUTS						
Full-scale input voltage (AINP – AINN)				$\pm 0.5V_{REF}$ / 128		V
		V_{REF} = AVDD = 5V		±19.5		mV
		V_{REF} = AVDD = 3V		±11.7		mV
Common-mode input range			GND + 1.5		AVDD – 1.5	V
Differential input current				±2		nA
LOW-SIDE POWER SWITCH						
On-resistance (R_{ON})		AVDD = 5V, I_{SW} = 30mA		3.5	5	Ω
		AVDD = 3V, I_{SW} = 30mA		4	7	Ω
Current through switch					30	mA
SYSTEM PERFORMANCE						
Resolution		No missing codes	24			Bits
Data rate		Internal oscillator, SPEED = high		80		SPS
		Internal oscillator, SPEED = low		10		SPS
		External clock, SPEED = high		f_{CLKIN} / 61,440		SPS
		External clock, SPEED = low		f_{CLKIN} / 491,520		SPS
Digital filter settling time		Full settling		4		Conversions
Noise		f_{DATA} = 10SPS, AVDD = V_{REF} = 5V		35		nV, rms
		f_{DATA} = 80SPS, AVDD = V_{REF} = 5V		102		nV, rms
		f_{DATA} = 10SPS, AVDD = V_{REF} = 5V		232		nV, P-P
		f_{DATA} = 80SPS, AVDD = V_{REF} = 5V		622		nV, P-P
Integral nonlinearity (INL)		Differential input, end-point fit		±8		ppm
Input offset error				10		µV
Input offset drift				±20		nV/°C
Gain error				1		%
Gain drift				±2		ppm/°C
Normal-mode rejection(1)		f_{IN} = 50Hz or 60Hz ±1Hz, f_{DATA} = 10SPS, internal oscillator	80	100		dB
		f_{IN} = 50Hz or 60Hz ±1Hz, f_{DATA} = 10SPS, external clock(2)	90	110		dB
Common-mode rejection		At dc		110		dB
Power-supply rejection		At dc	90	100		dB
VOLTAGE REFERENCE INPUT						
Voltage reference input (V_{REF})		V_{REF} = VREFP – VREFN	1.5	AVDD	AVDD + 0.1	V
Negative reference input (VREFN)			GND – 0.1		VREFP – 1.5	V
Positive reference input (VREFP)			VREFN + 1.5		AVDD + 0.1	V
Voltage reference input current				10		nA
DIGITAL INPUT/OUTPUT (DVDD = 3V to 5.3V)						
Logic levels	V_{IH}		0.8 DVDD		DVDD + 0.1	V
	V_{IL}		GND		0.2 DVDD	V
	V_{OH}	I_{OH} = 500µA	DVDD – 0.4			V
	V_{OL}	I_{OL} = 500µA			0.2 DVDD	V
Input leakage		0 < $V_{DIGITAL\ INPUT}$ < DVDD			±10	µA
External clock input frequency (f_{CLKIN})			1	4.9152	6	MHz
Serial clock input frequency (f_{SCLK})					5	MHz

(1) Specification is assured by the combination of design and final test.
(2) f_{CLKIN} = 4.9152MHz.

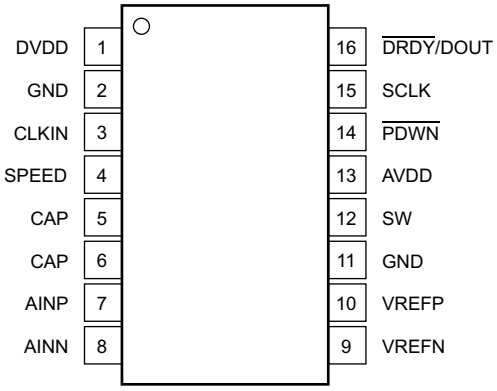
ELECTRICAL CHARACTERISTICS (continued)

Minimum/maximum limit specifications apply from –40°C to +85°C. Typical specifications at +25°C.
All specifications at AVDD = DVDD = VREFP = +5V, V_{CM} = 2.5V and VREFN = GND, unless otherwise noted.

PARAMETER	CONDITIONS	ADS1231			UNIT
		MIN	TYP	MAX	
POWER SUPPLY					
Power-supply voltage (AVDD, DVDD)		3		5.3	V
Analog supply current	Normal mode, AVDD = 3V		900		µA
	Normal mode, AVDD = 5V		900		µA
	Standby mode		0.1		µA
	Power-down		0.1		µA
Digital supply current	Normal mode, DVDD = 3V		60		µA
	Normal mode, DVDD = 5V		95		µA
	Standby mode, SCLK = high, DVDD = 3V		45		µA
	Standby mode, SCLK = high, DVDD = 5V		65		µA
	Power-down		0.2		µA
Power dissipation, total	Normal mode, AVDD = DVDD = 3V		2.9		mW
	Normal mode, AVDD = DVDD = 5V		5		mW
TEMPERATURE					
Operating temperature range		–40		+85	°C
Specified temperature range		–40		+85	°C

PIN CONFIGURATION

D PACKAGE
SO-16
(TOP VIEW)



PIN DESCRIPTIONS

NAME	TERMINAL	ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION
DVDD	1	Digital	Digital power supply
GND	2	Supply	Ground for digital and analog supplies
CLKIN	3	Digital input	External clock input: typically 4.9152MHz. Tie low to activate internal oscillator.
SPEED	4	Digital input	Data rate select: SPEED: 0 → DATA RATE: 10SPS SPEED: 1 → DATA RATE: 80SPS
CAP	5	Analog	Gain amplifier bypass capacitor connection
CAP	6	Analog	Gain amplifier bypass capacitor connection
AINP	7	Analog input	Positive analog input
AINN	8	Analog input	Negative analog input
VREFN	9	Analog input	Negative reference input
VREFP	10	Analog input	Positive reference input
GND	11	Supply	Ground for digital and analog supplies
SW	12	Analog	Low-side power switch
AVDD	13	Supply	Analog power supply
$\overline{\text{PDWN}}$	14	Digital input	Power-down: holding this pin low powers down the entire converter and resets the ADC.
SCLK	15	Digital input	Serial clock: clock out data on the rising edge. Also used to initiate Standby mode. See the *Standby Mode* section for more details.
$\overline{\text{DRDY}}$/DOUT	16	Digital output	Dual-purpose output: Data ready: indicates valid data by going low. Data output: outputs data, MSB first, on the first rising edge of SCLK.

NOISE PERFORMANCE

The ADS1231 offers outstanding noise performance. Table 1 summarizes the typical noise performance with inputs shorted externally for different data rates and voltage reference values.

The RMS and Peak-to-Peak noise are referred to the input. The effective number of bits (ENOB) is defined as:

ENOB = ln (FSR/RMS noise)/ln(2)

The Noise-Free Bits are defined as:

Noise-Free Bits = ln (FSR/Peak-to-Peak Noise)/ln(2)

Where:

FSR (Full-Scale Range) = V_{REF}/Gain.

Table 1. Noise Performance

DATA RATE	AVDD and V_{REF} (V)	RMS NOISE(1) (nV)	PEAK-TO-PEAK NOISE(1) (nV)	ENOB (RMS)	NOISE-FREE BITS
10	5	35.2	231.9	20.1	17.4
	3	33.5	199.2	19.4	16.8
80	5	102.1	622.1	18.5	15.9
	3	80.3	549.6	18.2	15.4

(1) Noise specifications are based on direct measurement of 1024 consecutive samples.

TYPICAL CHARACTERISTICS

At T_A = +25°C, AVDD = DVDD = REFP = 5V, REFN = GND, and V_{CM} = 2.5V unless otherwise noted.

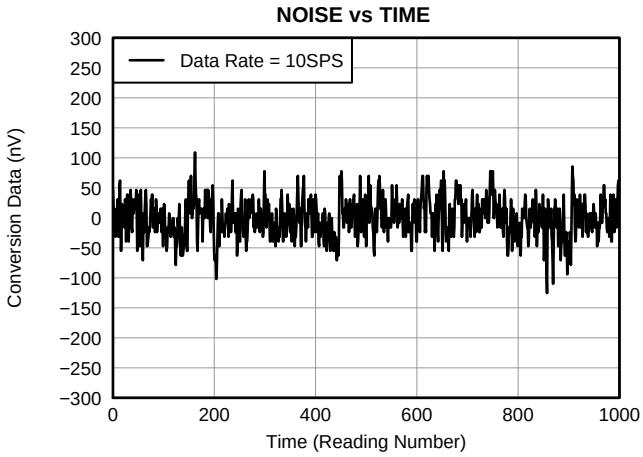


Figure 1.

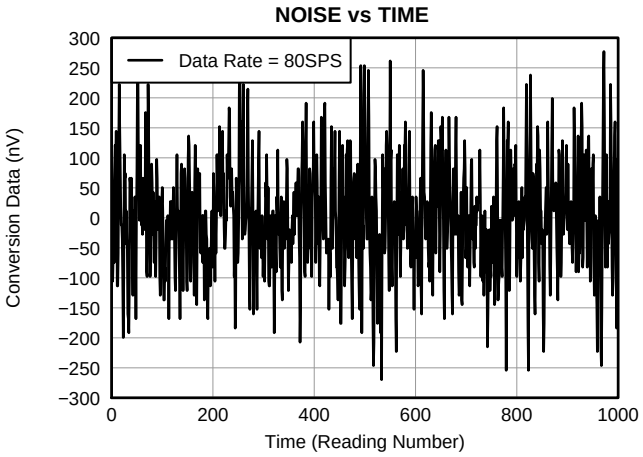


Figure 2.

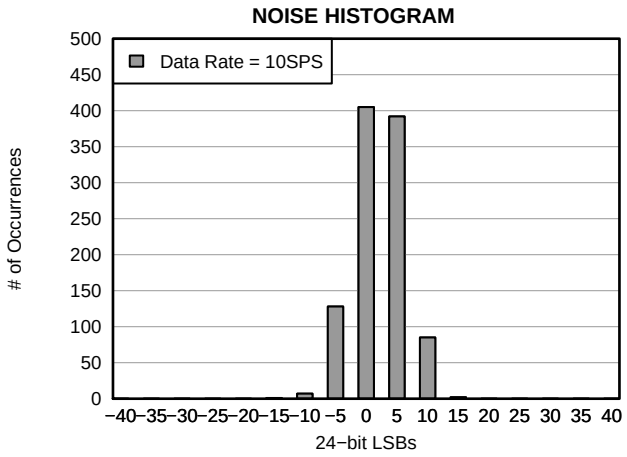


Figure 3.

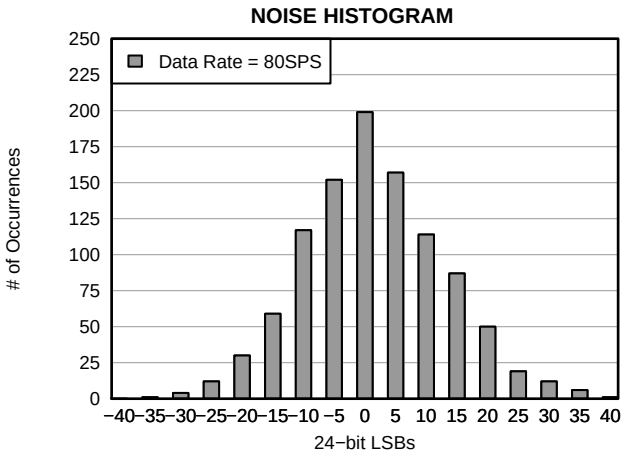


Figure 4.

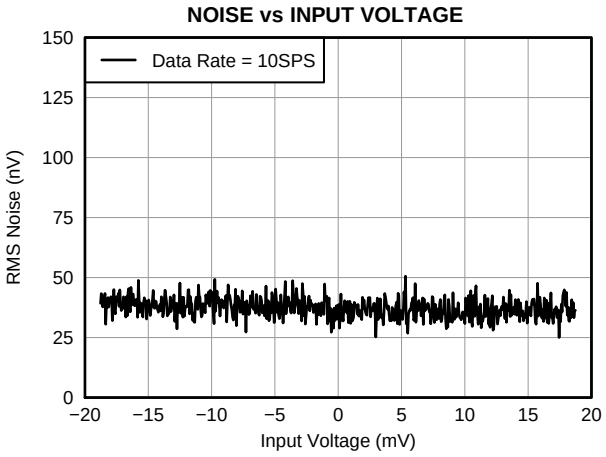


Figure 5.

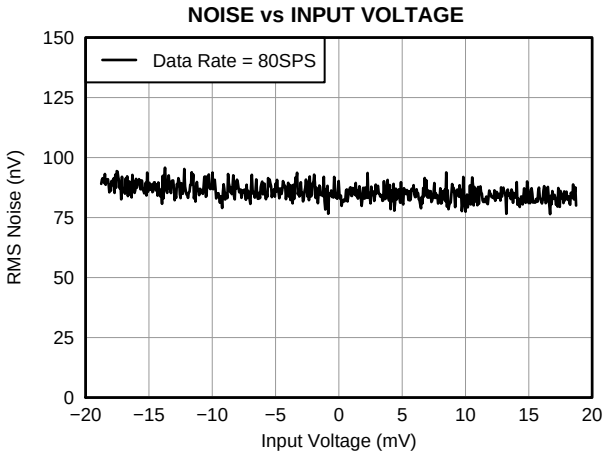


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = DVDD = REFP = 5V, REFN = GND, and V_{CM} = 2.5V unless otherwise noted.

OFFSET DRIFT vs TEMPERATURE

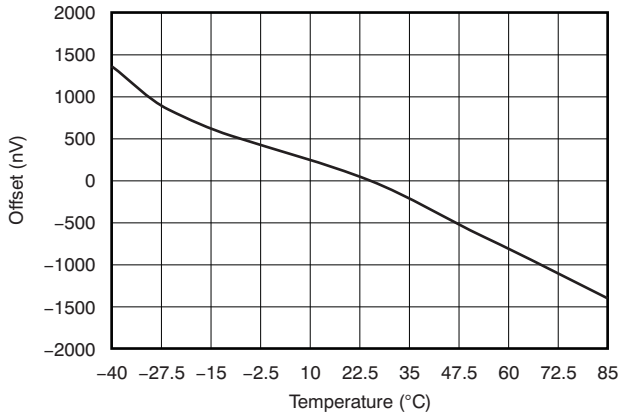


Figure 7.

GAIN ERROR vs TEMPERATURE

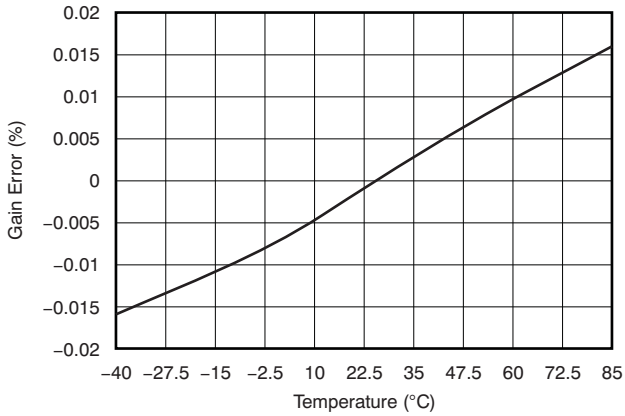


Figure 8.

INL vs INPUT VOLTAGE

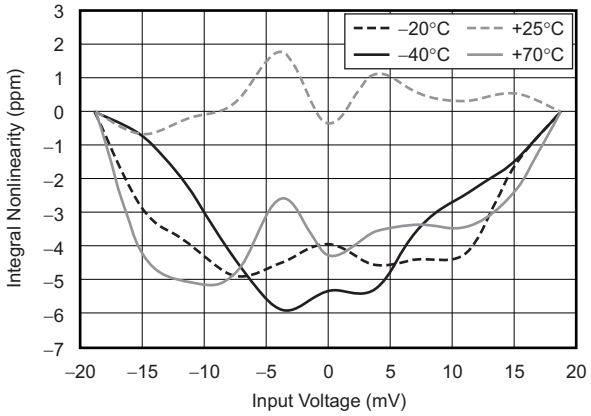


Figure 9.

DATA RATE vs TEMPERATURE

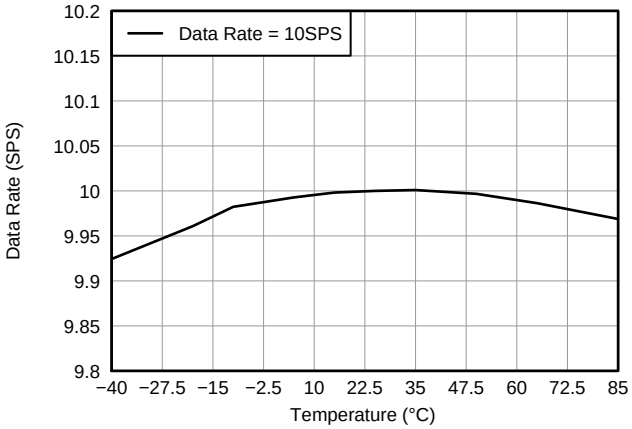


Figure 10.

ANALOG SUPPLY CURRENT vs TEMPERATURE

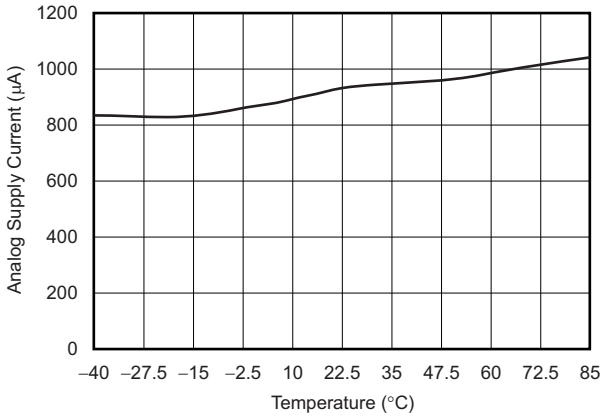


Figure 11.

DIGITAL SUPPLY CURRENT vs TEMPERATURE

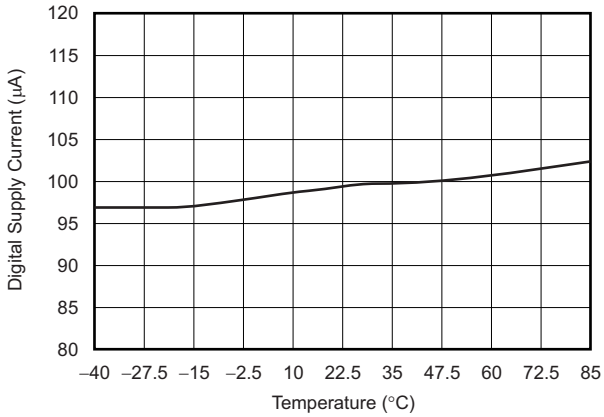


Figure 12.

OVERVIEW

The ADS1231 is a precision, 24-bit ADC that includes a low-noise PGA, internal oscillator, third-order delta-sigma (ΔΣ) modulator, and fourth-order digital filter. The ADS1231 provides a complete front-end solution for bridge sensor applications such as weigh scales, strain gauges, and pressure sensors.

Data can be output at 10SPS for excellent 50Hz and 60Hz rejection, or at 80SPS when higher speeds are needed. The ADS1231 is easy to configure, and all digital control is accomplished through dedicated pins; there are no registers to program. A simple two-wire serial interface retrieves the data.

ANALOG INPUTS (AINP, AINN)

The input signal to be measured is applied to the input pins AINP and AINN. The ADS1231 accepts differential input signals, but can also measure unipolar signals.

LOW-NOISE AMPLIFIER

The ADS1231 features a low-drift, low-noise amplifier that provides a complete front-end solution for bridge sensors. A simplified diagram of the amplifier is shown in Figure 13. It consists of two chopper-stabilized amplifiers (A1 and A2) and three accurately matched resistors (R_1, R_{F1}, and R_{F2}) that construct a differential front-end stage with a gain of 128, followed by gain stage A3 (Gain = 1). The inputs are equipped with an EMI filter, as shown in Figure 13. The cutoff frequency of the EMI filter is 20MHz. By using AVDD as the reference input, the bipolar input ranges from –19.5mV to +19.5mV. The inputs of the ADS1231 are protected with internal diodes connected to the power-supply rails. These diodes clamp the applied signal to prevent it from damaging the input circuitry.

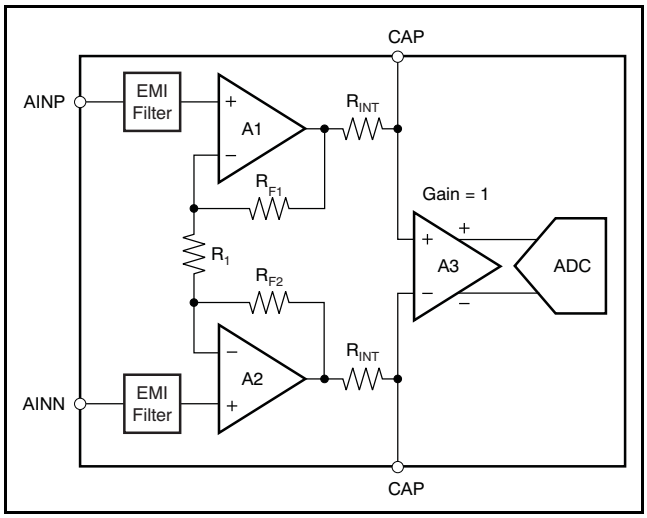


Figure 13. Simplified Diagram of the Amplifier

External Capacitor

An external capacitor (C_{EXT}) across the two ADS1231 CAP pins combines with the internal resistor R_{INT} (on-chip) to create a low-pass filter. The recommended value for C_{EXT} is 0.1μF which provides a corner frequency of 720Hz. This low-pass filter serves two purposes. First, the input signal is band-limited to prevent aliasing by the ADC and to filter out the high-frequency noise. Second, it attenuates the chopping residue from the amplifier to improve temperature drift performance. NPO or C0G capacitors are recommended. For optimal performance, place the external capacitor very close to the CAP pins.

VOLTAGE REFERENCE INPUTS (VREFP, VREFN)

The voltage reference used by the modulator is generated from the voltage difference between VREFP and VREFN: V_{REF} = VREFP – VREFN. The reference inputs use a structure similar to that of the analog inputs. In order to increase the reference input impedance, switching buffer circuitry is used to reduce the input equivalent capacitance. The reference drift and noise impact ADC performance. In order to achieve best results, pay close attention to the reference noise and drift specifications. A simplified diagram of the circuitry on the reference inputs is shown in Figure 14. The switches and capacitors can be modeled approximately using an effective impedance of Z_{EFF} = 500MΩ.

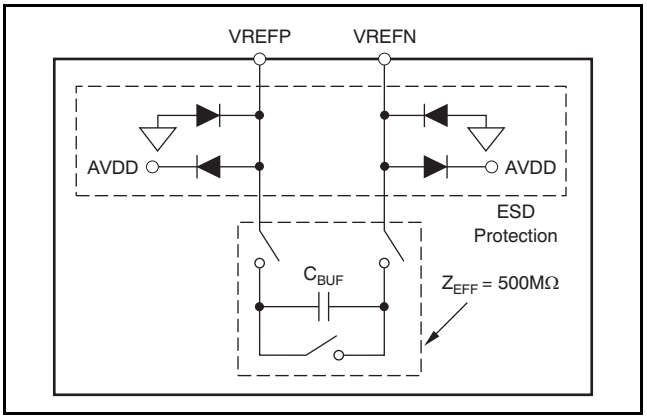


Figure 14. Simplified Reference Input Circuitry

ESD diodes protect the reference inputs. To prevent these diodes from turning on, make sure the voltages on the reference pins do not go below GND by more than 100mV, and likewise, do not exceed AVDD by 100mV:

GND – 100mV < (VREFP or VREFN) < AVDD + 100mV

LOW-SIDE POWER SWITCH (SW)

The ADS1231 incorporates an internal switch for use with an external bridge sensor, as shown in Figure 15. The switch can be used in a return path for the bridge power. By opening the switch, power dissipation in the bridge is eliminated.

The switch is controlled by the ADS1231 conversion status. During normal conversions, the switch is closed (the SW pin is connected to GND). During standby or power-down modes, the switch is opened (the SW pin is high impedance). When using the switch, it is recommended that the negative reference input (VREFN) be connected directly to the bridge ground terminal, as shown in Figure 15 for best performance.

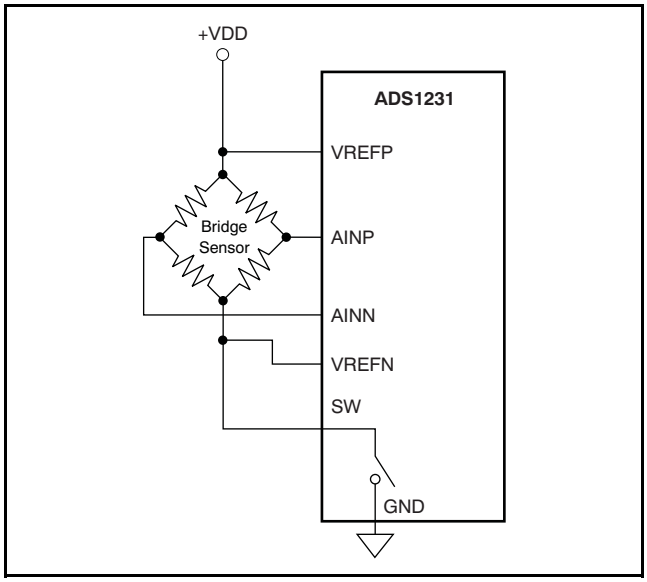


Figure 15. Low-Side Power Switch

CLOCK SOURCE

The ADS1231 can use the internal oscillator or an external clock source to accommodate a wide variety of applications. Figure 16 shows the equivalent circuitry of the clock module. The CLK_DETECT block determines whether an external clock signal is applied to the CLKIN pin so that the internal oscillator is bypassed or activated. When the CLKIN pin frequency is above ~200kHz, the CLK_DETECT circuit shuts down the internal oscillator and passes the external clock signal to the ADC. When the CLKIN pin frequency is below ~200kHz, the CLK_DETECT block activates the internal oscillator. When the internal oscillator is chosen, make sure to connect the CLKIN pin to GND.

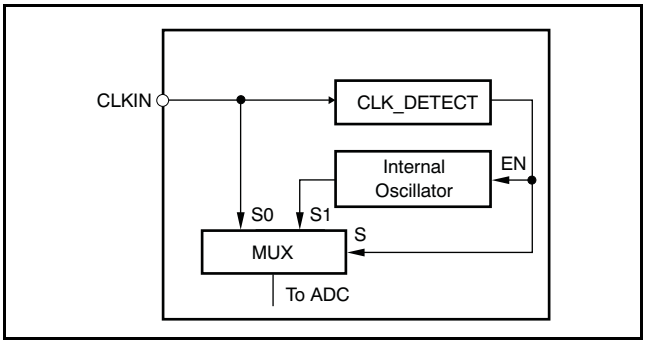


Figure 16. Equivalent Circuitry of the Clock Source

The allowable frequency range for the external clock signal f_{CLKIN} is specified in the Electrical Characteristics table.

FREQUENCY RESPONSE

The ADS1231 uses a sinc^4 digital filter with the frequency response shown in Figure 17 for f_{CLKIN} = 4.9152MHz. The frequency response repeats at multiples of the modulator sampling frequency of 76.8kHz. The overall response is that of a low-pass filter with a –3dB cutoff frequency of 3.32Hz with the SPEED pin tied low (10SPS data rate) and 11.64Hz with the SPEED pin tied high (80SPS data rate).

To help see the response at lower frequencies, Figure 17(a) illustrates the nominal response out to 100Hz, when the data rate = 10SPS. Notice that signals at multiples of 10Hz are rejected, and therefore simultaneous rejection of 50Hz and 60Hz is achieved.

The benefit of using a sinc^4 filter is that every frequency notch has four zeros on the same location, thus providing excellent normal-mode rejection of line-cycle interference.

Figure 17(b) zooms in on the 50Hz and 60Hz notches with the SPEED pin tied low (10SPS data rate).

The ADS1231 data rate and frequency response scale directly with clock frequency. For example, if f_{CLKIN} increases from 4.9152MHz to 5.5296MHz when the SPEED pin is tied high, the data rate increases from 80SPS to 90SPS, while the notch also increases from 80Hz to 90Hz. Note that these changes are only possible when an external clock source is applied.

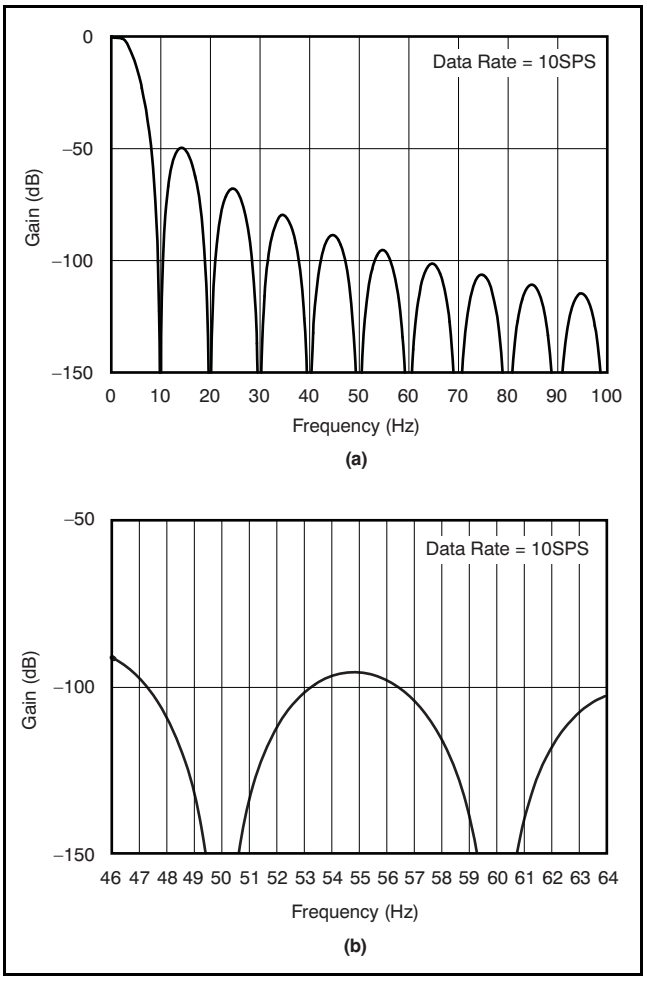


Figure 17. Nominal Frequency Response Out To 100Hz

SETTLING TIME

Fast changes in the input signal require time to settle. For example, an external multiplexer in front of the ADS1231 can generate abrupt changes in input voltage by simply switching the multiplexer input channels. These sorts of changes in the input require four data conversion cycles to settle. When continuously converting, five readings may be necessary in order to settle the data. If the change in input occurs in the middle of the first conversion, four more full conversions of the fully-settled input are required to obtain fully-settled data. Discard the first four readings because they contain only partially-settled data. Figure 18 illustrates the settling time for the ADS1231.

DATA RATE

The ADS1231 data rate is set by the SPEED pin, as shown in Table 2. When SPEED is low, the data rate is nominally 10SPS. This data rate provides the lowest noise, and also has excellent rejection of both 50Hz and 60Hz line-cycle interference. For applications requiring fast data rates, setting SPEED high selects a data rate of nominally 80SPS.

Table 2. Data Rate Settings

SPEED PIN	DATA RATE	
	Internal Oscillator	External Clock
0	10SPS	f_{CLKIN} / 491,520
1	80SPS	f_{CLKIN} / 61,440

DATA FORMAT

The ADS1231 outputs 24 bits of data in binary twos complement format. The least significant bit (LSB) has a weight of $(0.5V_{REF}/128)(2^{23} - 1)$. The positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 3 summarizes the ideal output codes for different input signals.

Table 3. Ideal Output Code vs Input Signal

INPUT SIGNAL V_{IN} (AINP – AINN)	IDEAL OUTPUT
≥ $+0.5V_{REF}/128$	7FFFFFh
$(+0.5V_{REF}/128)/(2^{23} - 1)$	000001h
0	000000h
$(-0.5V_{REF}/128)/(2^{23} - 1)$	FFFFFFh
≤ $-0.5V_{REF}/128$	800000h

1. Excludes effects of noise, INL, offset, and gain errors.

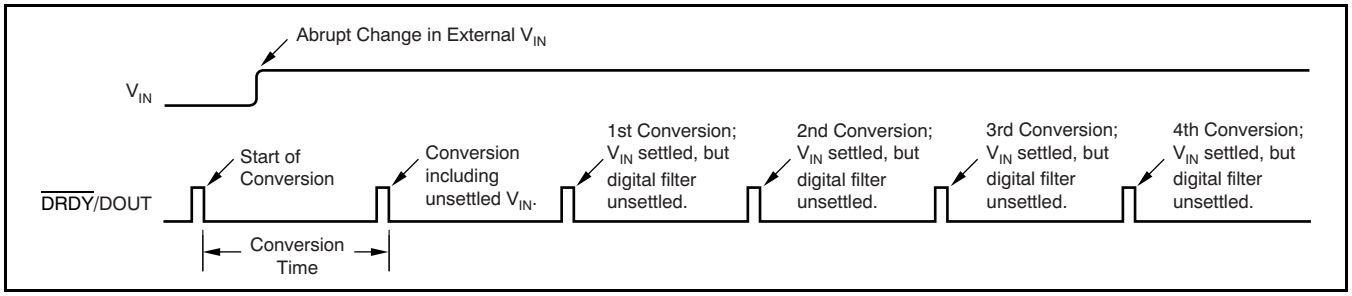


Figure 18. Settling Time in Continuous Conversion Mode

DATA READY/DATA OUTPUT (DRDY/DOUT)

This digital output pin serves two purposes. First, it indicates when new data are ready by going low. Afterwards, on the first rising edge of SCLK, the DRDY/DOUT pin changes function and begins outputting the conversion data, most significant bit (MSB) first. Data are shifted out on each subsequent SCLK rising edge. After all 24 bits have been retrieved, the pin can be forced high with an additional SCLK. It then stays high until new data are ready. This configuration is useful when polling on the status of DRDY/DOUT to determine when to begin data retrieval.

SERIAL CLOCK INPUT (SCLK)

This digital input shifts serial data out with each rising edge. This input has built-in hysteresis, but care should still be taken to ensure a clean signal. Glitches or slow-rising signals can cause unwanted additional shifting. For this reason, it is best to make sure the rise and fall times of SCLK are both less than 50ns.

DATA RETRIEVAL

The ADS1231 continuously converts the analog input signal. To retrieve data, wait until DRDY/DOUT goes low, as shown in Figure 19. After DRDY/DOUT goes low, begin shifting out the data by applying SCLKs. Data are shifted out MSB first. It is not required to shift out all 24 bits of data, but the data must be retrieved before new data are updated (within t_{CONV}) or else the data will be overwritten. Avoid data retrieval during the update period (t_{UPDATE}). If only 24 SCLKs have been applied, DRDY/DOUT remains at the state of the last bit shifted out until it is taken high (see t_{UPDATE}), indicating that new data are being updated. To avoid having DRDY/DOUT remain in the state of the last bit, the 25th SCLK can be applied to force DRDY/DOUT high, as shown in Figure 20. This technique is useful when a host controlling the device is polling DRDY/DOUT to determine when data are ready.

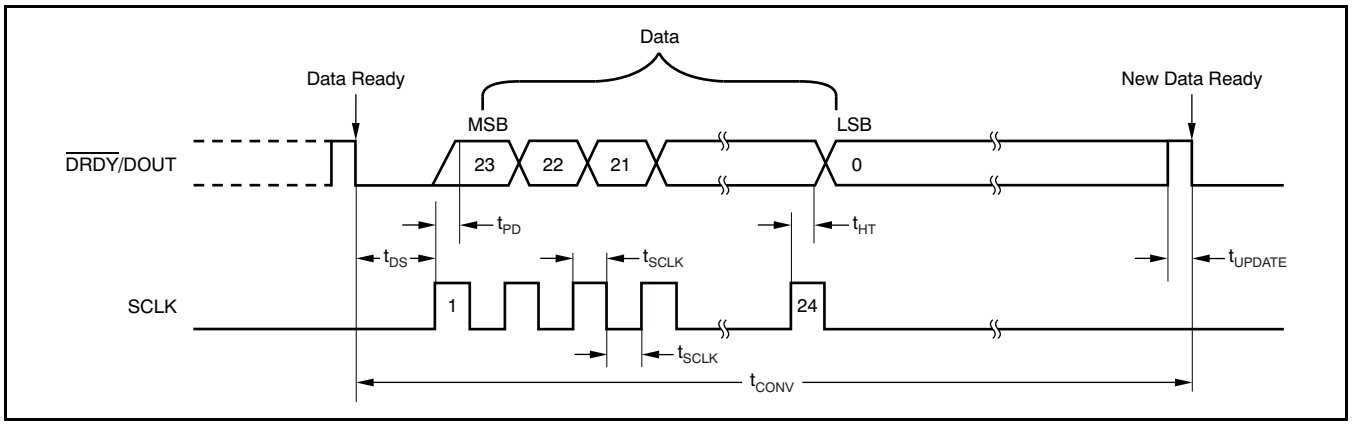


Figure 19. 24-Bit Data Retrieval Timing

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNITS
t_{DS}	DRDY/DOUT low to first SCLK rising edge		0			ns
t_{SCLK}	SCLK positive or negative pulse width		100			ns
t_{PD} (1)	SCLK rising edge to new data bit valid: propagation delay				50	ns
t_{HT} (1)	SCLK rising edge to old data bit valid: hold time		20			ns
t_{UPDATE}	Data updating: no readback allowed			90		µs
t_{CONV}	Conversion time (1/data rate)	SPEED = 1		12.5		ms
		SPEED = 0		100		ms

(1) Minimum required from simulation.

STANDBY MODE

Standby mode dramatically reduces power consumption by shutting down most of the circuitry. To enter Standby mode, simply hold SCLK high after DRDY/DOUT goes low; see Figure 21. Standby mode can be initiated at any time during readback; it is not necessary to retrieve all 24 bits of data beforehand.

When $t_{STANDBY}$ has passed with SCLK held high, Standby mode activates. DRDY/DOUT stays high when Standby mode begins. SCLK must remain high to stay in Standby mode. To exit Standby mode (wake up), set SCLK low. The first data after exiting Standby mode are valid.

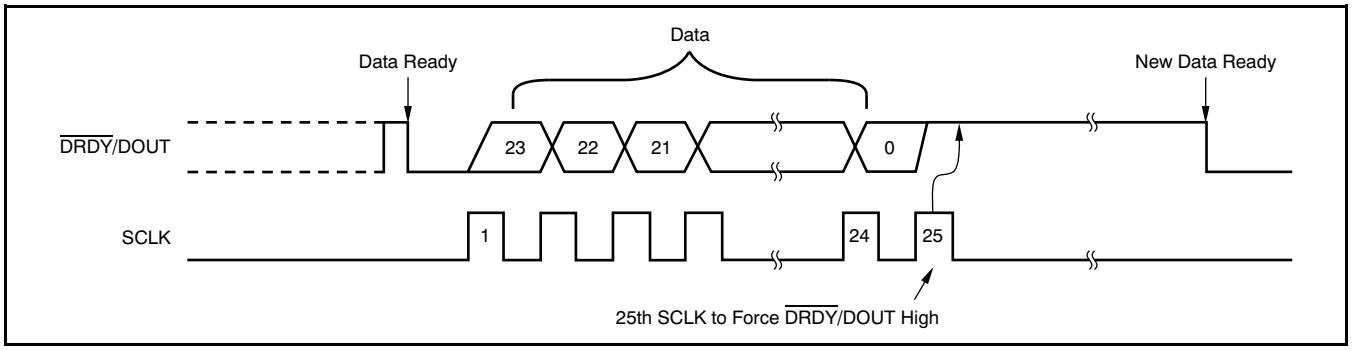


Figure 20. Data Retrieval with DRDY/DOUT Forced High Afterwards

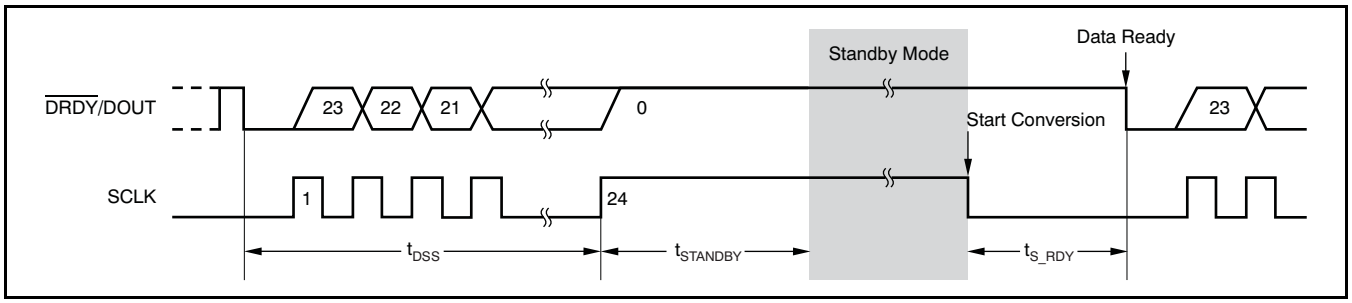


Figure 21. Standby Mode Timing (Can be used for single conversions)

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNITS
t_{DSS} (1)	SCLK high after DRDY/DOUT goes low to activate Standby mode	SPEED = 1			12.44	ms
		SPEED = 0			99.94	ms
$t_{STANDBY}$	Standby mode activation time	SPEED = 1	12.5			ms
		SPEED = 0	100			ms
t_{S_RDY} (1)	Data ready after exiting Standby mode	SPEED = 1		52.6		ms
		SPEED = 0		401.8		ms

(1) Based on an ideal internal oscillator.

POWER-DOWN MODE

Power-Down mode shuts down the entire ADC circuitry and reduces the total power consumption close to zero. To enter Power-Down mode, simply hold the $\overline{\text{PDWN}}$ pin low. Power-Down mode also resets the entire circuitry. Power-Down mode can be initiated at any time during readback; it is not necessary to retrieve all 24 bits of data beforehand. Figure 23 shows the wake-up timing from Power-Down mode.

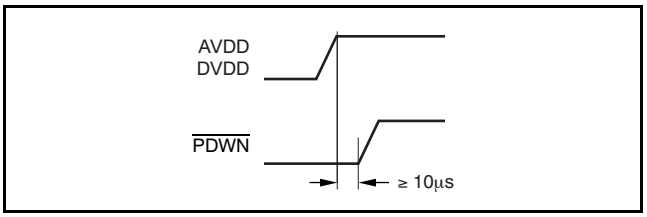


Figure 22. Power-Up Timing Sequence

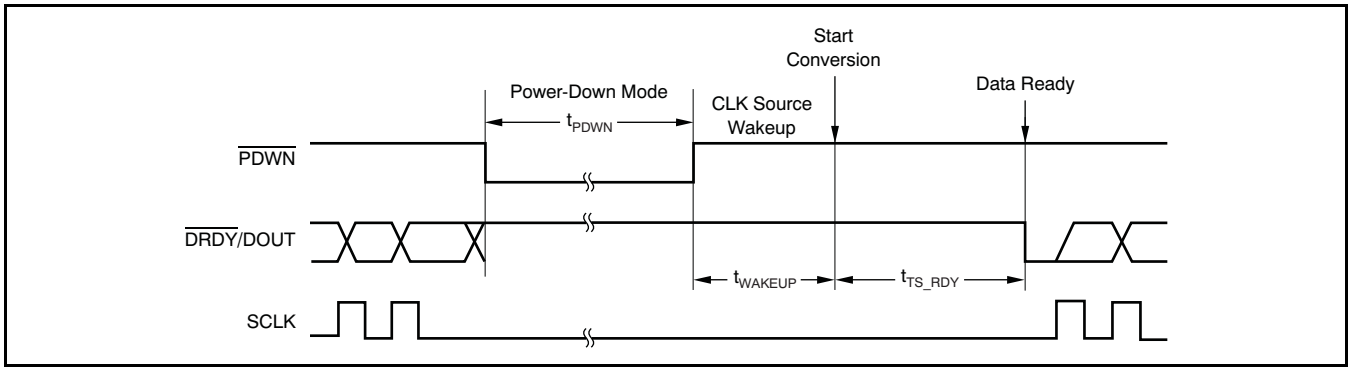


Figure 23. Wake-Up Timing from Power-Down Mode

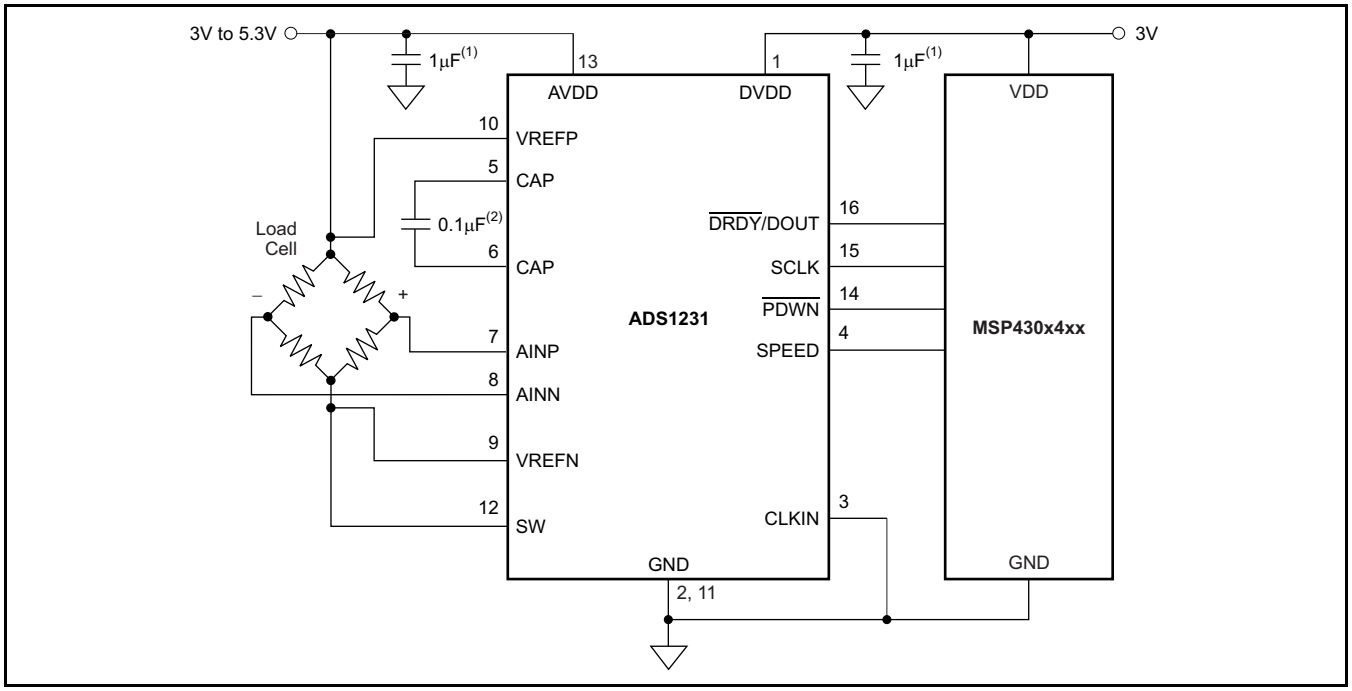
SYMBOL	DESCRIPTION	MIN	TYP	UNITS
t_{WAKEUP} (1)(2)	Wake-up time after Power-Down mode		7.95	µs
t_{PDWN} (1)	$\overline{\text{PDWN}}$ pulse width	26		µs

(1) Based on an ideal internal oscillator.
(2) Typical required from simulation.

APPLICATION EXAMPLE

Weigh Scale System

Figure 24 shows a typical ADS1231 application as part of a weigh scale system.



(1) Place a 0.1µF or higher capacitor as close as possible on both AVDD and DVDD.

(2) Place capacitor very close to the ADS1231 CAP pins for optimal performance.

Figure 24. Weigh Scale Example

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2010) to Revision D **Page**

- Changed "oscillator" to "clock" in data rate parameter of electrical characteristics 3
- Changed all "f_{CLK}" to "f_{CLKIN}" throughout data sheet 3
- Deleted extra space in data rate parameter typical value (typo) 3
- Changed "oscillator" to "clock" in data rate parameter of electrical characteristics 3
- Deleted extra space in data rate parameter typical value (typo) 3
- Changed location of noise parameter 3
- Changed "oscillator" to "clock" in normal-mode rejection parameter of electrical characteristics 3
- Changed "AGND" to "GND" in negative reference input parameter min value 3
- Added new external clock input frequency parameter 3
- Changed "oscillator" to "f_{CLKIN}" in note 2 of electrical characteristics 3
- Changed pin 12 name from PSW to SW in pinout drawing 5
- Changed pin 12 name from PSW to SW in Pin Descriptions table 5
- Changed title of Figure 5 7
- Changed title of Figure 6 7
- Changed plot title and X-axis label of Figure 9 8
- Changed plot title and Y-axis label of Figure 11 8
- Changed plot title and Y-axis label of Figure 12 8
- Changed *Clock Source* section 10
- Added text to first sentence of *Frequency Response* section 11
- Changed third paragraph of *Frequency Response* section 11
- Added new text to end of *Frequency Response* section 11
- Changed Table 2 12
- Changed pin numbers in Figure 24 to match the device pinout and added missing CLKIN pin 16

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS1231ID	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1231
ADS1231IDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1231

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

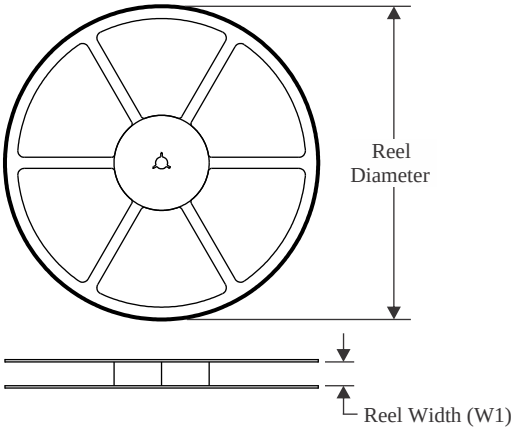
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

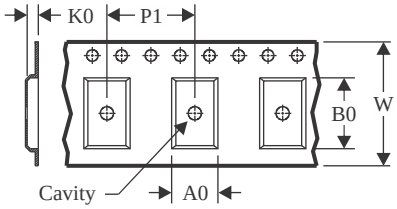
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

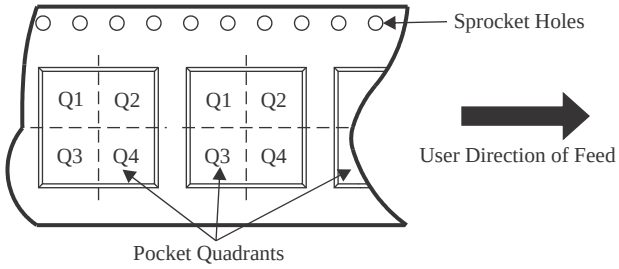


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

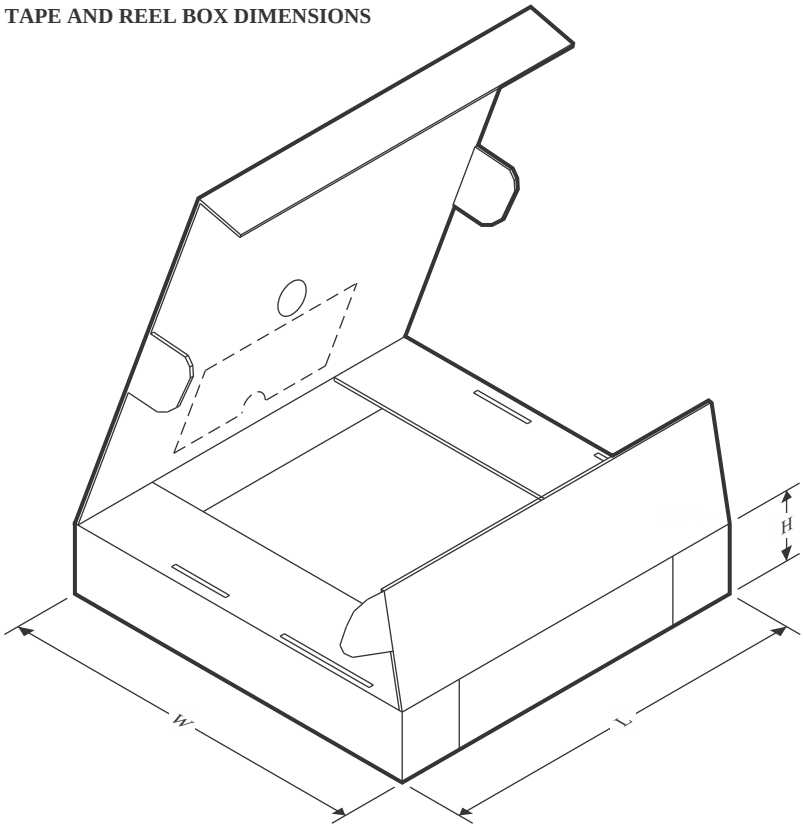
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1231IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

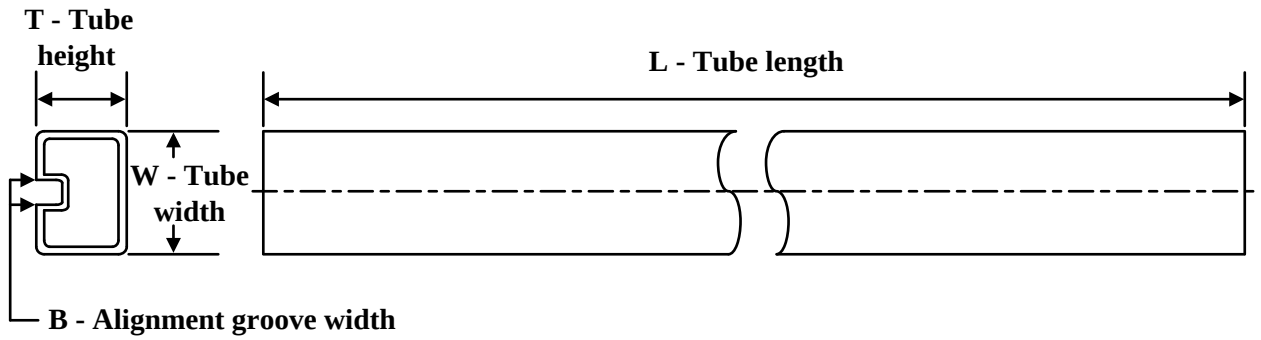
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1231IDR	SOIC	D	16	2500	353.0	353.0	32.0

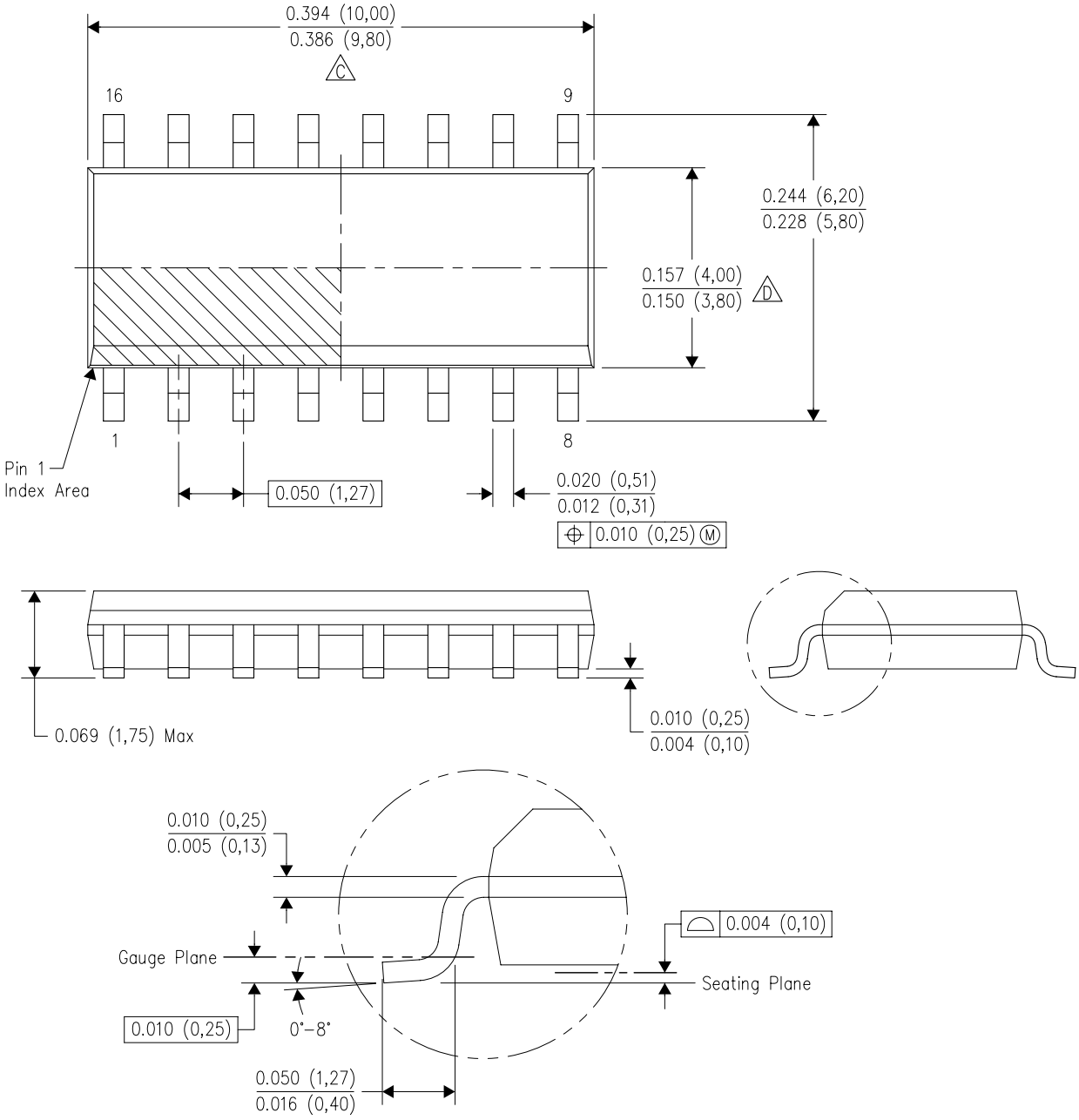
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS1231ID	D	SOIC	16	40	507	8	3940	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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