Application Brief

Power-Supply Design for Sitara AM62A/P/D(-Q1) Using TPS6522430-Q1 and TPS6522230-Q1 PMICs

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This application brief shows the design considerations for implementing the TPS6522x-Q1 PMIC in systems the need compact, safe and cost-effective multi-rail power delivery like digital clusters, driver monitoring systems, camera mirrors and industrial vision modules. As embedded processors like the Sitara™ and Jacinto™ Processors become increasingly central to ADAS and infotainment platforms, power solutions must scale with performance demands while staying within strict size, thermal and reliability constraints.

The TPS65222-Q1 and TPS65224-Q1 address these challenges by integrating four high-efficiency buck converters and three configurable low-dropout regulators into a single 5x6mm package. With support for 5.5A single and dual phase buck operation up to 10A. It is capable of powering high-performance SoCs while reducing board space and BOM complexity. The PMIC also includes integrated power sequencing logic and GPIO-configurable PDN profiles, allowing reusability across multiple system configurations with minimal hardware changes. For variants that include an internal 12-bit ADC, *such as the TPS65224-Q1*, voltage telemetry enables in system monitoring of critical rails for diagnostic and safety assurance.

Functional safety is a cornerstone of the TPS6522x-Q1 design. Developed with ISO26262 in mind, it meets ASIL-B hardware integrity requirements and includes built-in protections like an integrated watchdog, over/undervoltage monitoring, thermal shutdown, and error signal management.

Device Versions

There are three different variants with the same functionality but slightly different features that are highlighted in Table 1. In this document, all these devices are referenced with TPS6522x30-Q1.

Table 1. Device Versions

Generic Part Number (GPN)	Orderable Part Number	ADC	Package
TPS65224-Q1	TPS6522430RAHRQ1	Yes	Non-Wettable Flank
	TPS6522430WRAHRQ1	Yes	Wettable Flank
TPS65222-Q1	TPS6522230WRAHRQ1	No	Wettable Flank

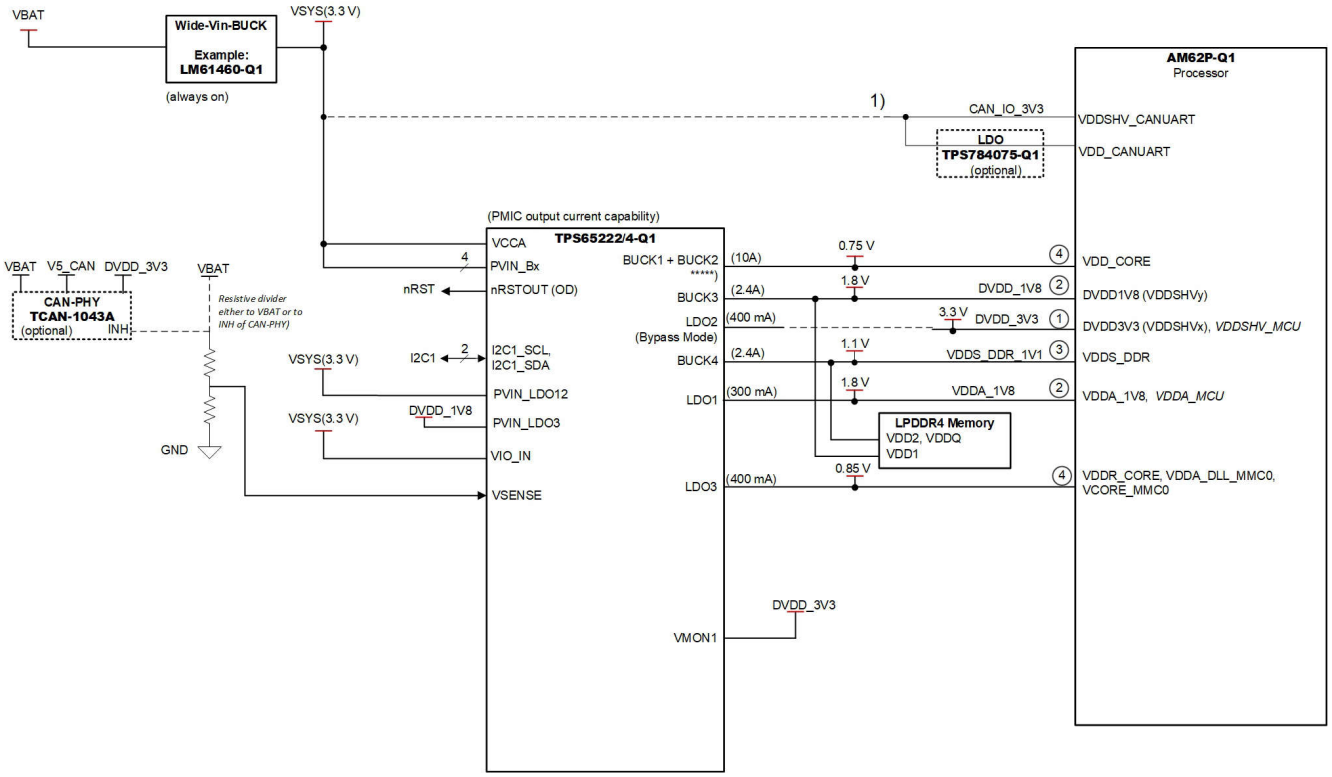

Figure 1. Block Diagram

Optional components are available for integration. Certain use cases may require these to achieve full functionality.

For a more detailed power design user's guide and supported use cases, request access at the following link: *https://www.ti.com/drr/opn/TPS6522X-DESIGN-RESOURCES to make integration as easy as possible.*

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