Application Note

How to Use 650V GaN in 800V Battery Applications

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ABSTRACT

A Stacked Half Bridge (SHB) circuit and new control methodology based on Phase Shift Full Bridge (PSFB) are introduced for automotive high-voltage (HV) to low-voltage (LV) DC/DC applications. The new topology enables the use of high frequency performance 650V-rated switches in 800V battery systems. With a special control scheme, the SHB-PSFB can realize voltage balance on the split input capacitors, and let the switches in the series stack achieve ZVS or sufficient ZVS to maintain the required efficiency. This application note discusses the detailed operation principles and experimental results.

Table of Contents

Trademarks

1 Introduction

In EV applications, more and more vehicle vendors use 800V batteries. At the high voltage battery side, customer tends to use 1200V power switches, which are high-cost, high Rdson and poor high frequency performance compared to 650V power switches. Is there a way to use 650V switches in 800V battery application?

Three Level (TL) topology is one of the candidates that enables 650V switches used in 800V battery system. In I-type TL topology, as Figure 1-1 and Figure 1-2 show. No matter the non-isolated or isolated scenario, the main components are four switches in series, and two clamping diodes. Take isolated TL for example, one terminal of magnetic connects to middle of four switches, another terminal connects to middle of two series input capacitors. The control scheme is that in first mode switch Q1 and Q2 turn on, while switch Q3 and Q4 are off. The next mode switches Q3 and Q4 turn on after switches Q1 and Q2 are off. Those two modes repeat alternately.

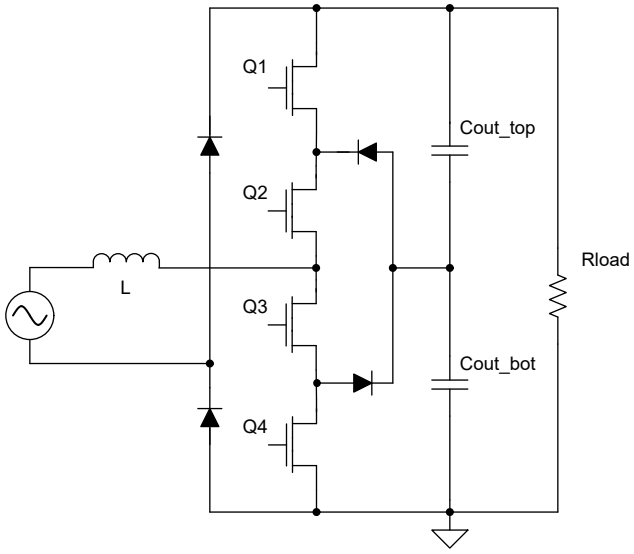

Figure 1-1. Non-Isolated TL Topology

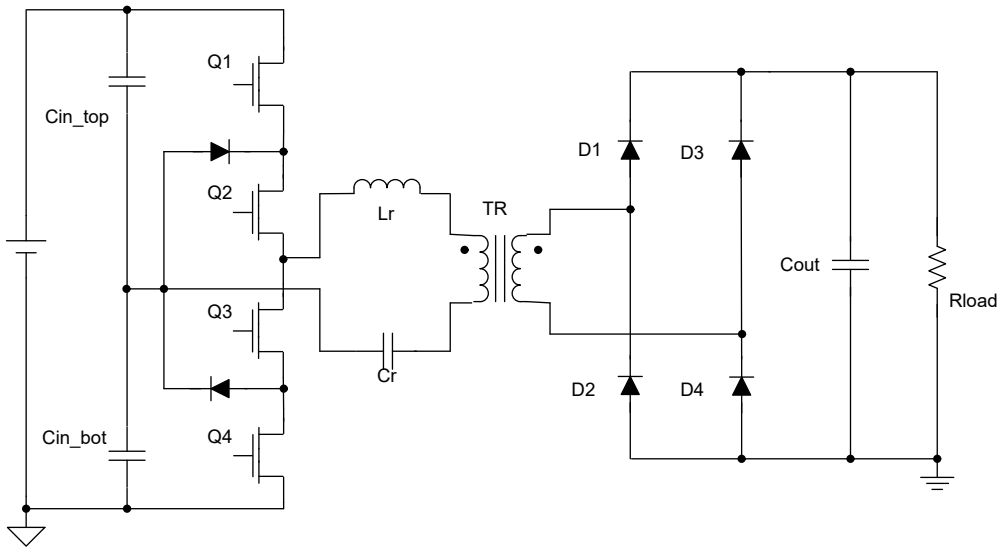

Figure 1-2. Isolated TL Topology

Stacked Half Bridge (SHB) is another option. As Figure 1-3 shows, a lot of differences are shown between TL and SHB. For SHB, main components are four switches in series, and one high voltage-rated DC block capacitor. One terminal of magnetics connects to the middle of the upper two switches. Another terminal connects to the middle of the lower two switches. The control scheme is also different with that of TL topology.

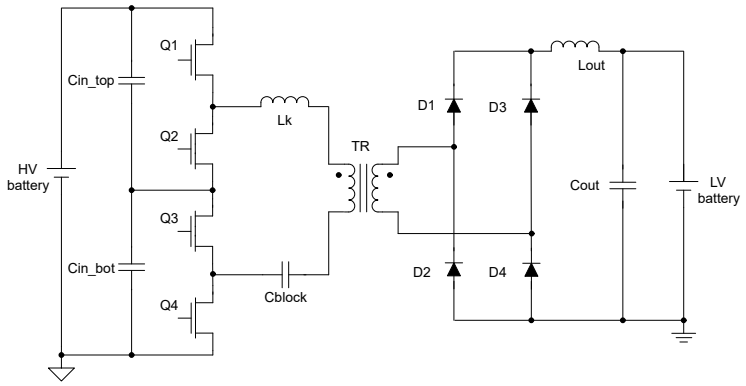

Figure 1-3. SHB Topology

In high voltage to low voltage DCDC and OBC applications, compared to TL topology, SHB has no clamping diode, which leads to high power density. This topic is dedicated to SHB topology.

2 SHB Topology in Primary Side

As shown in Figure 2-1, at stage t0 to t1, switches Q1 and Q4 can turn on together while switches Q2 and Q3 are off , the current is shown in the blue arrows. At stage t3 to t4, switch Q2 and Q3 can turn on after switch Q1 and Q4 are off. The current is shown by the green arrows. At stage t1 to t2 and t3 to t4, all MOSFETs are off, and the current is zero.

With the above control scheme, the Imid is zero. That means the top capacitor and the bottom capacitor can charge and discharge at the same time, the middle voltage of the two input caps are half of input voltage. This control scheme is designed for Hard Switch Half Bridge (HSFB), LLC, and Single Phase Shift Dual Active Bridge (SPSDAB), but not for Phase Shift Half Bridge (PSFB). This turns out to be much more complicated for phase shift control. This is explained in details in the following sections.

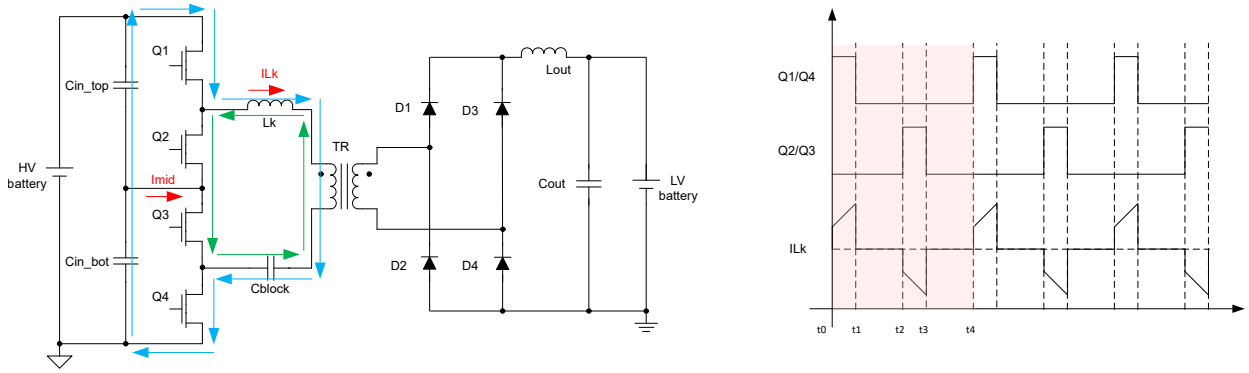

Figure 2-1. SHB Topology and Control Scheme

Figure 2-2 shows the Simplis simulation results for HSFB SHB control. Vmid is the middle voltage of input series capacitors, Imid is current goes in and out middle point. The Imid remains zero through the time zone, so there is no Middle Voltage Balance Issue (MVBI) here. Make sure that the on the DC bias voltage on the block capacitor is half of the input voltage.

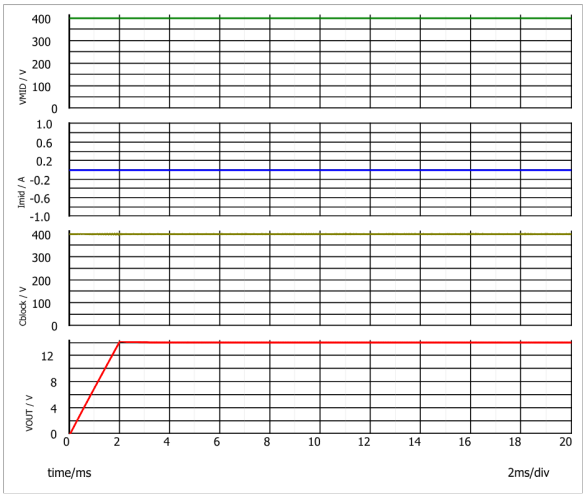

Figure 2-2. Simulation Results for HSFB SHB Control

With the original PSFB control scheme, as Figure 2-3 shows, the middle voltage of the two series input capacitors can be unbalanced, which means the voltage of each input capacitors is not Vin / 2. The main reason is due to the circling current in the primary side, which can keep discharging one capacitor while another capacitor is in balance.

Here, the voltage stress of upper two switches is up to the upper capacitor. The voltage stress of lower two switches is up to lower capacitor.

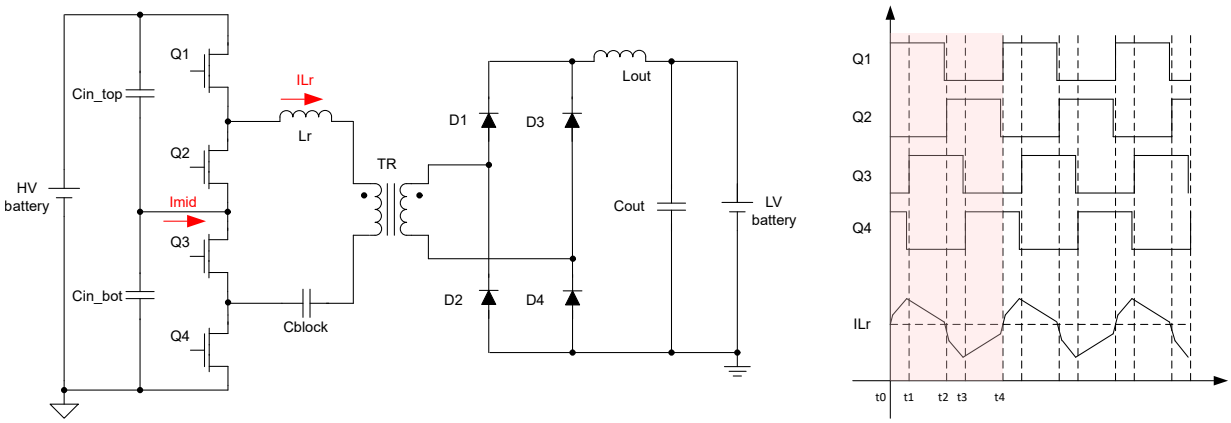

Figure 2-3. PSFB SHB Control with Original Control

From the simulation results shown in Figure 2-4, the under steady state, the Vmid can finally achieve a stable value. The stable value depends on the load. The heavier load, the larger voltage vibration of Cin_top and Cin_bot. Under certain transient condition, such as OCP or short, the middle voltage can become quite large (or quite small), which can lead to switch failure. This is why there is a user must pay attention to MVBI.

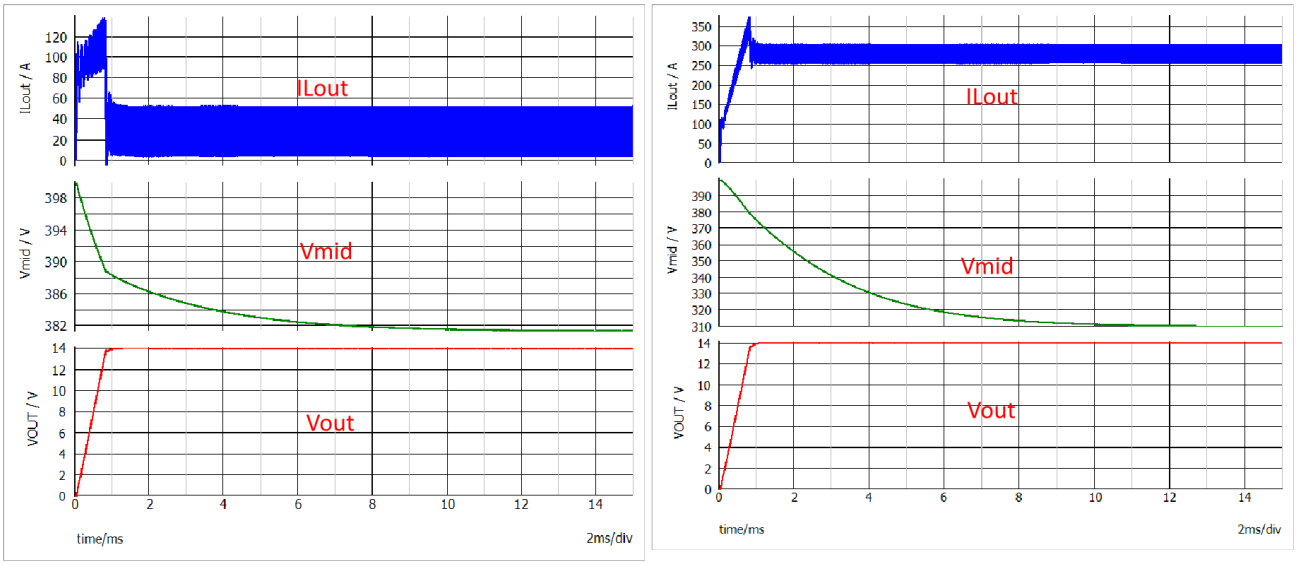

Figure 2-4. Simulation Results for PSFB SHB with Original Control

Figure 2-5 and Figure 2-9show the root cause of middle voltage balance issue.

At stages T0 to T1, Q1 and Q4 are on, Q2 and Q3 are off, the current flow path is as the blue arrows shows. No current can flow in or out to Imid. Cin_top and Cin_bot are discharging.

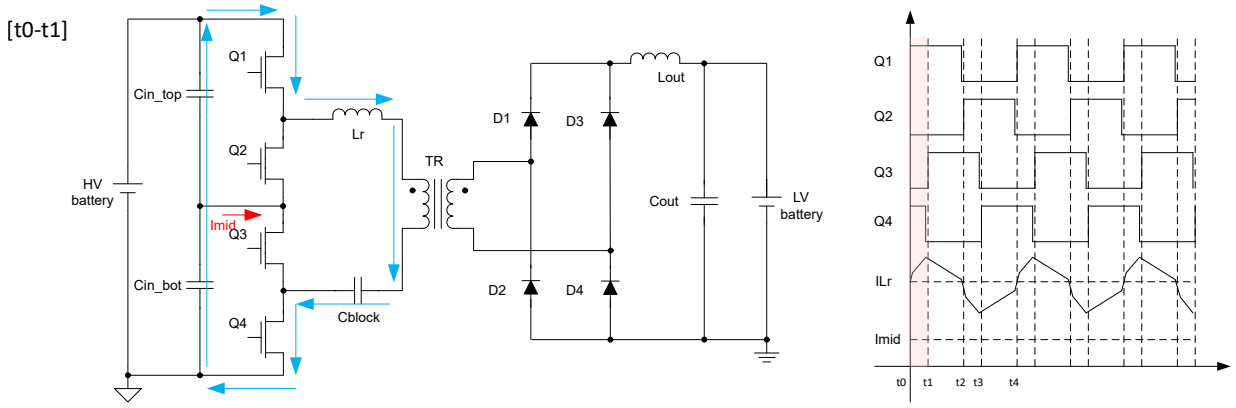

Figure 2-5. Stage (T0, T1) for PSFB SHB with Original Control

At stages T1 to T2, Q1 and Q2 are on, Q3 and Q4 are off, the current flow path is as the blue arrow shows. Negative Imid happens. Cin_top is still discharging.

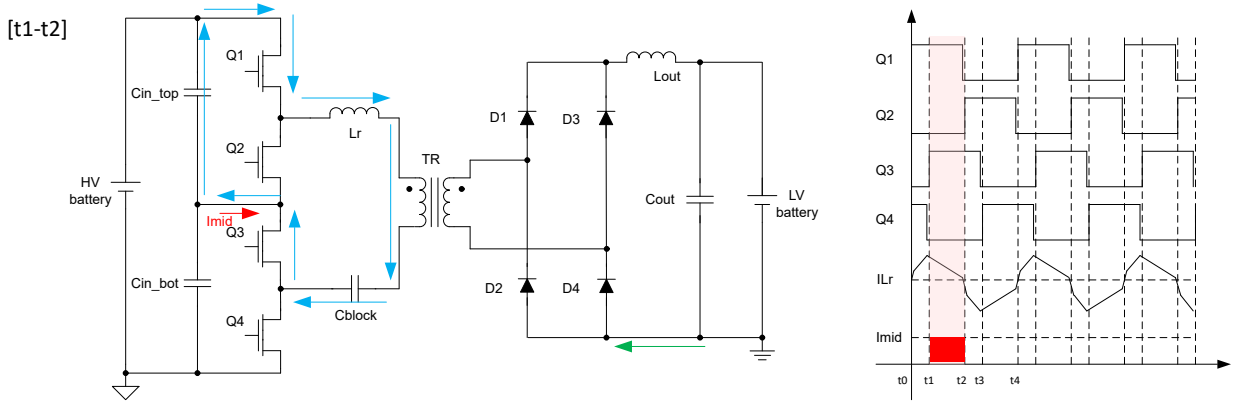

Figure 2-6. Stage (T1, T2) for PSFB SHB with Original Control

At stages T2 to T3, Q2 and Q3 are on, Q1 and Q4 are off, the current flow path is as the blue arrows show. No current can flow in or out to Imid.

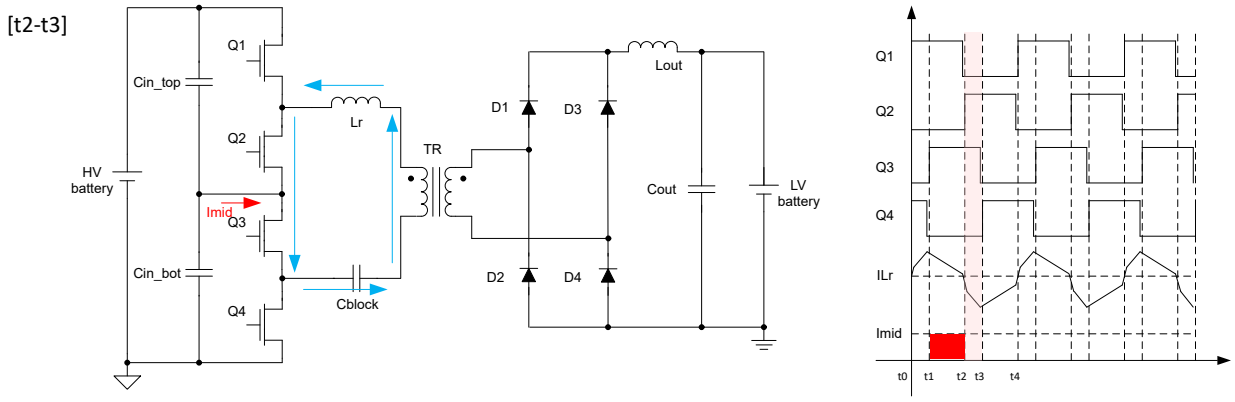

Figure 2-7. Stage (T2, T3) for PSFB SHB with Original Control

At stage T3 to T4, Q2 and Q4 are on, Q1 and Q3 are off, the current flow path is as the blue arrows show. Negative Imid again. Cin_bot is charging.

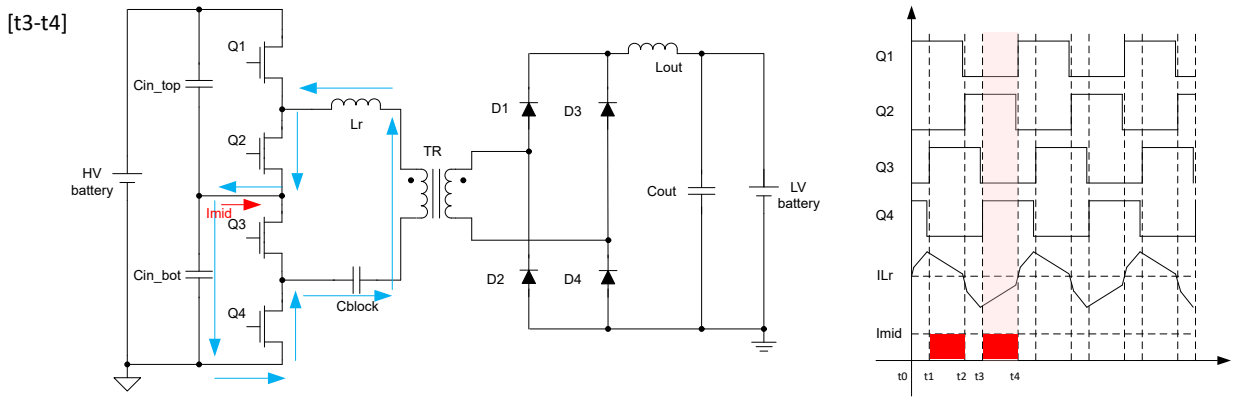

Figure 2-8. Stage (T3, T4) for PSFB SHB with Original Control

Imid keeps the same direction in four stages, that makes Cin_top always discharging, while Cin_bot charging and discharging one time for each. So, middle voltage balance issue happens. And the vibration voltage can be calculated using Equation 1 . This is proportional to Iout.

$$Vbri = (2 \times Lr \times ((Iout + 0.5 \times \Delta IL)/Nps))/Toff \quad (1)$$

where: Toff is the cycling current time in half period.

Nps is the turn ratio of transformer

ΔIL is the ripple current of output choke

The root cause is related to the cycling current. How to fix this? The basic idea is energy flows in or out of Cin_top or Cin_bot can the equal. That means we need to neutralize the Imid in one switching period.

One feasible plan is proposed as Figure 2-9 shows. In first half cycle marked in pink, Imid can flow through Cin_top twice, and in another half cycle marked in blue, Imid also can flow through Cin_bot twice. In each half cycle, the direction of Imid can reverse, Cin_top or Cin_bot can charge one time and discharge one time. So the middle voltage of input capacitors is balanced.

The following sections show the details of each step from Figure 2-9 to Figure 2-17.

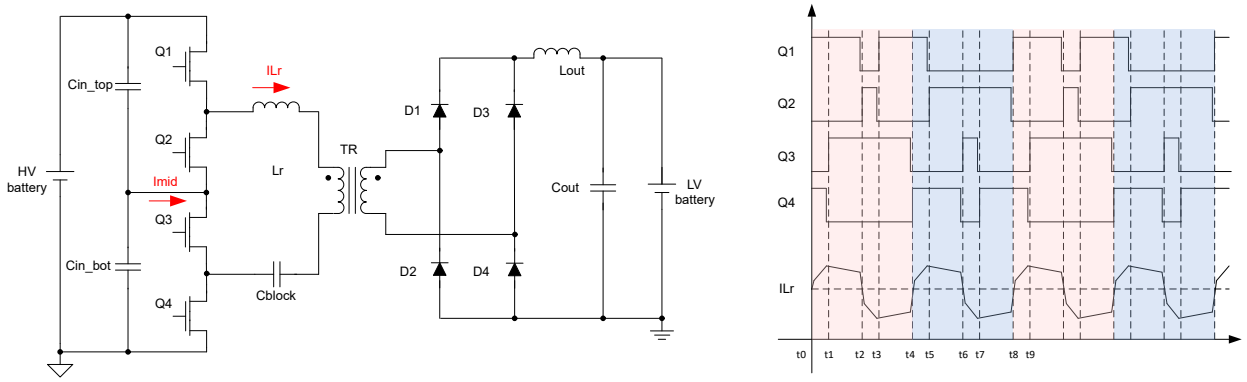

Figure 2-9. PSFB SHB with Proposed Control

At stages T0 to T1, Q1 and Q4 are on, Q2 and Q3 are off. The current flow path is as the blue arrow shows. No current can flow in or out to Imid. Cin_top and Cin_bot are discharging.

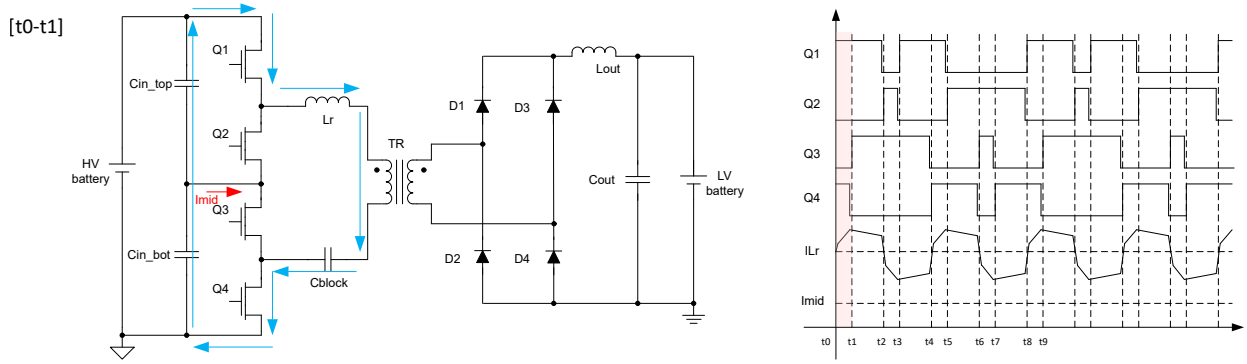

Figure 2-10. Stage (T0, T1) for PSFB with Proposed Control

At stages T1 to T2, Q1 and Q2 are on, Q3 and Q4 are off, the current flow path is as the blue arrow shows. Negative Imid happens. Cin_top is still discharging.

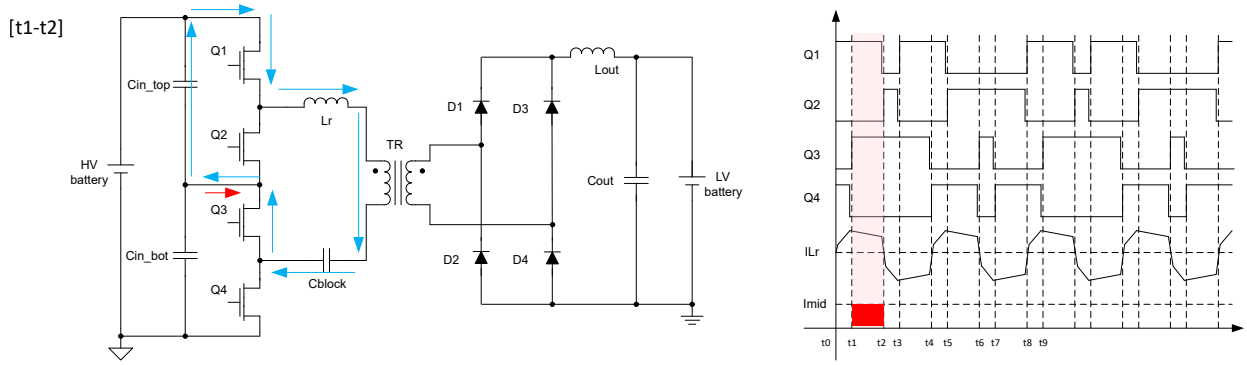

Figure 2-11. Stage (T1, T2) for PSFB SHB with Proposed Control

At stages T2 to T3, Q2 and Q3 are on, Q1 and Q4 are off, the current flow path is as the blue arrow shows. No current can flow in or out to Imid.

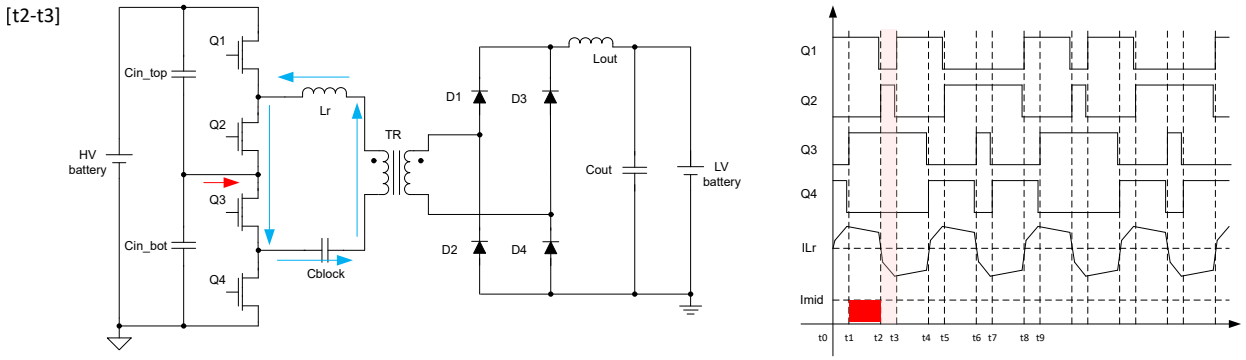

Figure 2-12. Stage (T2, T3) for PSFB SHB with Proposed Control

At stages T3 to T4, Q2 and Q4 are on, Q1 and Q3 are off, the current flow path is as the blue arrow shows. Positive Imid. Cin_top is charging.

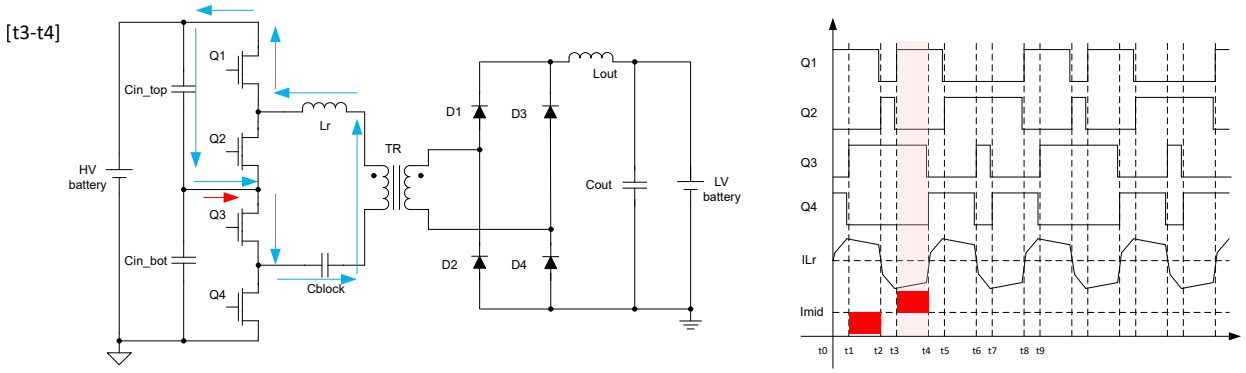

Figure 2-13. Stage (T3 to T4) for PSFB SHB with Proposed Control

In first half cycle, Imid can flow through Cin_top twice on reverse direction, so voltage of Cin_top keeps similar with original value.

At stages T4 to T5, Q1 and Q4 are on, Q2 and Q3 are off, the current flow path is as the blue arrow shows. No current can flow in or out to Imid. Cin_top and Cin_bot are discharging.

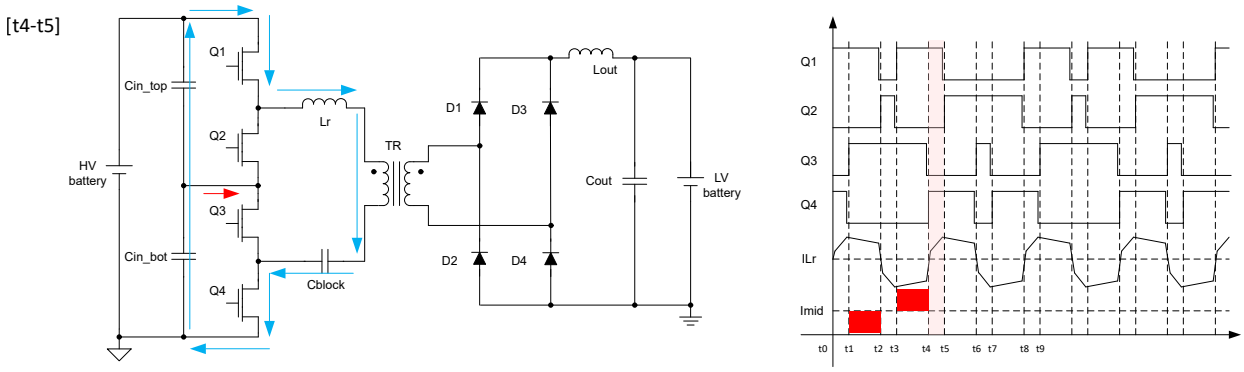

Figure 2-14. Stage (T4, T5) for PSFB SHB with Proposed Control

At stages T5 to T6, Q2 and Q4 are on, Q1 and Q3 are off, the current flow path is as the blue arrow shows. Positive Imid happens. Cin_bot is still discharging.

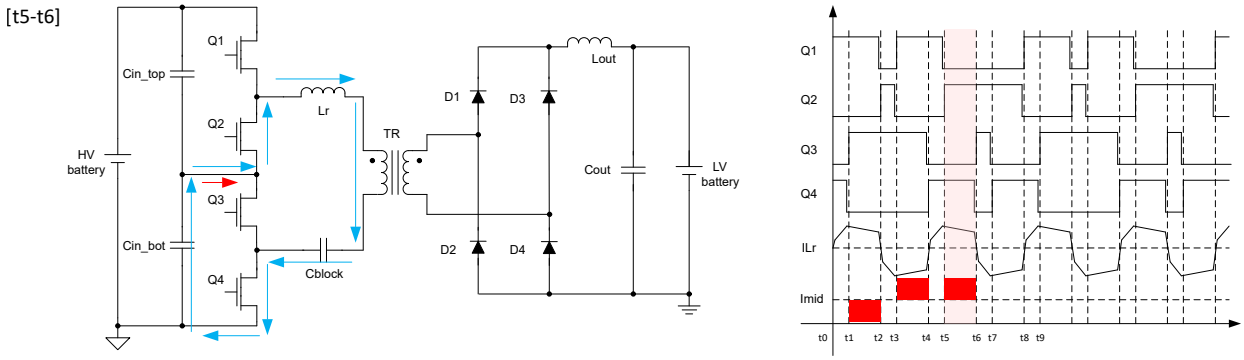

Figure 2-15. Stage (T5, T6) for PSFB SHB with Proposed Control

At stages T6 to T7, Q2 and Q3 are on, Q1 and Q4 are off, the current flow path is as the blue arrow shows. No current can flow in or out to Imid.

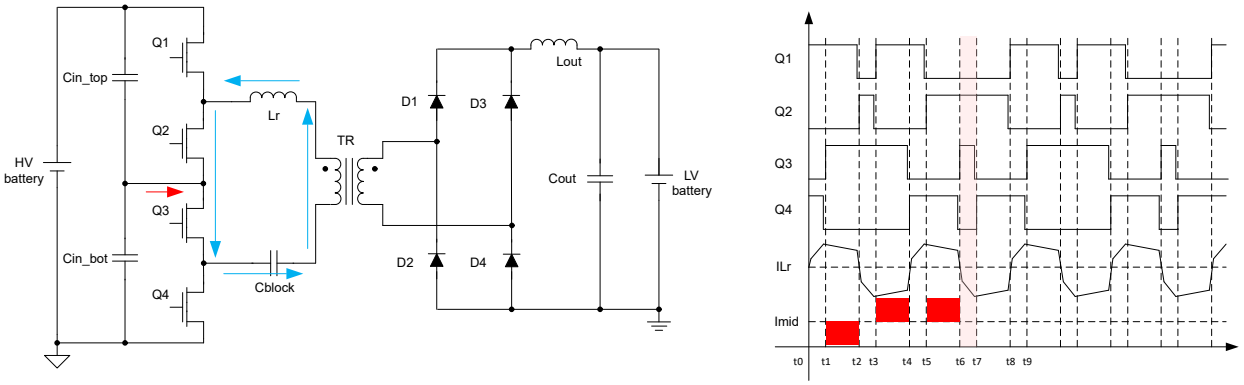

Figure 2-16. Stage (T6, T7) for PSFB SHB with Proposed Control

At stages T7 to T8, Q2 and Q4 are on, Q1 and Q3 are off, the current flow path is as the blue arrow shows. Negative Imid. Cin_bot is charging.

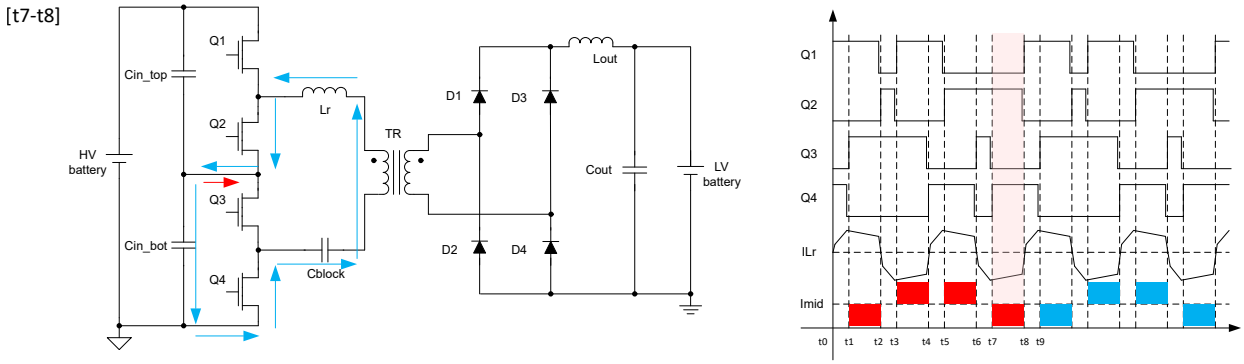

Figure 2-17. Stage (T7, T8) for PSFB SHB with Proposed Control

In the second half of the cycle, Imid also can flow through Cin_bot twice on reverse direction, so voltage of Cin_bot keeps Vin/2.

With this design, the middle voltage balance issue is resolved. But the PWM is quite complex, this needs two pulses in one cycle. Most MCU devices cannot do that. TI's new generation of C2000 devices have proposed Type-5 ePWM features, which has eight extended compare registers. Instead of generating a single pulse within a single PWM period, generation of up to a maximum of four pulses within a single PWM period is possible.

Note that the type-5 feature is not supported for all C2000 devices. Only up-mode can be used in type-5. The F28P65X series is used in this application note.

Figure 2-18 provides an example of generating two pulses in one PWM period. By allocating XCMP1-4 to CMPA and XCMP5-8 to CMPB, a user can obtain two independent PWMs with two pulses in one PWM period.

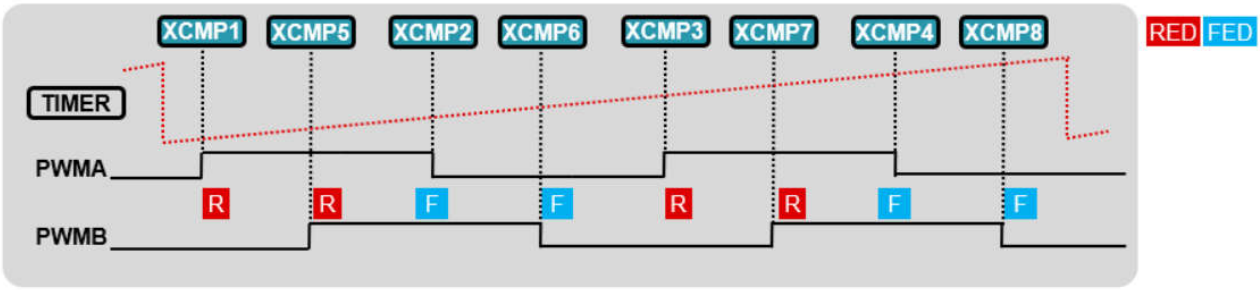

Figure 2-18. Using Type 5 to Generate Two Pulses in One Period

The designed switching frequency of PMP41139 is 200kHz, but time base clock (TBCLK) can be set to 100kHz because the current in the resonant tank can cycle twice. Figure 2-19 shows the type 5 ePWM configuration for proposed control scheme.

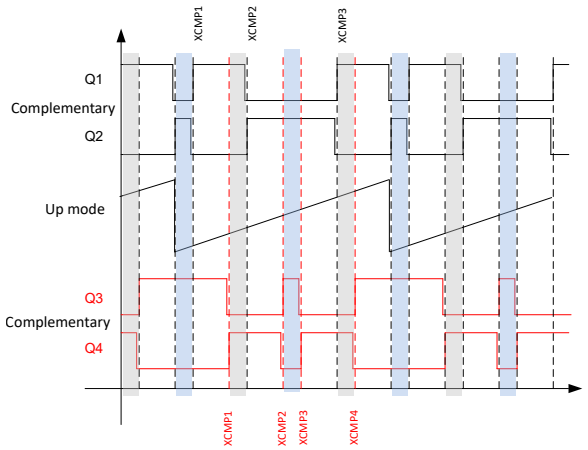

Figure 2-19. Type 5 EPWM Setup for PSFB SHB with Proposed Control

Q1 and Q2 are complementary; set XCMP1-3 to Q1.

Q3 and Q4 are complementary; set XCMP1-4 to Q3.

When using type-5, several XCMP values for PWM must be updated. Is there a simple way to achieve the same PWM? Can type-4 be used?

The answer is yes. The pink area and blue area have axial symmetry, as shown in Figure 2-20. In the pink area, only CMPA and CMPB must be set to obtain Q1, and in the blue area, exchange the CMPA and CMPB value to obtain Q1.

In PMP41139, use this method to output the desired PWM.

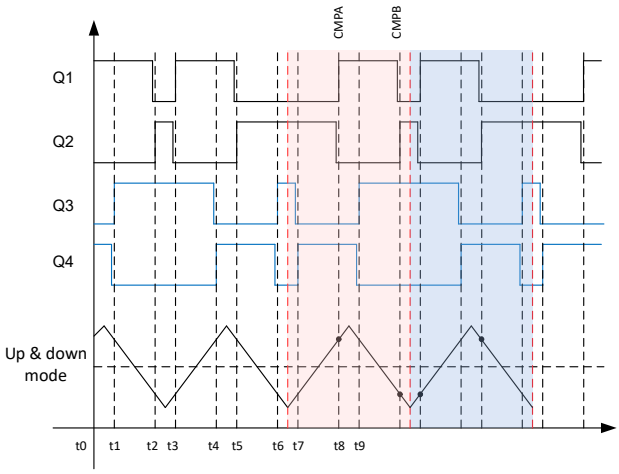

Figure 2-20. Type 4 EPWM Setup for PSFB SHB with Proposed Control

3 SHB Topology in Secondary Side

The SHB design mentioned previously is at the primary side. This also can be moved to the secondary side. The main components, connection and control scheme is the same with that at primary side without phase shift.

Figure 3-1 shows an example of using SHB as synchronous rectifier in CLLLC topology. Q5 and Q8 turn on together, Q6 and Q7 turn on together. There is no Imid current flow, and no middle voltage balance issue.

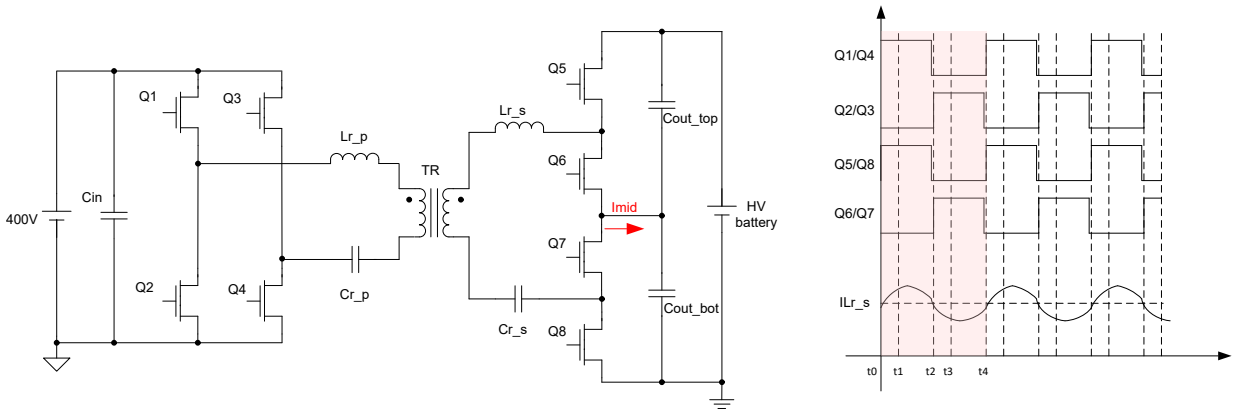

Figure 3-1. SHB Topology in Secondary Side and Control Scheme

The simulation results in Figure 3-2 proves the previous viewpoint.

- Red: output voltage
- Green: middle voltage
- Blue: voltage of resonant capacitor

Notice that there is a ½ Vout DC bias voltage on resonant capacitors.

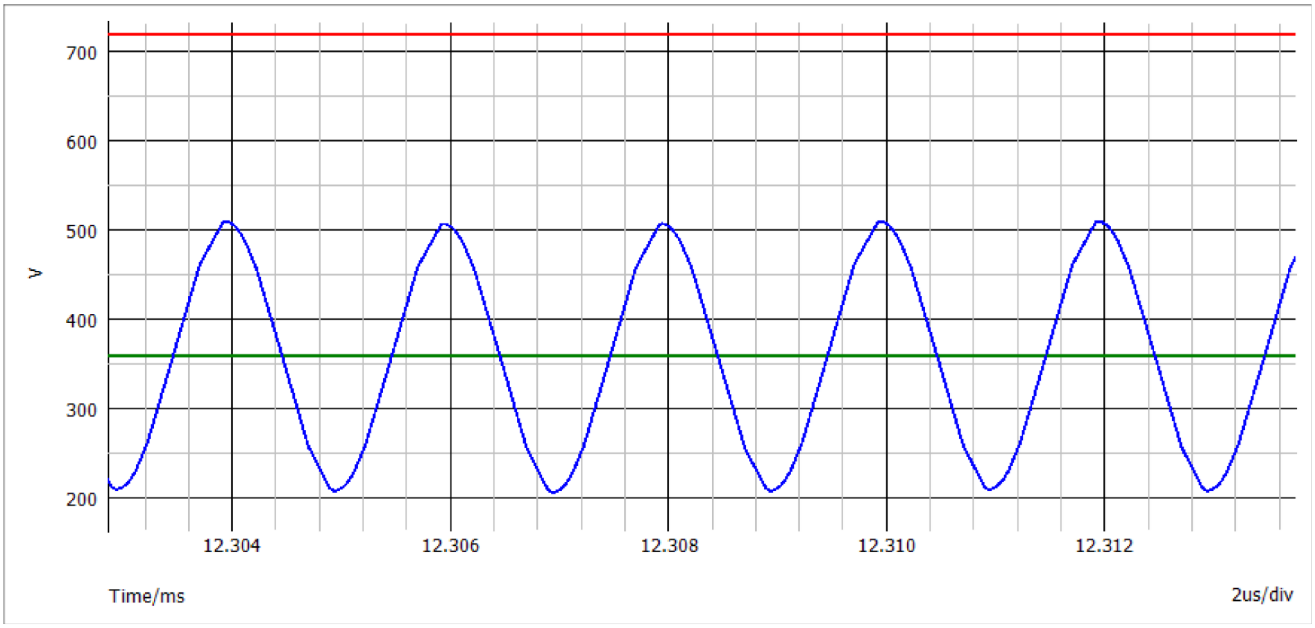

Figure 3-2. Simulation Results for CLLLC SHB SR Control

4 Test Results

PMP41139 is an automotive 3.5kW 800V to 14V DC/DC converter reference design, in which we used 650V rated GaN device LMG3522R030-Q1 as primary switches Q1 to Q4, as Figure 4-1 shows. The input voltage ranges from 400V to 900V. Table 4-1 shows the differential value with or without proposed control. The test condition is 400Vin, 13.5Vout, 100A load. With proposed control, voltage unbalance is reduced from 28V to 2V. The improvement of middle voltage balance issue is shown in Figure 4-2.

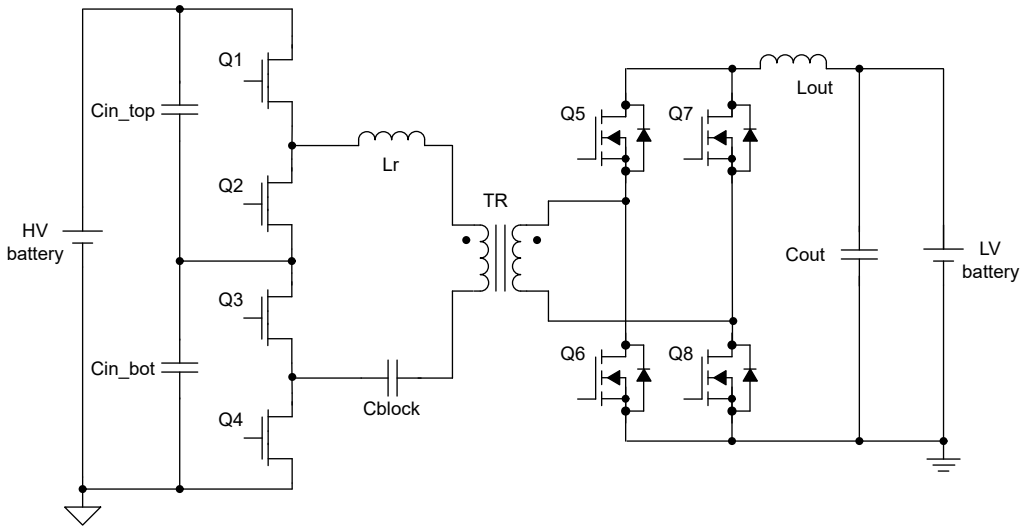

Figure 4-1. PMP41139 Schematic Diagram

Table 4-1. Differential Value between Cin_top and Cin_bot With or Without Proposed Control

Control Scheme	VCin_top	VCin_bot	VCap_diff
Without proposed control	218V	190V	28V
With proposed control	204V	202V	2V

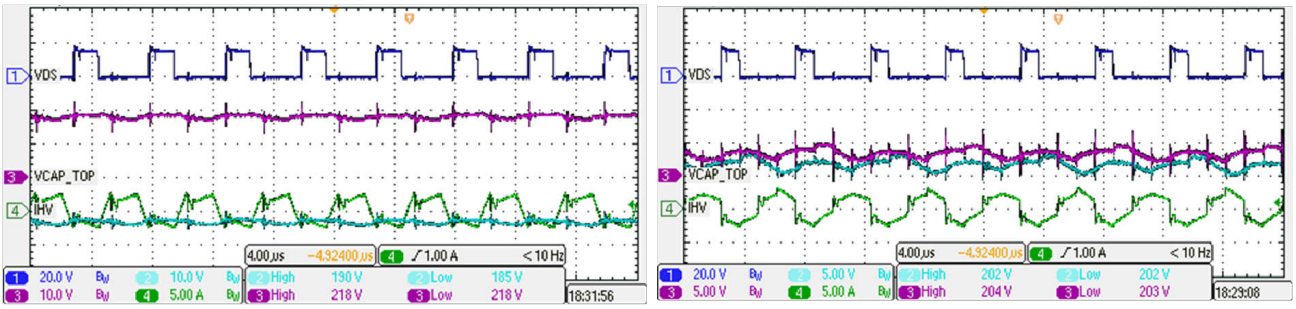

Figure 4-2. Waveforms of PSFB SHB With or Without Proposed Control

- CH1: Vgs of Q5
- CH2: VCin_bot
- CH3: VCin_top
- CH4: Current of PSFB resonant tank

The middle voltage of Cin in different Vin and load is shown in Figure 4-3. The results turn out to be that middle voltage is close to half of input voltage, the maximum deviation is no more than 5V.

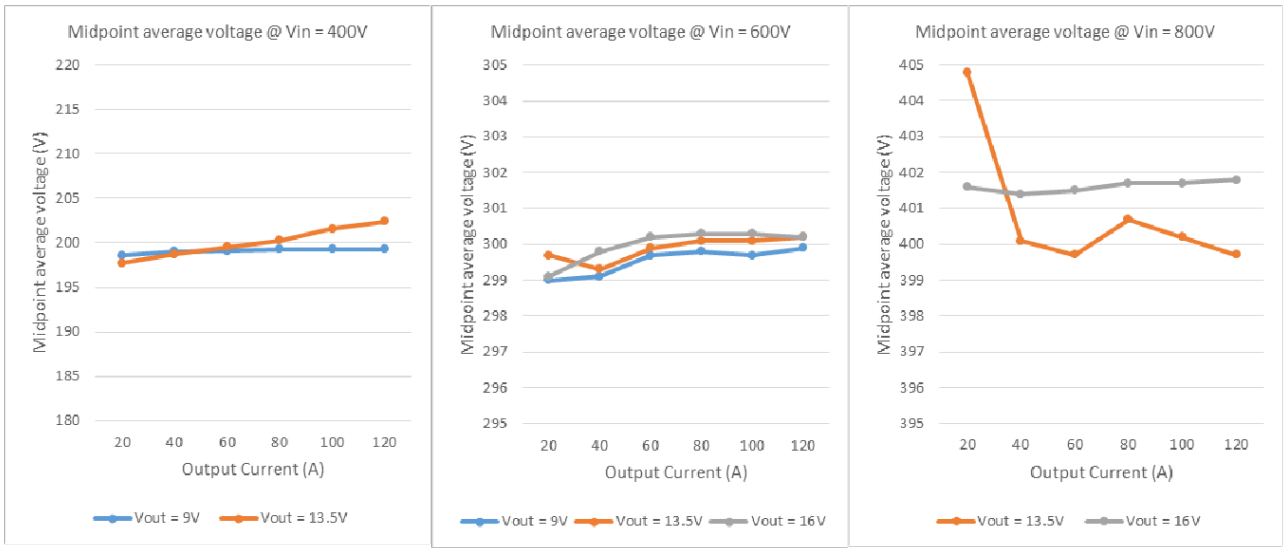

Figure 4-3. Middle Voltage VS Load at Different VIN

PMP23461 is a 400V to 800V CLLLC converter reference design, in which a 650V rated GaN device LMG3522R030-Q1 is used as secondary switches Q5 to Q8, as Figure 4-1 shows. The output voltage ranges from 400V to 900V. Table 4-2 shows the voltage of Cout_top and Cout_bot at different Vin and load. As is analyzed in theory, the CLLLC topology has no middle voltage balance issue. What is tested in low output voltage shows the middle point voltage deviation is with 5V even though there is no balance control, as shown in Figure 4-5 and Table 4-2. The existing deviation is mainly due to layout asymmetry of the SHB top two switches and the bottom two switches.

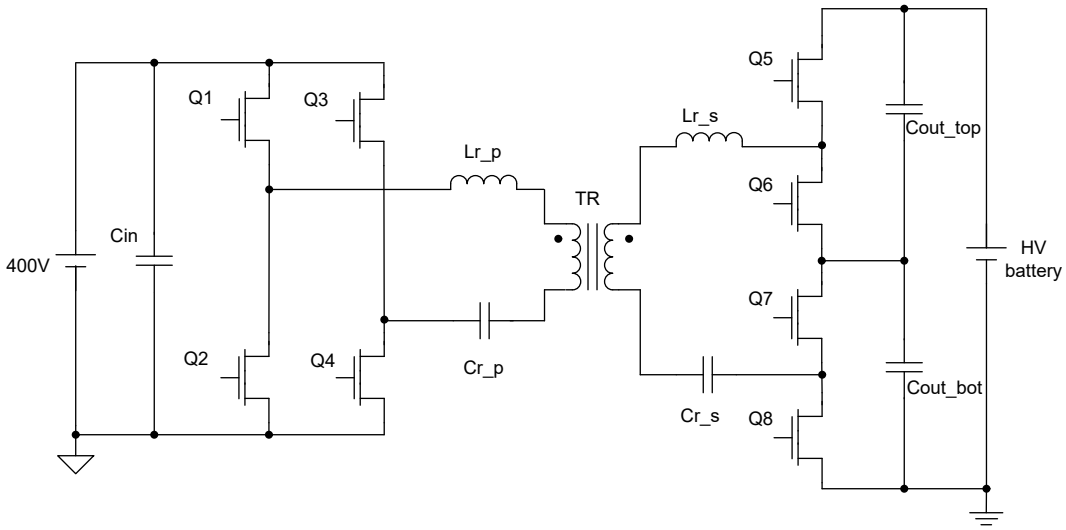

Figure 4-4. PMP23461 Schematic Diagram

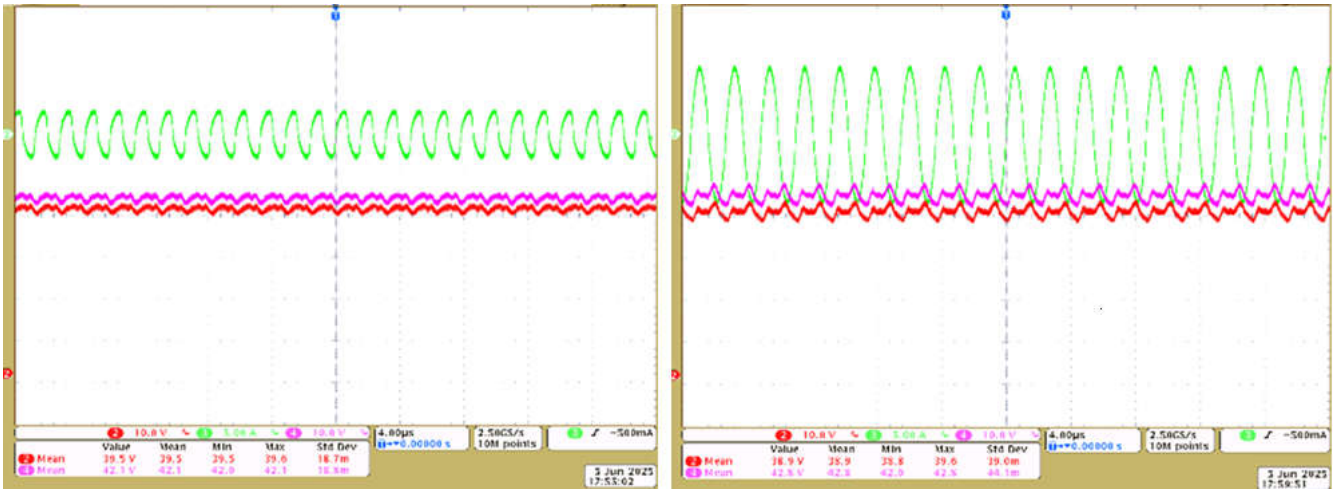

Figure 4-5. Waveforms of CLLLC SHB SR at Different Load

Table 4-2. Voltage of Cout at Different Vin and Load

	Vin=50V Vout=80V/1A	Vin=50V Vout=80V/2A	Vin=50V Vout=80V/3A	Vin=100V Vout=170V/1A	Vin=100V Vout=170V/2A	Vin=100V Vout=170V/3A
VCout_top	39.5V	38.9V	38.9V	84.5V	85.8V	85V
VCout_bot	42V	42.8V	42.8V	89.6V	88.5V	89.4V

5 Summary

As discussed in previous sections, compared to TL topology, SHB topology has higher power density. Stacked half bridge topology can fully overcome the gap for using 650V GaN HEMT LMG3522R030-Q1 in 800V battery application, no matter if used in primary side as switches or in secondary side as synchronization rectifiers. The type-5 ePWM module of C2000 device can fulfill the special PWM requirement for SHB topology. The test results show that SHB also has high efficiency, load transient performance in 800V scenario as similar as original topology in PMP41078 in a 400V scenario, which can drive people to enlarge this from isolated to a non-isolated application.

6 References

- Texas Instruments, *PMP41139 3.5kW, 800V to 14V DC/DC Converter Reference Design*, design guide.
- Texas Instruments, *PMP41078 High-Voltage to Low-Voltage DC-DC Converter Reference Design With GaN HEMT*, test report.
- Texas Instruments, *PMP23461 Test Report*, test report.
- Texas Instruments, *LM3522R030-Q1 650 V 30 mΩ GaN FET with Integrated Driver, Protection and Temperature Reporting*, data sheet.

7 Acronyms

TL	Three Level
SHB	Stacked Half Bridge
DC	Direct Current
OBC	On Board Charge
HSHB	Hard Switch Half Bridge
SPSDAB	Single Phase Shift Dual Active Bridge
MVBI	Middle Voltage Balance Issue
PWM	Pulse Width Modulate

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