Application Brief

Full Assist in LMX2624

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Introduction

Frequency hopping between multiple frequencies occurs in applications in multiple systems such as down converter and up converter chains where switching time expected is very low. Figure 1 shows the typical receiver architecture that requires one or more local oscillators (LOs) to generate the different frequency signals and mix them with an incoming reception signal.

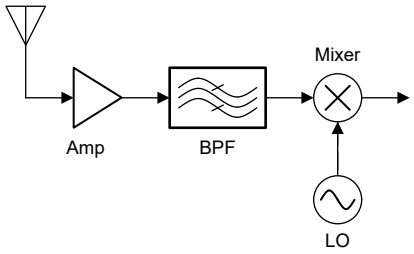

Figure 1. RX Chain

Challenges in Frequency Hopping

- RF synthesizers based on integrated VCOs have multiple frequency bands, which depends on the cap bank length.
- Number of frequency bands depend on the wideband frequency coverage of the VCOs including the number of VCOs.
- When frequency is hopped from F1 to F2, the challenge is to select the frequency band corresponding to F2 in less time with no degradation in phase noise from VCOs.
- Once the frequency band is selected, smooth settling based on the PLL bandwidth takes place. The total time the settling takes when moving from F1 to F2 is the lock time.
- Majority of the time taken during the frequency hopping is the VCO calibration which helps select the frequency band with no degradation in phase noise.
- Depending on the architecture, some RF synthesizers for K-band frequency generation uses open loop multipliers, which must be calibrated.

Components of Lock Time

When the frequency is hopped from F1 to F2, the time this takes to hop is defined as lock time, which contains the following sequence of events:

- Register Write Time :
  - SPI register writes involve settings that need to be changed like N.F(Integer + Fraction) etc. to get the PLL lock to the required frequency.
- VCO/Multiplier calibration time :
  - For the frequency required, particular VCO band and amplitude setting must be selected. Depending on the type of calibration method used, the VCO calibration time changes. For a multiplier architecture based on tuned filters, band where highest gain is possible for that particular frequency must be selected and amplitude settings must be selected for the best phase noise.
- Analog Settling time :

– After the VCO band and amplitude is selected, there is some frequency delta compared to the expected frequency. PLL adjusts the varactor vtune to the required voltage to match the vtune to the expected frequency. The PLL has certain bandwidth and varactor settling depending on the PLL bandwidth.

Design in LMX2624

- FULL ASSIST feature for both VCO and Multiplier eliminates completely the VCO and Multiplier calibration time.
- Instead of calibrating the VCO and Multiplier every time, if calibration codes are noted once for particular frequency, forcing them at once can result in faster frequency switching .
- Lock time now consists of register write time and analog loop settling.
- SPI can go as high as 40MHz

Full Assist Feature in LMX2624

- For frequency switching from F1 to F2, PLL feedback divider, VCO/Multiplier calibration code must be written through SPI. So, there is register write wait time involved here depending on the SPI speed and number of registers written. During this register write time, output frequency can be unstable which is not desired.
- To avoid this, the required registers to switch to F2 are internally stored in shadow registers (doubler buffered) and only applied when one special register (SR) is written.
- This helps frequency switching very fast as all calibration codes are going to respective blocks in single shot post toggling that special register. Figure 2 shows what the output frequency looks like with and without full assist feature.
- Analog PLL lock time is PLL bandwidth dependent.

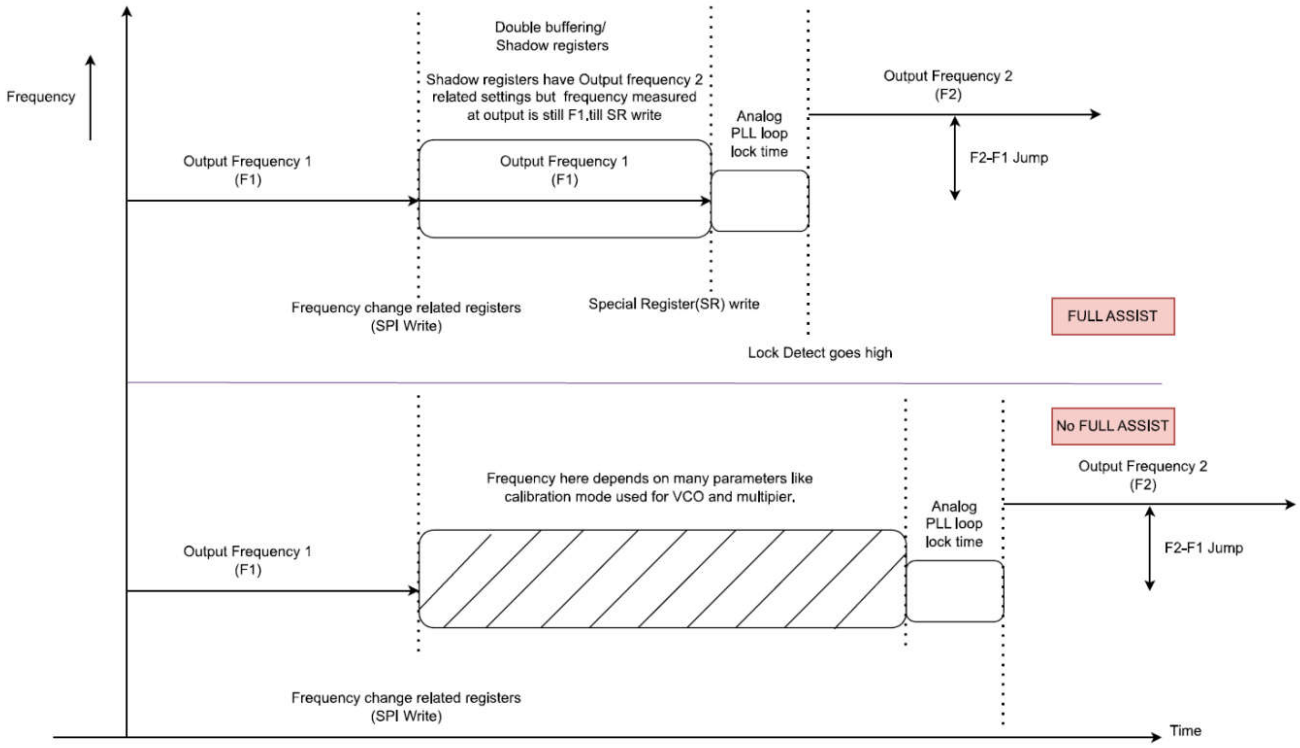

Figure 2. Full Assist Frequency Transient with Time

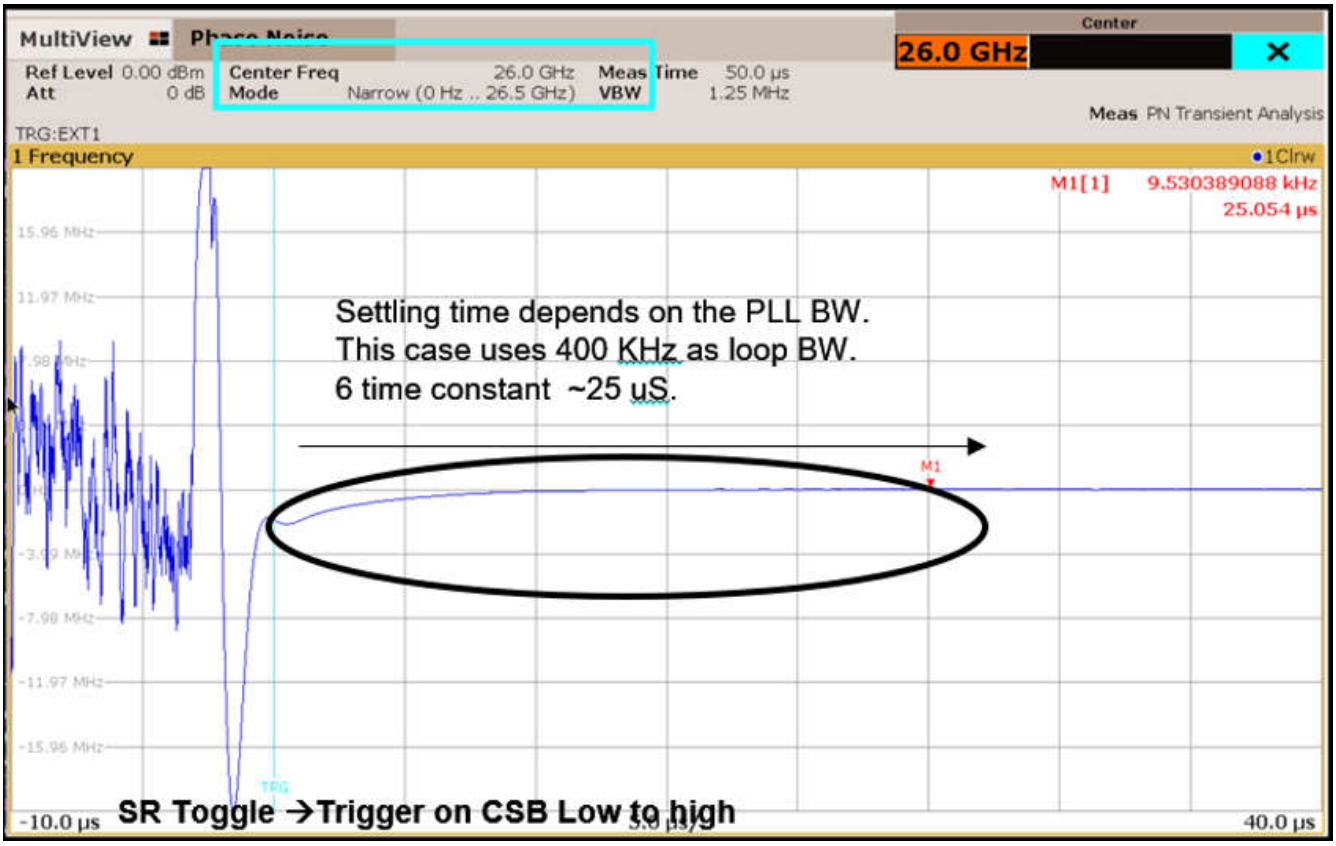

Figure 3. FSWP Frequency Settling Time in Full Assist

Figure 3 shows the silicon phase noise plot for the settling behavior at 26GHz, triggered on special register, where frequency jump is from 16GHz to 26GHz. FSWP cannot capture wide frequency jumps like 16GHz to 26GHz. So, the narrow band option is selected where span is limited to 40MHz around 26GHz as the center frequency in frequency transient capture.

Sequence of Steps

- Verify DBL_BUF_EN = 1(R16<8>). Double buffering is enabled for the registers related to VCO, doubler, PLL, Output MUX and channel divider. Register map section shows more details about registers.
- Once the calibration has been done,VCO and DBLR related registers value must be readback for frequency F1 and frequency F2 as shown in following tics-pro page(V1.7.7.7). Make sure that MUXOUT(R22<6:0>) is 1 and Readback(R1<13> is 1) when doing register readback. Tics Pro Snapshot shows the snapshot of the VCO calibrated codes readback. In this case, the doubler is not engaged, so the doubler is in power down.
- Figure 5 shows the doubler readback data, which is used during the frequency switching.

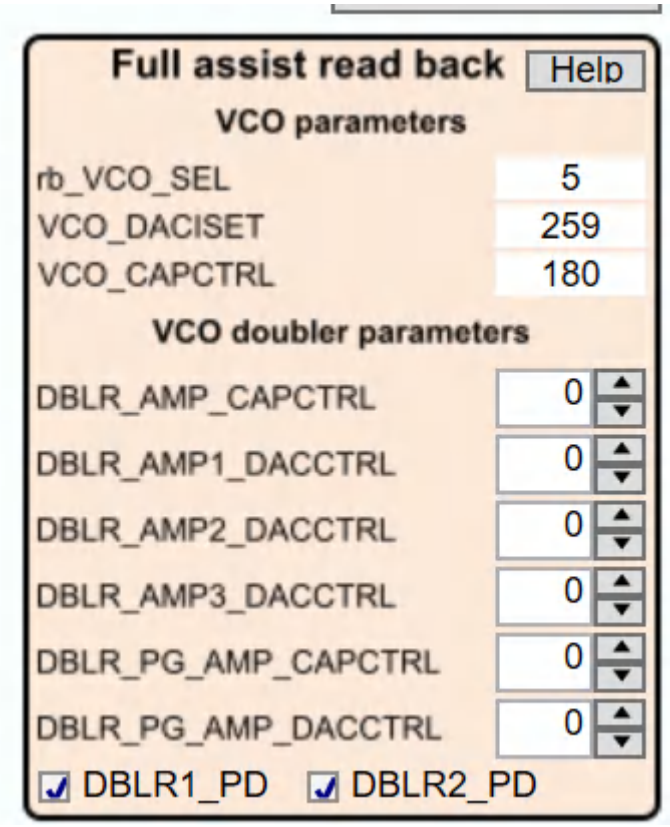

Figure 4. Tics Pro Snapshot

- VCO_FULL_ASSIST(R5<12>)=1
- Write into full_assist registers.
  - VCO: VCO_SEL, VCO_CAPCTRL, VCODACISET
  - Doubler : DBLR1_PD, DBLR_AMP_CAPCTRL, DBLR_AMP1_DACCTRL, DBLR_AMP2_DACCTRL, DBLR_AMP3_DACCTRL, DBLR_PG_AMP_CAPCTRL, DBLR_PG_AMP_DACCTRL

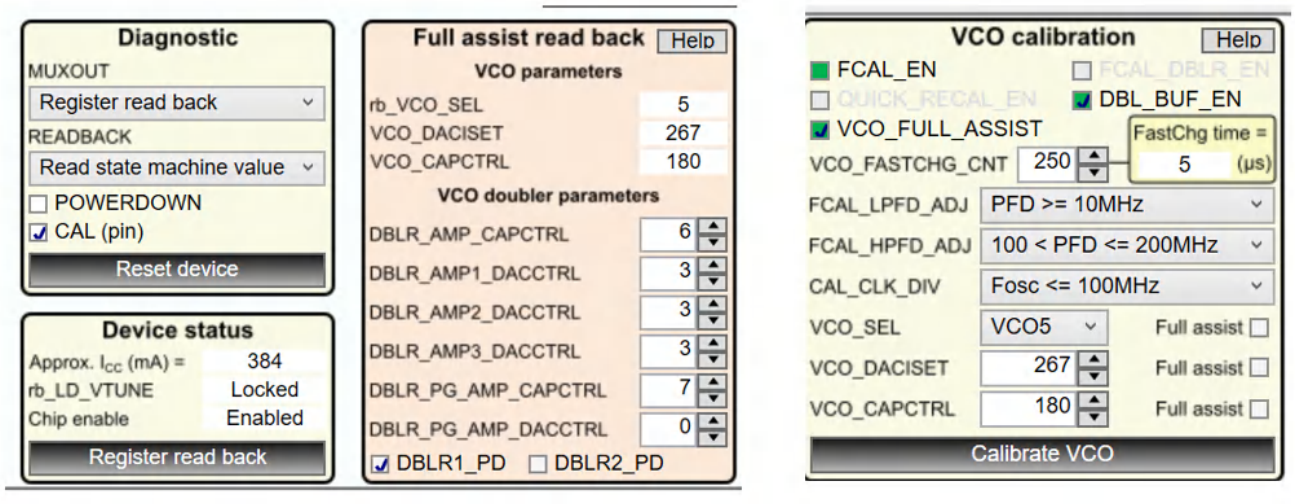

Figure 5. Tics Pro Snapshot Showing More Registers

- Change PLL related registers to change the output frequency to required Freq F1 or F2. (PLL_N(R9<2:0>/R8), PLL_NUM(R15/R14), PLL_DEN(R10/R11), MASH_ORDER(R5<15:13>), PFD_DLY(R3<10:5>).
- Output MUX select can also be changed to engage channel divider on channel B (OUTA_MUX(R3<13:12>), OUTB_MUX(R3<15:14>), CHDIV(R3<4:0>))

- Write into Register 0 with FCAL_EN=0(R0<2>), DBLR_FCAL_EN=0(R0<12>), DBLR_ACAL_EN=0(R0<13>). This acts as trigger for double buffering.

Another factor to consider which can potentially degrade the lock time is the capacitor on the VbiasVCO pin. For faster settling, the recommended capacitor is as low as 1uF. VCO_FASTCHG_CNT register(R7<14:7>) helps charge this VbiasVCO pin faster. If the capacitor in VbiasVCO pin is lower, there is slight degradation in the phase noise numbers.

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