Application Note

PLC Analog Output Module Architectures

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ABSTRACT

Analog Output (AOUT) Modules are essential PLC modules to drive analog actuators. The analog output has the highest cost per channel among all IO modules and possibly the most challenging to protect. There are multiple topologies to implement analog output modules to achieve required performance at a designed for cost. Understanding these topologies and why designer can choose them is key factor in selecting the right parts for your AOUT project.

This overview includes the AOUT module key parameters, understanding how the AOUT affect the topology selection, and what different topologies are available to choose from.

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Trademarks

1 Introduction

Analog Output (AOUT) Modules are essential PLC modules to drive analog actuators. The analog output has the highest cost per channel among all IO modules and possibly the most challenging to protect. There are multiple topologies to implement analog output modules to achieve required performance at a designed for cost. Understanding these topologies and why designer can choose a module is a key factor in selecting the correct parts for your AOUT project.

2 Analog Output Module Specification

Like analog input modules, the output modules features large number of performance specifications, which results in diversity in module types. This diversity is not possible to cover by a single architecture.

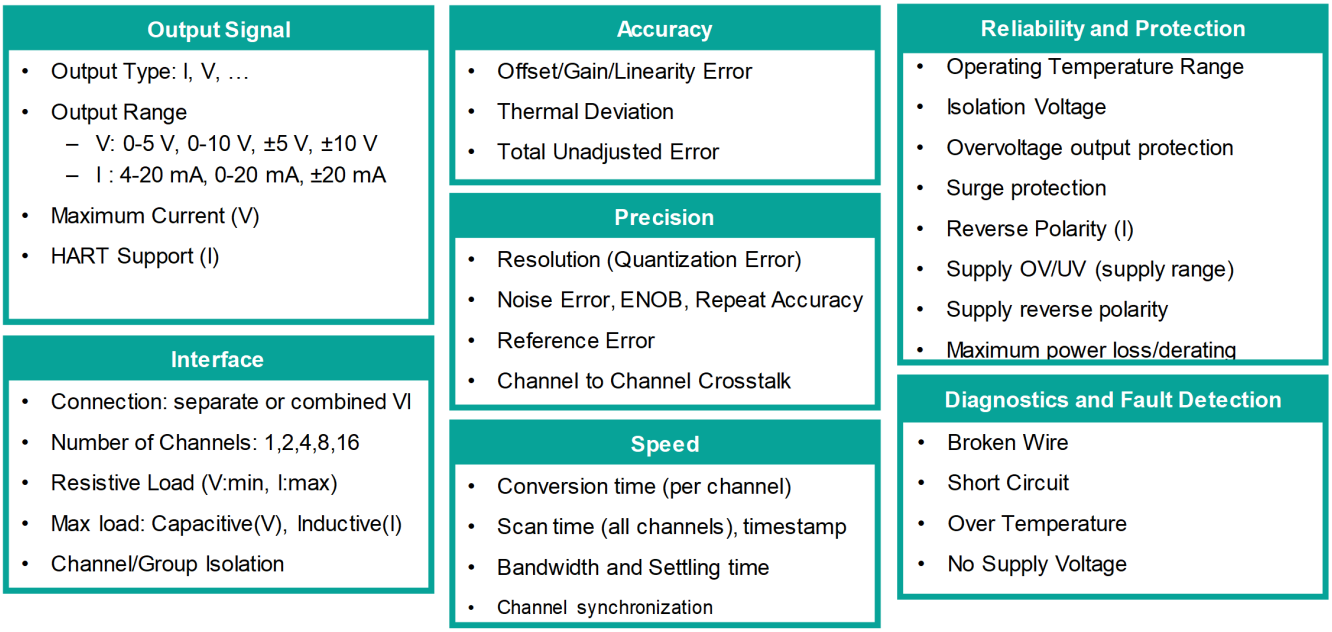


Figure 2-1. AOUT Module Specifications

As Figure 2-1 shows, the specifications can be clustered into groups covering output signal and interface, accuracy, precision, speed, reliability, and diagnostics. Although the specifications are numerous, few important parameters are determining the designed for architecture to chose. among the most important specs of AOUT module are:

- Output type (voltage or current) and the range (±10V or 4-20mA are common) as well as load range
- Number of channels, and channel isolation
- Conversion time and output noise.

3 Analog Output Module Structure

The Figure 3-1 application page on TI.com provides a rich source of information about TI designs for PLC analog output. The page supports the generic structure of the AOUT module as shown in the following figure.

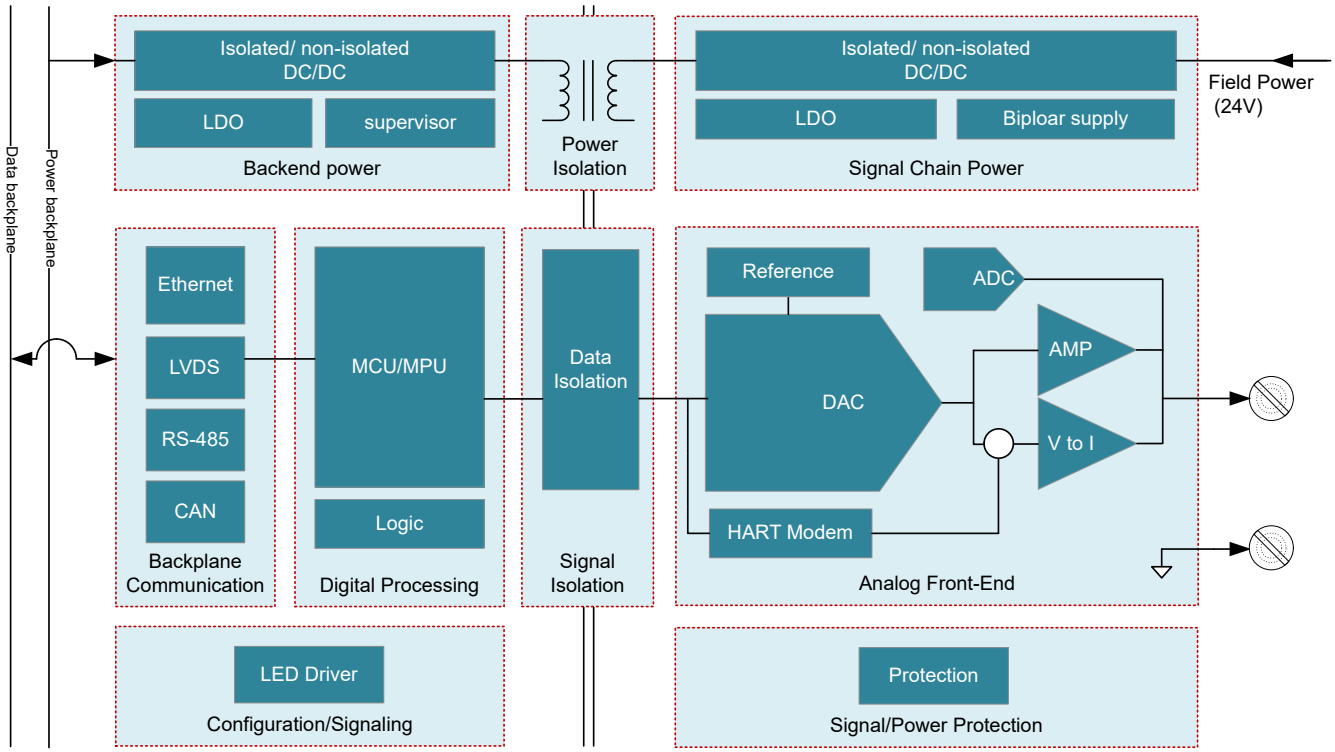


Figure 3-1. Analog Output Module Structure

The core of the AOUT module front-end is a digital-to-analog DAC converter, which drives output buffers either voltage or current. DAC requires a voltage reference, and HART modem is optional for current outputs. Power for AOUT front-end either comes from the field side, or less common from the backplane over isolated stage. This is a functional diagram, the different functions can either be integrated into one device or spread over multiple devices.

This article focuses on the front-end architectures, and what can be the correct architecture to use based on different requirements.

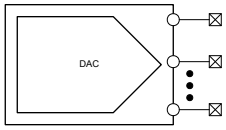
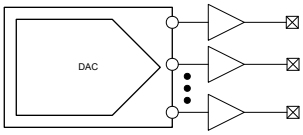
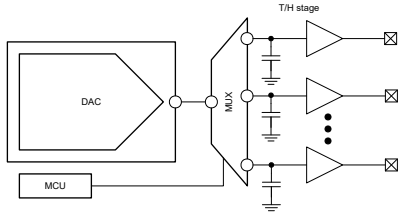
4 Multi-Channel Output Architectures

In principle, there are three common architectures for Multi-channel AOUT modules.

1. Fully integrated DAC: this approach offers the smallest area and possibly the highest performance for the highest cost per channel as this approach requires high voltage DAC.
2. Low-voltage DAC plus an output buffer: this approach provides scalability regarding number of channels, and flexibility in choosing the DAC and the buffer features at lower cost than the integrated design.
3. Track and hold multiplexed single channel DAC: this approach offers the lowest cost per channel in the expense of more complex design as channel sequencing needs an MCU. This implementation generally has longer settling time, and higher noise than the other implementations.

Choosing the designed for architecture is a function of the performance, cost, and speed targets

Table 4-1. Multi-Channel AOUT Architectures

	Fully integrated DAC	**Voltage DAC+ buffer stage**	**Multiplexed Track&Hold**
Block diagram			
Features	High integration, accuracy, smaller area but Higher cost per channel	Scalable in performance and number of channels and low cost per channel but larger area	Lowest cost per channel, but requires MCU and complex design and slower settling
Devices	**DAC8775, DAC8140x**	**DAC8050x, XTR111, XTR305, TLV9302, OPA2990S**	**DAC80501+TMUX1108/4, DAC8760+TMUX6208**

4.1 Fully Integrated DAC Architecture

The DAC8755 provides one chip design for 4-channel,16b, bipolar voltage and current with 10us settling time, with highly integrated output front-end including the DAC, the reference, the buffers, as well as the buck-boost stages to implement adaptive power for current output from a wide Vin single supply of 12-65V. *Less Than 1-W, Quad-Channel, Analog Output Module With Adaptive Power Management* is a reference design showing the powerful features of this device, while *Quad-Channel Industrial Voltage and Current Output Driver (EMC/EMI Tested)* is going into the details of passing the EMC/EMI tests for the design.

Figure 4-1 shows how this integrated DAC simplifies board design (only one channel is shown), still providing flexibility of software output configuration, and adaptive power management.

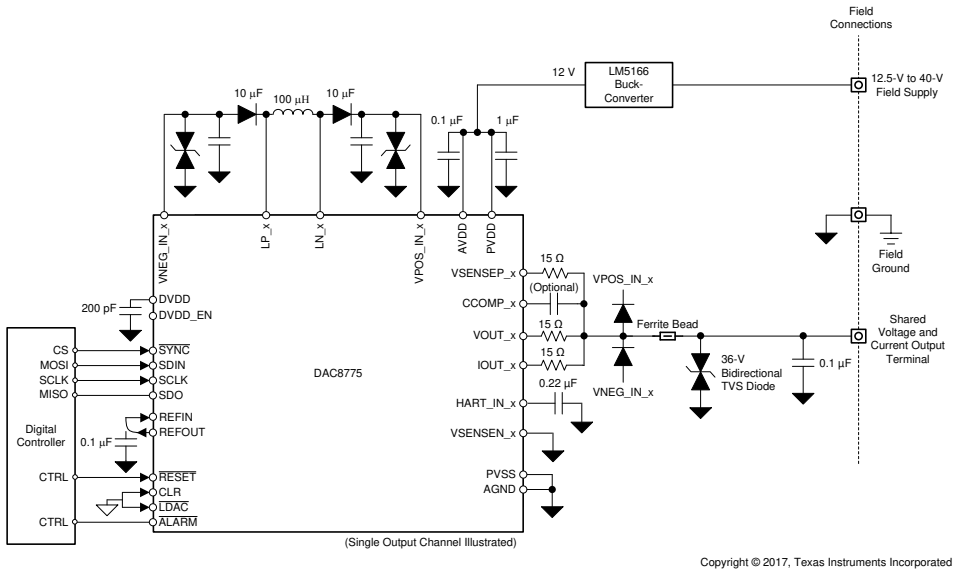


Figure 4-1. Schematic of DAC8775 AOUT Circuit

When only voltage output is required, DAC81404 offers wide range of resolution and channel count to choose from. With integrated reference and 12us settling time, DAC81404 is able to cover the highest voltage AOUT demands. The DAC814xx family is capable of high voltage output up to ±20V or unipolar 40V needed for special applications. The 4-channel device DAC81404 provides voltage sense pins which helps maintaining output accuracy when protection devices are placed in series.

Table 4-2. DAC81408 Device Family

Channels	12 bit	14 bit	16 bit
2	DAC61402		
4			DAC81404
8	DAC61408	DAC71408	DAC81408
16	DAC61416	DAC71416	DAC81416

4.2 Low Voltage DAC Plus an Output Buffer

This is popular architecture as low voltage DAC are readily available. Even the non-buffered DAC can be used making more parts available to select from. DAC80504 is an excellent DAC for such application. DAC80504 is a family of unipolar 5V buffered voltage output DAC with integrated REF (2ppm/°C), only 5us settling time, programmable output range, and INL=1 LSB in small package. The DAC does not have sense pin, but with output buffers this is not necessary, as the output compensation is done by the buffer feedback loop.

The large family of devices makes sure the designer can find the resolution and the number of channels required. The output buffer options are discussed in detail in a later section.

Table 4-3. DAC80508 Device Family

Channels	12 bit	14 bit	16 bit
1	DAC60501	DAC70501	DAC80501
2	DAC60502	DAC70502	DAC80502
4	DAC60504	DAC70504	DAC80504
8	DAC60508	DAC70508	DAC80508

The DAC plus buffer architecture is a must if higher output current drive is needed, as most integrated DACs have limited current drive. Also if very fast settling is required as a designer can combine fast low voltage DACs and wide bandwidth buffers, but hardly can find any integrated high voltage DAC with faster than 10us settling time.

4.3 Track and Hold Multiplexed Output

In this architecture, a single-channel voltage DAC is connected to a de-multiplexer with hold capacitor on each output channel. The MUX switch in addition to the hold capacitor acts as track and hold circuit. If the DAC output is sequentially changed in synchronicity with the multiplexer, separate static or dynamic outputs can be generated from a single channel DAC output.

This is a cost effective implementation, but requires careful design as the settling time of the DAC output, as well as the MUX leakage puts the minimum and maximum limits of the MUX hold time and scanning frequency. These tradeoff are well explained in *Multi-Channel Analog Output Module With Multiplexed Single-Channel DAC for PLCs* reference design.

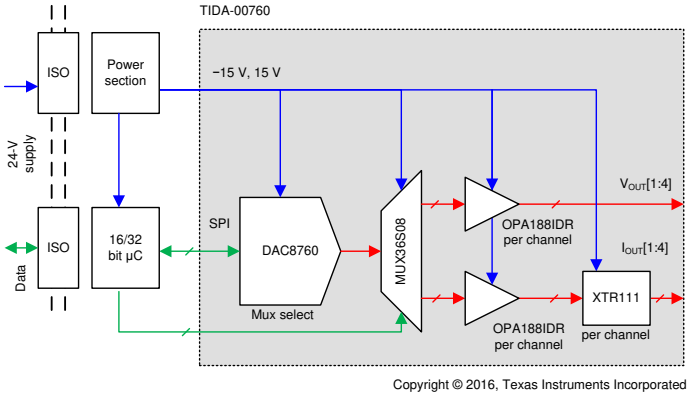


Figure 4-2. Block diagram for track and hold multiplexed output architecture

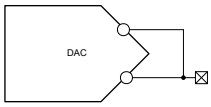
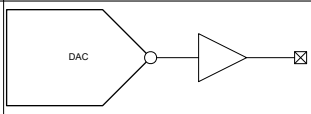
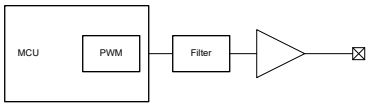
Both low voltage DACs like DAC80501 (16b) ,DAC70501 (14b), DAC60501 (12b) or high voltage DACs like DAC8760 (16b) or DAC7760 (12b) can be used in this architecture. When low voltage DACs is used, the necessary gain is fulfilled by the output buffer. This architecture uses voltage and current buffers like the previous architecture, which are described in a later section.

5 Single-Channel Output Architectures

When only a single-channel output is required, as in the case of channel-to-channel isolated modules, there are three options similar to the multi-channel case, although not exactly, and also different devices of choice.

1. Fully integrated DAC: this approach offers the smallest area and possibly the highest performance for the highest cost per channel as this approach requires high voltage DAC.
2. Low-voltage DAC plus an output buffer: this approach provides scalability and flexibility in choosing the DAC and the buffer features at lower cost than the integrated design.
3. Pulse-width modulation (PWM DAC) plus a buffer: this approach offers the lowest cost per channel but has longer settling time, and higher noise than the other implementations.

Table 5-1. Single-Channel AOUT Architectures

	Fully Integrated DAC	Voltage DAC+ Buffer Stage	PWM DAC + Buffer
Block diagram			
Features	High integration, accuracy, smaller area but Higher cost per channel	Lower cost, and can achieve higher drive and faster settling.	Lowest cost per channel, but slower settling and higher noise
Devices	**DAC8760, DAC7760, DAC8750**	**AFE882H1/201, DAC80501, DAC70501, DAC60501**	**MSPM0L, MSPM0G**

5.1 Fully Integrated DAC

As mentioned previously, the fully-integrated DAC provides compact, accurate design with slightly higher cost. Single channel high voltage DACs like **DAC8760** is capable of bipolar voltage (+/-10V) and unipolar current output (0-20mA) with TUE=0.1%FSR and DNL=1 LSB. The DAC accepts power supply up to +/-20V. The **DAC7760** is the 12-b version for less demanding applications.

The application note, *Combined Voltage and Current Output with the DACx760* shows how to use DAC8760 for combined voltage and current output as done in the reference design, *Combined Voltage and Current Output Terminal for Analog Outputs (AO) in Industrial Applications*. The reference design, *Single-Channel Industrial Voltage and Current Output Driver, Isolated, EMC/EMI Tested* shows separate V/I outputs instead.

If single-channel current-only output is needed, then **DAC8750** (16b) or **DAC7750** (12b) is the device of choice.

5.2 Low-Voltage DAC Plus an Output Buffer

A single-channel DAC, **AFE882H1** family offers feature-rich, integrated reference, and HART modem option both in 14b and 16b versions. The AFE882H1 is especially important for safety-related applications. With TUE=0.08 %FSR this family offers the highest accuracy for such implementation.

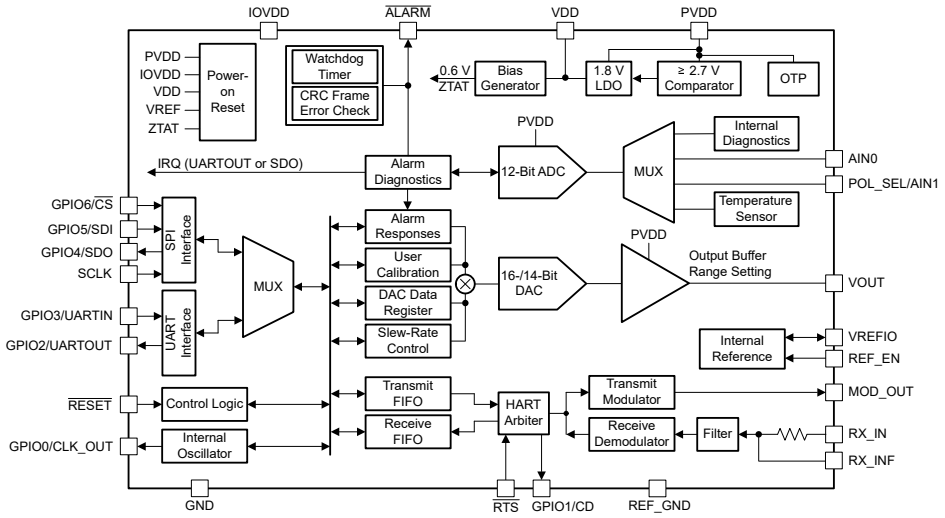


Figure 5-1. AFE882H1 Device Block Diagram

Table 5-2. AFE882H1 Device Family

	14 bits	16 bits
With HART	AFE782H1	AFE882H1
No HART	AFE78201	AFE88201

The **DAC80501** family, including the 12b,14b, and 16b variants of single channel ADC offers high linearity (INL=1LSB), fast settling (5us), and excellent reference drift (2ppm/°C) in a very small package, making DAC80501 an device of choice for such architecture when no safety or HART support is needed.

5.3 Pulse-Width Modulation Plus a Buffer

Pulse-Width Modulation (PWM DAC) is a special architecture used when the stand-alone DAC is to be avoided, and MCU is available in the system. The PWM can be converted to an analog voltage signal using a low-pass filter. Advanced techniques can be used to reach 16b of resolution, and relatively fast output settling time as described in *Designing high-performance PWM DACs for field transmitters*, and *High-Performance 16-bit PWM to 4- to 20-mA DAC for Field Transmitters*.

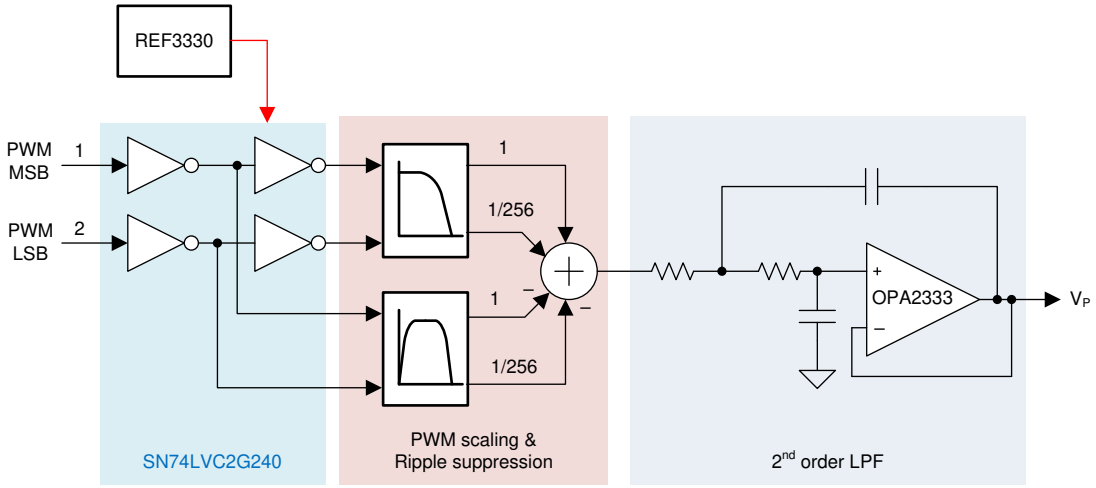


Figure 5-2. 2-Path PWM-Based DAC Block Diagram

6 Output Buffers

In this section, output buffer catalog is presented to cover various types of output signal needs. Output buffers are typically used with low-voltage single-supply DAC that is either 5V or 2.5V output or even lower like 1.25V output.

6.1 Unidirectional Current Buffer

When a source current buffer is required, a unidirectional current buffer is used. A dual-op amp is a straightforward choice which allows a low-cost low noise implementation. For this implementation op amp U1 needs to allow input to the negative rail, while U1 allows input to the positive rail, the op amps are powered by vsup, which is typically 24V, so high voltage low-offset op amps are required. **TLV9302**, and **OPA2990** are a couple of good options for this circuit. In addition a 3 precision resistors are needed. More design details about this circuit can be found in *Programmable, Two-Stage, High-Side Current Source Circuit*.

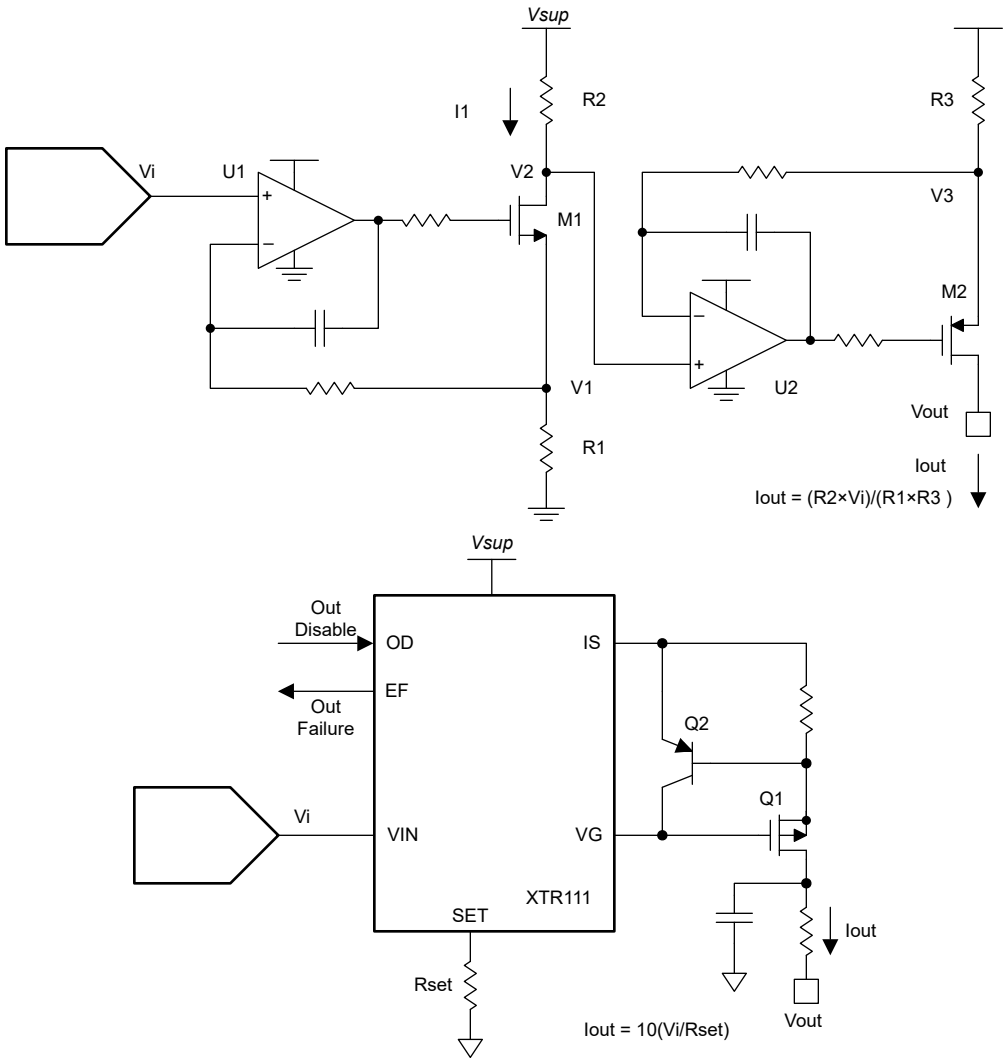


Figure 6-1. Unidirectional Current Buffer

The other implementation is using **XTR111**, which offers more integration, output disable option, and output failure diagnostic feedback signal. XTR111 requires only one single precision resistor and has maximum offset in the 1mV range, and works up to 40V supply.

6.2 Bidirectional Current Buffer

Bidirectional current output is less common for AOUT modules. When a bidirectional current output is required, a modified Howland circuit is used.

An integrated difference amplifier implementation like **INA592** provides resistor matching for high output accuracy, and requires only one external precision resistor. The amplifier has extremely low offset in the uV range, and has relatively high bandwidth of 2MHz. Check *High-side current sources for industrial applications* for more details.

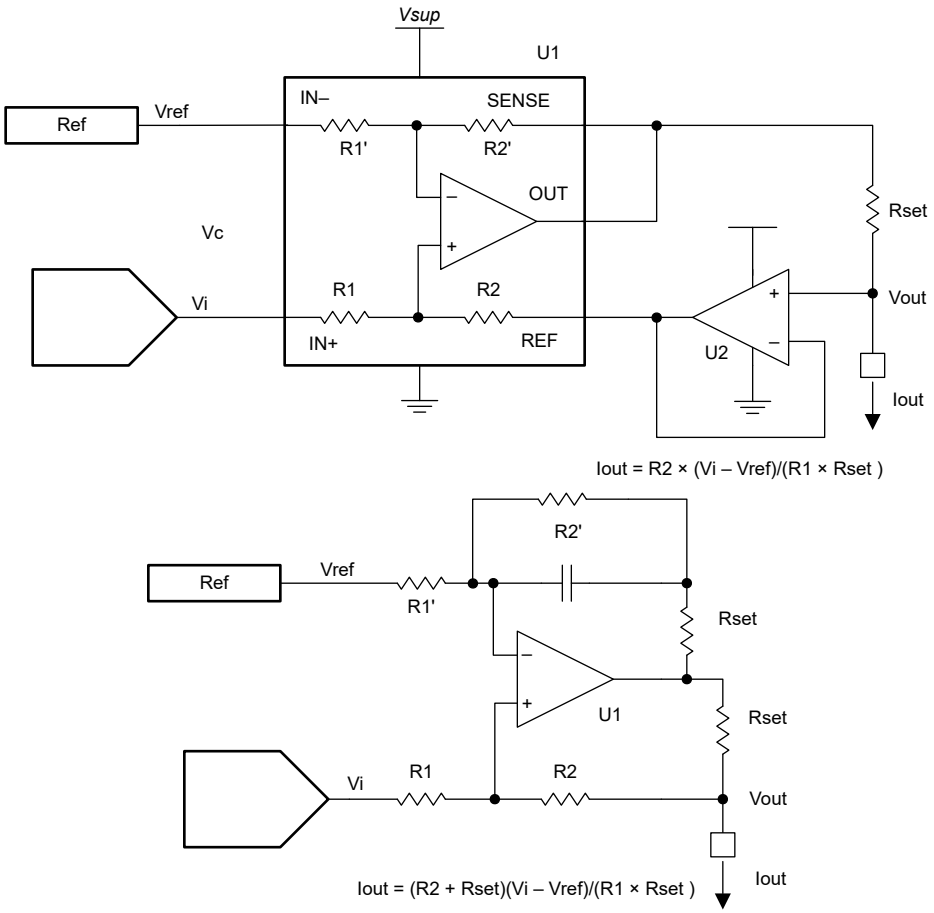


Figure 6-2. Bidirectional Current Buffer

The difference amplifier can also be built discrete using op amps like **OPA196**, this however needs precisely matched resistors to achieve a reasonable accuracy.

In both implementations, in addition to the voltage input, a reference input in the middle of the input range is needed to generate the bidirectional current. More details about this design can be found in *Analysis of Improved Howland Current Pump Configurations*.

6.3 Voltage Buffer

Voltage buffer is simpler and straightforward and provides the required gain for low-voltage DAC signal to reach ±10V. According to the available supply and the maximum output voltage, rail-to-rail output op amp is not be needed. Low offset voltage is important for achieving high accuracy. Precision matched resistors with low drift are required for precise gain.

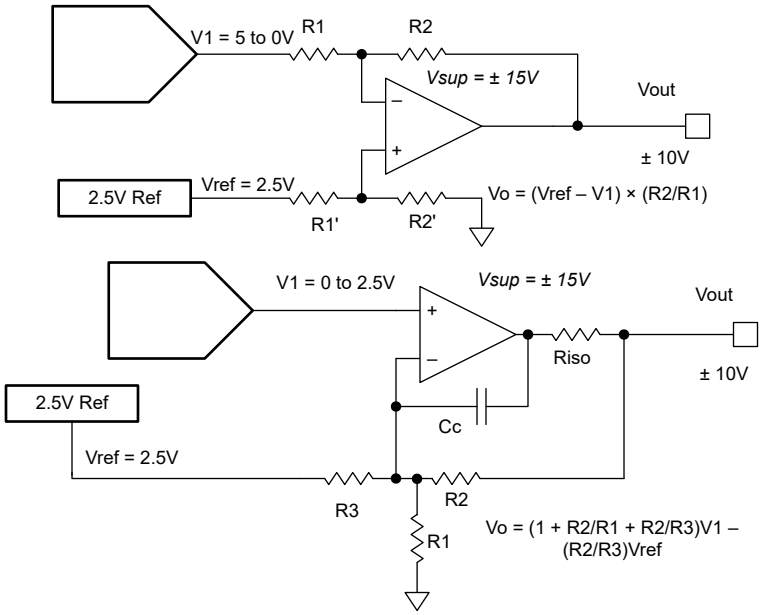


Figure 6-3. Voltage Buffer

Inverting difference amplifier can be used as in Figure 6-3, which enables the use of matched resistors readily available. The inverting amplifier input impedance is finite, designer need to make sure the DAC can drive the selected resistors.

The second implementation shown in Figure 6-3 is the non-inverting summing amplifier. The amplifier has high input impedance, but requires precision resistors, and possibly needs calibration. The amplifier allows also for the use of lower than 5V DAC.

6.4 Combined Voltage or Current Buffer

For ultimate flexibility of the output channel, a combined voltage and current buffer can be used. The first implementation shown in Figure 6-4 is discrete implementation using a pair of dual op amps with disable function like **OPA2990S**. Figure 6-4 shows how **TPS26614** loop protector can be used to protect the circuit from overcurrent or overvoltage. This circuit has bidirectional voltage output and unidirectional (sourcing) current. For more information about this circuit and the design process check *Protected, Low-Noise, Combined V-I Output Stage as Analog Output Building Block.*

The second implementation in Figure 6-4 is using the integrated **XTR305** device which provides higher accuracy, requires less precision resistors, and has some output error signal feedback. The device requires headroom and footroom of 3V for operation. Please refer to *Compact Programmable 4-mA to 20-mA and ±10-V Analog Output Reference Design for AC/Servo Drives D* for more details about designing with XTR305.

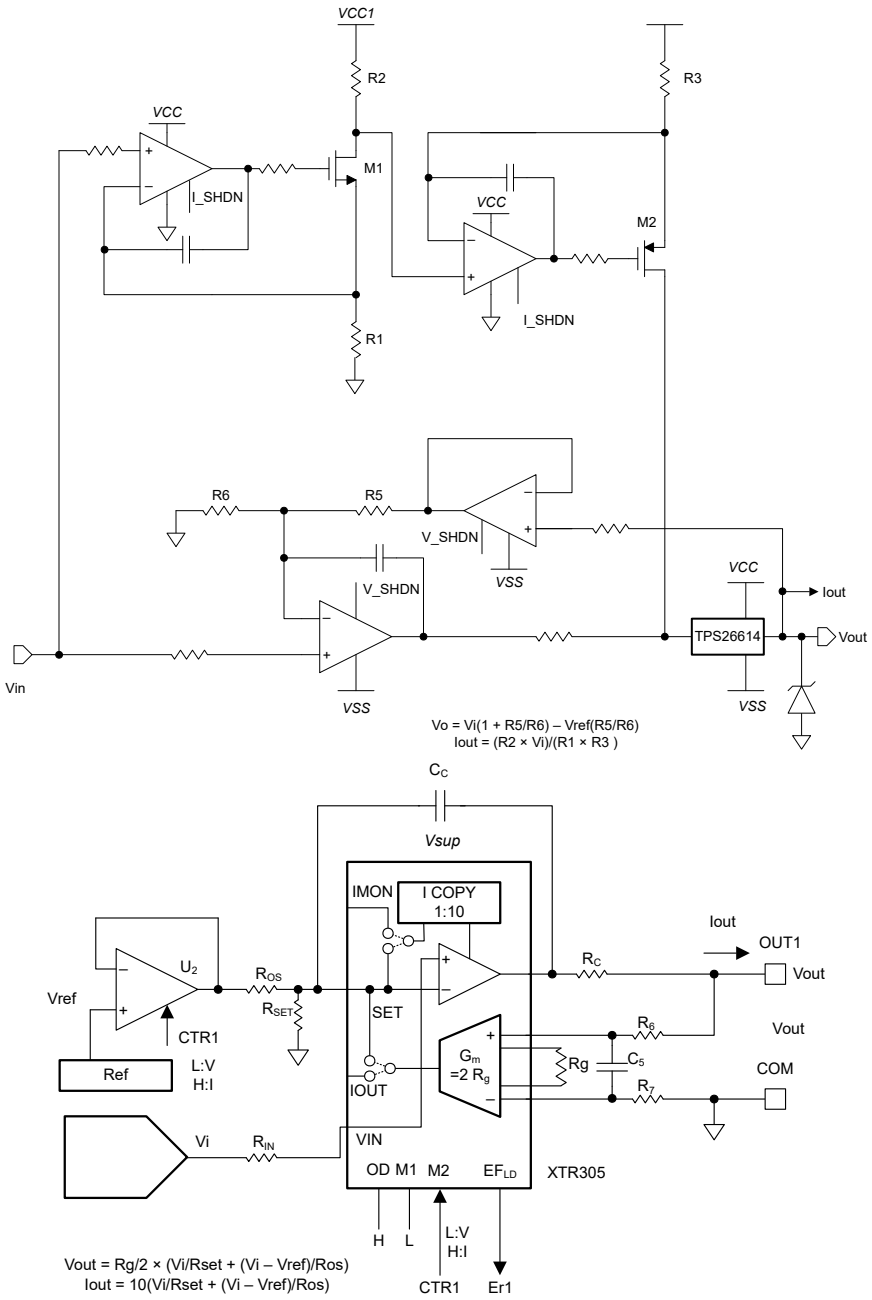


Figure 6-4. Combined V/I Buffer

7 Summary

Understanding the design goals is crucial in selecting the correct architecture for PLC AOUT module. Generally higher integration provides higher accuracy and comes at higher cost, while less integrated architecture provides less cost and more flexibility in device selection. Starting from specifying the targeted number of channels, the resolution, and the conversion time (or speed) the designer can come quickly to the right DAC. Then by specifying the output type, range, and drive strength, the output buffer is selected. When the application demands higher precision or safety features, integrated designs have advantage. When application has special requirements, like high output voltage, high current drive, or high slew rate, the non-integrated design is typically necessary.

8 References

- Texas Instruments, *Quad-Channel Industrial Voltage and Current Output Driver Reference Design (EMC/EMI Tested)*, design guide.
- Texas Instruments, *Less Than 1-W, Quad-Channel, Analog Output Module With Adaptive Power Management Reference Design*, design guide.
- Texas Instruments, *Multi-Channel Analog Output Module With Multiplexed Single-Channel DAC for PLCs Reference Design* design guide.
- Texas Instruments, *Combined Voltage and Current Output with the DACx760*, application note.
- Texas Instruments, *Combined Voltage and Current Output Terminal for Analog Outputs (AO) in Industrial Applications*, design guide.
- Texas Instruments, *Single-Channel Industrial Voltage and Current Output Driver, Isolated, EMC/EMI Tested*, design guide.
- Texas Instruments, *Designing high-performance PWM DACs for field transmitters*, technical article.
- Texas Instruments, *Programmable, Two-Stage, High-Side Current Source Circuit*, analog engineer's circuit.
- Texas Instruments, *High-side current sources for industrial applications*, analog design journal.
- Texas Instruments, *Analysis of Improved Howland Current Pump Configurations*, application note.
- Texas Instruments, *Protected, Low-Noise, Combined V-I Output Stage as Analog Output Building Block.*, application note.
- Texas Instruments, *Compact Programmable 4-mA to 20-mA and ±10-V Analog Output Reference Design for AC/Servo Drives D*, design guide.

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