Application Note

TAD52xx Power Consumption Matrix Across Various Usage Scenarios

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ABSTRACT

This application note details the power consumption of TAD52xx devices across various usage scenarios. Applicable devices include:

- TAD5112
- TAD5142
- TAD5212
- TAD5242

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Trademarks

1 Introduction

Power consumption on TAD52xx devices is highly dependent on the enabled features and usage scenarios. The following tables summarize the power consumption across:

- Supply voltage
- Sampling frequency
- Enabled channel count
- Decimation filter
- Bit clock to frame sync ratio
- PLL state (enabled or disabled)
- Output loads
- Converted word length

The following tables report the average idle-channel current consumed on the analog supply (AVDD). This supply includes all the internal analog and digital circuits but excludes the current consumed by the I/O (input/output) pins due to application dependencies. I/O power is dependent upon:

- Load capacitance of the system bus interface
- Data input clock rate
- Bus interface pullups or pulldowns
- Frequency of I^2C commands sent by the host

2 Target Mode Power Consumption With PLL Disabled

This section describes the typical current consumption of the TAD52xx devices, when the PLL is disabled with AVDD set to 1.8V and 3.3V.

The PLL is disabled by:

1. Setting the corresponding B0_P0_R52[7] (PLL_DIS) and (DAC_LOW_PWR_FILT) bit fields.
2. Enabling the B0_P0_R79[2] field.

By default, the bit clock is used as the clock source to the internal block when the PLL is disabled. Alternatively, an external clock source (CCLK) can be used in the device through one of the GPI capable pins (GPIOx or GPIx), if the system has a low jitter clock available.

- If GPIOx is used for the CCLK input, the appropriate GPIOx_CFG bit field in the GPIOx_CFG0 register must be configured for GPI function.
- If GPIx is used for the CCLK input, the appropriate GPIx_CFG bit field in the GPI_CFG register must be enabled for GPI function.
- The pin configured for GPI must be configured as CCLK, this configuration is done by configuring B0_P0_R15[6:5] (CCLK_SEL), based on the pin configured.
- With the CCLK configured, the external CCLK must be used as the clock source, this configuration is done by configuring B0_P0_R52[3:1] (CLK_SRC_SEL).
- The CCLK must be synchronized with the frame syn. For example, the CCLK frequency must be an integer multiple of the frame sync frequency.
- Once configured, the device runs on the external CCLK as the clock source.

In Table 2-1, the power consumption measurements have the biquad filters disabled, and the idle DAC output (or outputs) and an external CCLK of 12.288MHz are provided as the clock source to the device through the GPIO1 pin.

Table 2-1. Target Mode Power Consumption With PLL Disabled

Sampling Frequency (kHz)	Enabled Channels	Output Configuration	Output Drive	BCLK-FS Ratio	Word Length	Low Power Filter	Decimation Filter	AVDD = 1.8V			AVDD = 3.3V		
								AVDD Current (mA)	Dynamic Range (dB-A weighted)	THD+N (dB)	AVDD Current (mA)	Dynamic Range (dB-A weighted)	THD+N (dB)
24	1	Fully Differential	Headphone	24	24	Enabled	Linear Phase	7.12	106.17	-98.30	8.37	106.67	-99.61
24	1	Fully Differential	Line Out	24	24	Enabled	Linear Phase	6.53	106.04	-95.29	7.68	106.54	-100.87
24	1	Single Ended	Headphone	24	24	Enabled	Linear Phase	6.15	102.42	-90.68	7.24	105.14	-89.51
24	1	Single Ended	Line Out	24	24	Enabled	Linear Phase	5.85	102.37	-91.43	6.95	105.09	-93.76
24	2	Fully Differential	Headphone	48	24	Enabled	Linear Phase	12.09	112.33	-90.52	14.37	114.25	-99.51
24	2	Fully Differential	Line Out	48	24	Enabled	Linear Phase	10.93	112.72	-95.30	12.98	120.07	-101.10
24	2	Single Ended	Headphone	48	24	Enabled	Linear Phase	10.11	104.04	-89.68	12.11	109.06	-88.89
24	2	Single Ended	Line Out	48	24	Enabled	Linear Phase	9.51	104.06	-90.90	11.44	109.34	-94.30
32	1	Fully Differential	Headphone	24	24	Enabled	Linear Phase	7.10	112.47	-91.68	8.33	114.68	-101.53
32	1	Fully Differential	Line Out	24	24	Enabled	Linear Phase	6.53	112.91	-96.07	7.67	115.30	-103.55
32	1	Single Ended	Headphone	24	24	Enabled	Linear Phase	6.13	104.30	-89.31	7.27	109.76	-92.50
32	1	Single Ended	Line Out	24	24	Enabled	Linear Phase	5.83	104.30	-91.44	6.95	109.74	-96.82

Table 2-1. Target Mode Power Consumption With PLL Disabled (continued)

Sampling Frequency (kHz)	Enabled Channels	Output Configuration	Output Drive	BCLK-FS Ratio	Word Length	Low Power Filter	Decimation Filter	AVDD = 1.8V			AVDD = 3.3V		
								AVDD Current (mA)	Dynamic Range (dB-A weighted)	THD+N (dB)	AVDD Current (mA)	Dynamic Range (dB-A weighted)	THD+N (dB)
32	2	Fully Differential	Headphone	48	24	Enabled	Linear Phase	12.18	111.08	-85.23	14.45	113.14	-99.08
32	2	Fully Differential	Line Out	48	24	Enabled	Linear Phase	11.00	111.57	-96.26	13.06	113.52	-100.93
32	2	Single Ended	Headphone	48	24	Enabled	Linear Phase	10.16	103.97	-86.67	12.18	108.82	-91.13
32	2	Single Ended	Line Out	48	24	Enabled	Linear Phase	9.57	103.85	-90.16	11.42	108.74	-95.16
48	1	Fully Differential	Headphone	24	24	Enabled	Linear Phase	7.18	111.54	-101.28	8.41	113.30	-101.45
48	1	Fully Differential	Line Out	24	24	Enabled	Linear Phase	6.57	112.04	-95.98	7.72	114.22	-103.22
48	1	Single Ended	Headphone	24	24	Enabled	Linear Phase	6.21	104.11	-91.24	7.37	109.23	-89.60
48	1	Single Ended	Line Out	24	24	Enabled	Linear Phase	5.89	104.26	-91.54	7.00	109.28	-94.15
48	2	Fully Differential	Headphone	48	24	Enabled	Linear Phase	12.15	111.32	-91.26	14.43	112.16	-99.04
48	2	Fully Differential	Line Out	48	24	Enabled	Linear Phase	10.98	111.42	-95.67	13.01	112.35	-103.12
48	2	Single Ended	Headphone	48	24	Enabled	Linear Phase	10.17	103.72	-89.69	12.15	108.28	-88.53
48	2	Single Ended	Line Out	48	24	Enabled	Linear Phase	9.53	103.79	-90.69	11.44	108.31	-93.44
96	1	Fully Differential	Headphone	24	24	Enabled	Linear Phase	7.42	109.89	-100.85	8.66	111.22	-101.43
96	1	Fully Differential	Line Out	24	24	Enabled	Linear Phase	6.82	110.09	-95.94	7.99	111.48	-102.64
96	1	Single Ended	Headphone	24	24	Enabled	Linear Phase	6.45	103.88	-91.23	7.60	108.30	-89.37
96	1	Single Ended	Line Out	24	24	Enabled	Linear Phase	6.16	103.97	-91.86	7.26	107.96	-93.85
96	2	Fully Differential	Headphone	48	24	Enabled	Linear Phase	12.48	108.42	-90.30	14.66	116.99	-101.26
96	2	Fully Differential	Line Out	48	24	Enabled	Linear Phase	11.28	108.75	-95.66	13.37	109.63	-102.47
96	2	Single Ended	Headphone	48	24	Enabled	Linear Phase	10.38	102.73	-89.53	12.41	107.29	-88.64
96	2	Single Ended	Line Out	48	24	Enabled	Linear Phase	9.86	103.23	-90.47	11.77	107.36	-93.70

3 Target Mode Power Consumption With PLL Enabled

This section describes the typical current consumption of the TAD52xx when the PLL is enabled with AVDD set to 1.8V and 3.3V.

By default, upon power-up, the PLL is configured as enabled. The bit field corresponding to this configuration is B0_P0_R52[7] (PLL_DIS) in the register map.

In Table 3-1, the current consumption measurements have the biquad filters disabled while maintaining the DAC output channel (or channels) idle.

Note

The dynamic range numbers are of a TAD5212 variant, provided for benchmarking.

Table 3-1. Target Mode Power Consumption With PLL Enabled

Sampling Frequency (kHz)	Enabled Channels	Output Configuration	Output Drive	BCLK-FS Ratio	Word Length	Decimation Filters	AVDD = 1.8V			AVDD = 3.3V		
							AVDD Current (mA)	Dynamic Range (dB-A weighted)	THD+N (dB)	AVDD Current (mA)	Dynamic Range (dB-A weighted)	THD+N (dB)
8	1	Fully Differential	Headphone	32	32	Linear Phase	9.24	114.23	-84.04	10.49	118.25	-85.16
8	1	Fully Differential	Line Out	32	32	Linear Phase	8.63	115.27	-84.19	9.78	120.32	-85.12
8	1	Single Ended	Headphone	32	32	Linear Phase	8.24	90.93	-79.69	9.42	108.84	-83.08
8	1	Single Ended	Line Out	32	32	Linear Phase	7.94	90.85	-81.28	9.09	108.89	-84.83
8	2	Fully Differential	Headphone	48	24	Linear Phase	14.53	114.16	-79.53	16.81	118.13	-85.11
8	2	Fully Differential	Line Out	48	24	Linear Phase	13.34	114.93	-83.83	15.39	120.09	-85.23
8	2	Single Ended	Headphone	48	24	Linear Phase	12.51	102.18	-78.07	14.58	109.08	-81.94
8	2	Single Ended	Line Out	48	24	Linear Phase	11.93	102.23	-82.90	13.86	109.17	-84.82
16	1	Fully Differential	Headphone	24	24	Linear Phase	10.11	114.16	-90.96	11.39	117.73	-100.36
16	1	Fully Differential	Line Out	24	24	Linear Phase	9.56	115.11	-94.84	10.7	120.06	-101.94
16	1	Single Ended	Headphone	24	24	Linear Phase	9.18	87.94	-78.51	10.32	107.13	-86.54
16	1	Single Ended	Line Out	24	24	Linear Phase	8.86	87.92	-79.68	10	107.12	-94.63
16	2	Fully Differential	Headphone	48	24	Linear Phase	15.85	113.96	-80.88	18.12	118.03	-96.32
16	2	Fully Differential	Line Out	48	24	Linear Phase	14.67	114.77	-92.69	16.76	119.89	-100.99
16	2	Single Ended	Headphone	48	24	Linear Phase	13.88	100.66	-79.12	15.88	108.39	-84.33
16	2	Single Ended	Line Out	48	24	Linear Phase	13.19	100.63	-87.52	15.21	108.3	-94.04
24	1	Fully Differential	Headphone	24	24	Linear Phase	11.64	114.2	-90.19	12.89	118.32	-103.78
24	1	Fully Differential	Line Out	24	24	Linear Phase	11.07	115.18	-95.86	12.22	120.2	-104.00
24	1	Single Ended	Headphone	24	24	Linear Phase	10.69	104.46	-84.38	11.8	110.55	-87.27
24	1	Single Ended	Line Out	24	24	Linear Phase	10.34	104.43	-90.81	11.5	110.64	-96.72
24	2	Fully Differential	Headphone	48	24	Linear Phase	17.35	114.26	-80.88	19.57	118.17	-97.40
24	2	Fully Differential	Line Out	48	24	Linear Phase	16.16	115.19	-95.33	18.22	120.24	-103.93
24	2	Single Ended	Headphone	48	24	Linear Phase	15.35	104.08	-78.79	17.33	110.19	-84.47
24	2	Single Ended	Line Out	48	24	Linear Phase	14.73	104.18	-88.69	16.63	109.91	-94.76

Table 3-1. Target Mode Power Consumption With PLL Enabled (continued)

Sampling Frequency (kHz)	Enabled Channels	Output Configuration	Output Drive	BCLK-FS Ratio	Word Length	Decimation Filters	AVDD = 1.8V			AVDD = 3.3V		
							AVDD Current (mA)	Dynamic Range (dB-A weighted)	THD+N (dB)	AVDD Current (mA)	Dynamic Range (dB-A weighted)	THD+N (dB)
32	1	Fully Differential	Headphone	24	24	Linear Phase	11.93	114.29	-91.02	13.22	117.99	-103.51
32	1	Fully Differential	Line Out	24	24	Linear Phase	11.36	115.2	-95.94	12.5	119.99	-104.01
32	1	Single Ended	Headphone	24	24	Linear Phase	10.93	104.51	-85.05	12.12	110.55	-86.73
32	1	Single Ended	Line Out	24	24	Linear Phase	10.67	104.43	-90.91	11.75	110.45	-95.79
32	2	Fully Differential	Headphone	48	24	Linear Phase	18.64	114.18	-80.96	20.95	117.94	-97.67
32	2	Fully Differential	Line Out	48	24	Linear Phase	17.47	115.14	-95.56	19.56	119.78	-104.37
32	2	Single Ended	Headphone	48	24	Linear Phase	16.66	104.38	-79.22	18.66	110.21	-84.35
32	2	Single Ended	Line Out	48	24	Linear Phase	16.07	104.34	-89.21	17.99	110.43	-94.70
48	1	Fully Differential	Headphone	24	24	Linear Phase	12.92	114.21	-90.63	14.16	118.07	-103.26
48	1	Fully Differential	Line Out	24	24	Linear Phase	12.32	115.11	-95.78	13.51	119.87	-104.04
48	1	Single Ended	Headphone	24	24	Linear Phase	11.92	104.36	-84.35	13.11	110.51	-86.95
48	1	Single Ended	Line Out	24	24	Linear Phase	11.65	104.32	-90.63	12.76	110.51	-96.04
48	2	Fully Differential	Headphone	48	24	Linear Phase	19.24	114.41	-80.62	21.59	118.04	-97.17
48	2	Fully Differential	Line Out	48	24	Linear Phase	18.09	115.11	-95.38	20.17	119.97	-103.95
48	2	Single Ended	Headphone	48	24	Linear Phase	17.25	104.47	-79.13	19.32	110.17	-84.22
48	2	Single Ended	Line Out	48	24	Linear Phase	16.72	104.44	-89.24	18.62	110.33	-94.50
96	1	Fully Differential	Headphone	24	24	Linear Phase	15.32	114.09	-90.73	16.61	117.99	-103.50
96	1	Fully Differential	Line Out	24	24	Linear Phase	14.75	114.91	-95.57	15.91	120.07	-103.91
96	1	Single Ended	Headphone	24	24	Linear Phase	14.35	104.39	-84.31	15.54	110.57	-86.60
96	1	Single Ended	Line Out	24	24	Linear Phase	14.06	104.44	-90.59	15.23	110.52	-95.45
96	2	Fully Differential	Headphone	48	24	Linear Phase	21.94	114.02	-80.61	24.29	118.01	-97.62
96	2	Fully Differential	Line Out	48	24	Linear Phase	20.83	114.93	-95.24	22.95	119.94	-103.90
96	2	Single Ended	Headphone	48	24	Linear Phase	20.02	104.4	-78.86	22.06	110.09	-84.72
96	2	Single Ended	Line Out	48	24	Linear Phase	19.39	104.36	-89.06	21.37	110.23	-95.20
192	1	Fully Differential	Headphone	24	24	Linear Phase	12.75	114.21	-89.96	14.01	117.93	-102.50
192	1	Fully Differential	Line Out	24	24	Linear Phase	12.17	114.71	-95.74	13.33	119.83	-104.21
192	1	Single Ended	Headphone	24	24	Linear Phase	11.79	104.36	-83.85	12.94	110.63	-86.51
192	1	Single Ended	Line Out	24	24	Linear Phase	11.49	104.49	-90.34	12.62	110.61	-95.48
192	2	Fully Differential	Headphone	48	24	Linear Phase	19.21	113.66	-80.69	21.52	117.97	-96.90
192	2	Fully Differential	Line Out	48	24	Linear Phase	17.98	114.6	-95.31	20.17	119.69	-103.70
192	2	Single Ended	Headphone	48	24	Linear Phase	17.21	104.27	-78.78	19.28	110.28	-84.98
192	2	Single Ended	Line Out	48	24	Linear Phase	16.61	104.42	-89.10	18.6	110.13	-95.23
384	1	Fully Differential	Headphone	24	24	Linear Phase	13.3	112.98	-89.71	14.58	117.19	-103.64
384	1	Fully Differential	Line Out	24	24	Linear Phase	12.73	113.54	-95.57	13.9	118.92	-104.18
384	1	Single Ended	Headphone	24	24	Linear Phase	12.32	104.34	-83.61	13.51	110.64	-87.11

Table 3-1. Target Mode Power Consumption With PLL Enabled (continued)

Sampling Frequency (kHz)	Enabled Channels	Output Configuration	Output Drive	BCLK-FS Ratio	Word Length	Decimation Filters	AVDD = 1.8V			AVDD = 3.3V		
							AVDD Current (mA)	Dynamic Range (dB-A weighted)	THD+N (dB)	AVDD Current (mA)	Dynamic Range (dB-A weighted)	THD+N (dB)
384	1	Single Ended	Line Out	24	24	Linear Phase	12.02	104.25	-90.37	13.18	110.68	-96.22
384	2	Fully Differential	Headphone	48	24	Linear Phase	21.05	112.02	-80.88	23.26	116.69	-96.67
384	2	Fully Differential	Line Out	48	24	Linear Phase	19.85	112.31	-95.44	21.98	117.79	-103.99
384	2	Single Ended	Headphone	48	24	Linear Phase	19.06	104.06	-79.99	21.04	110.04	-83.56
384	2	Single Ended	Line Out	48	24	Linear Phase	18.45	104.12	-90.16	20.34	109.94	-93.38

4 Settings for Lowest Power Consumption

To minimize the power consumption of the TAD52xx devices, verify that unused modules are disabled, use the lowest sampling rate, bit clock, and controller clock required by the application, and operate at the lowest AVDD and IOVDD supply voltage possible. The following list summarizes the settings and registers for lowest power operation:

- Operate at the lowest supply voltage possible. AVDD and IOVDD support a 1.8V or 3.3V supply, independently (AVDD and IOVDD can have different supply levels).
  - Unused digital inputs, tie to digital ground.
  - Unused outputs, leave unconnected.
- Disable unused DAC channels through the BO_PO_R118 (IN_CH_EN) register.
- Disable MICBIAS power, if unused, through the BO_PO_R120 (PWR_CFG) register.
- Operate at the lowest sample rate possible.
- Disable PLL, if the system supplies a low jitter controller clock. Refer to Section 2 for a description of the settings to disable PLL.
- Disable unused post-processing blocks:
  - Disable biquad filters, if unused, through the BO_PO_R115[4:3] (DSP_CFG) register.
- Select ultra-low latency over linear phase decimation filters (if the application allows) through the BO_PO_R115[7:6] (DSP_CFG) register.
- Use the smallest word length permissible by the application through the BO_PO_R26[5:4] (PASI_WLEN) register for primary ASI and BO_P3_R26[5:4] (SASI_WLEN) in cases of secondary ASI.

5 Summary

The typical power consumption matrix of the TAD52xx devices, across various usage scenarios, was tabulated in this document and recommendations for lowering power consumption were highlighted.

6 References

For related documentation see the following:

- Texas Instruments, *TAD5112 Low-Power Stereo Audio DAC With 106dB Dynamic Range*, data sheet.
- Texas Instruments, *TAD5112-Q1 Automotive Low-Power Stereo Audio DAC With 106dB Dynamic Range*, data sheet.
- Texas Instruments, *TAD5142 Hardware-Control Low-Power Stereo Audio DAC With 106dB Dynamic Range*, data sheet.
- Texas Instruments, *TAD5212 Low-Power Stereo Audio DAC With 120dB Dynamic Range*, data sheet.
- Texas Instruments, *TAD5212-Q1 Automotive Low-Power Stereo Audio DAC With 120dB Dynamic Range*, data sheet.
- Texas Instruments, *TAD5242 Hardware-Control Low-Power Stereo Audio DAC With 120dB Dynamic Range*, data sheet.

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