Application Note

Clock Edge Delay Compensation With Isolated Modulators Digital Interface to MCUs

Gizem Yuece, Alex Smith, Martin Staebler

ABSTRACT

Isolated Delta-Sigma modulators such as AMC1306M25 with high-speed digital interface are commonly used for accurate, low latency and high noise immunity shunt-based phase current sensing in servo drives and robotics applications. Especially at higher clock frequencies, proper routing, termination, and compliance with the corresponding MCU's setup and hold timings are critical for a reliable operation. A commonly used method and compromise to meet the MCU timing requirements is to reduce the modulator clock frequency, which also reduces the data output rate. This application note shows more designed for clock edge compensation methods to meet the setup and hold timing requirements up to the maximum clock rate of the modulator. This enables the system to operate at maximum data rate. The application note outlines options for clock edge compensation and shows example measurements with TI's isolated modulators AMC130x connected to C2000™ and Sitara™ MCUs. In addition, a calculation tool is provided to validate the digital interface timing.

Table of Contents

List of Figures

List of Tables

Trademarks

C2000™, Sitara™, OSR™, and Code Composer Studio™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

1 Introduction

Isolated Delta-Sigma Modulators are commonly used for shunt-based phase current sensing in servo drives and robotics applications as accurate and low latency isolated phase current sensing has a significant impact on the performance of three-phase inverters. Delta-Sigma modulators provide a digital bit stream with either LVDS or CMOS interface to an MCU that allows for exceptional noise immunity, high precision, and low latency phase current measurement. For additional information on isolated modulators, please see *Comparing Isolated Amplifiers and Isolated Modulators*, application note.

Often the shunts and the isolated Delta-Sigma modulators are placed on the power stage printed circuit board (PCB), while the MCU is placed on a separate control board PCB, as shown in figure 1. Proper routing schemes on the PCBs and the interface connector are crucial for digital signal integrity. Best practices for clock and data line routing and termination are discussed in *Better Signal Integrity w/ Isolated Delta-Sig. Modulators in Motor Drives (ti.com),* application report.

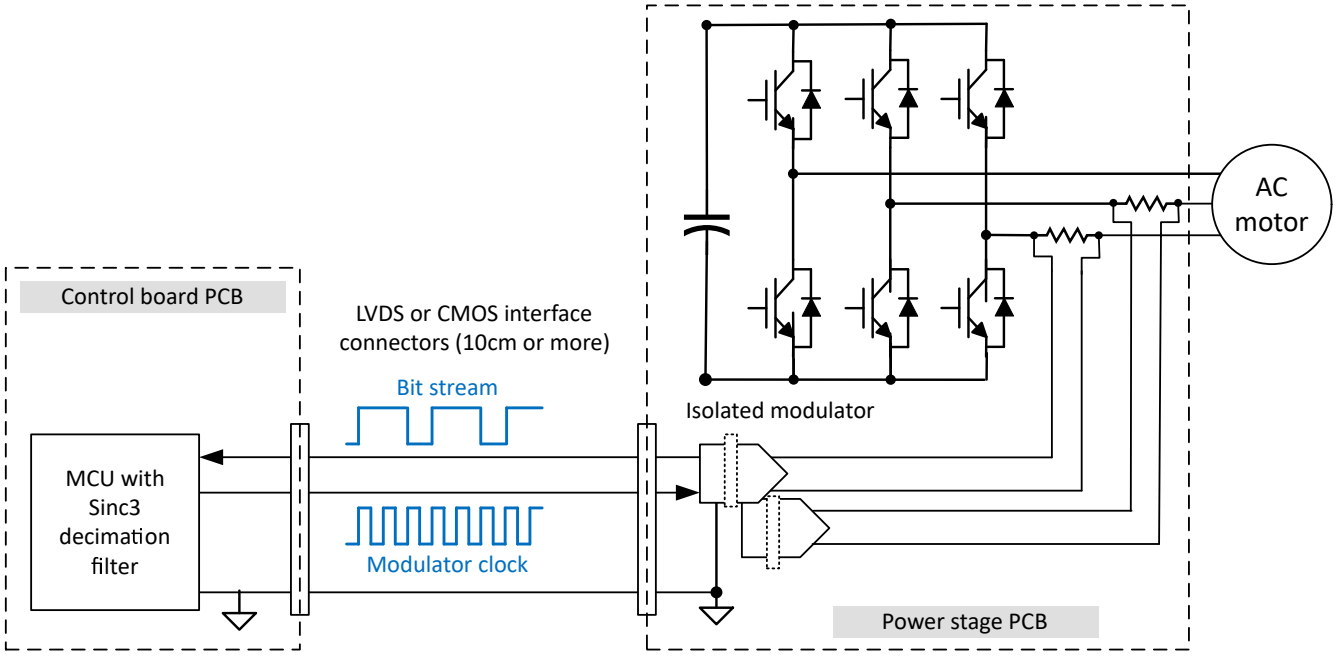


Figure 1-1. Simplified 3-Phase Inverter Block Diagram With Digital Interface From MCU to Isolator Modulators

There can be further design challenges to meet the timing between the modulator clock edge and the digital bitstream, especially when the signal traces are quite long, additional buffers and level translators are used. Then an additional propagation delay of the modulator clock and bitstream signal can even force designers to reduce the modulator clock from the maximum 21 MHz (AMC1306) to e.g. 15 MHz to meet the timing between clock edge and bitstream data at the MCU. Due to that the overall phase current measurement latency increases reverse proportional to the selected modulator clock. For example, a typically used Sinc3 decimation filter with an oversampling ratio of 64 has a measurement latency (propagation delay) of 4.8us at 20 MHz modulator clock, while the latency increases to 6.4us when only a 15 MHz modulator clock can be used.

The following sections of this document provide an overview of digital timing compensation methods to overcome this design challenge and show that designing with an isolated modulator offers not only the highest precision measurement but also the easiest.

2 Design Challenge With Digital Interface Timing Specifications

Isolated Delta-Sigma modulators offer interface options for both an externally and internally generated clock signal with either a CMOS interface or a LVDS interface. For devices with externally-provided clock source, for example AMC1306M25 with CMOS interface or AMC1305L25 with LVDS interface the clock signal is routed from the MCU to the Delta-Sigma modulator's clock input, whereas for devices with an internally-provided clock source, the output bit-stream is synchronized to the internally generated clock, for exampleAMC1303M2520. There are also isolated Delta-Sigma modulator devices with Manchester coded output bit stream that support single-wire data and clock transfer, for example AMC1306E25. For all isolated Delta-Sigma modulators, the data output of the modulator provides a bit stream of digital ones and zeros that is shifted out synchronous to the clock edge.

Figure 2-1 shows a simplified example of CMOS interface with 3.3V I/O between the isolated Delta-Sigma modulator AMC1306M25 and a C2000 MCU TMS320F28379D. As the AMC1306M25 requires an externally-provided clock source, the clock signal is generated by the MCU TMS320F28379D and is provided to the Delta-Sigma modulators clock input, CLKIN. In parallel, the generated clock signal is also routed to the clock input to the MCUs Sigma-Delta Filter Module (SDFM) SD1_C1 (GPIO123). Depending on the system design there can be a clock buffer included in the clock interface between the MCU and the isolated Delta-Sigma modulator. The isolated data output DOUT of the Delta-Sigma modulator is directly connected to the MCUs Sigma-Delta Filter Module (SDFM) data input SD1_D1 (GPIO122).

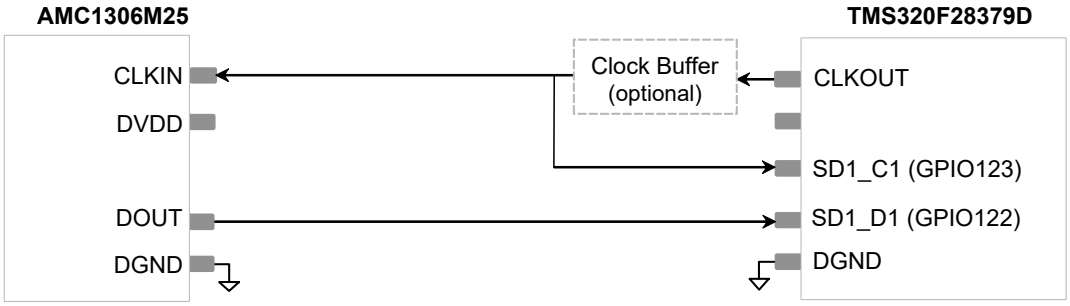


Figure 2-1. Simplified AMC1306M25 Digital Interface to TMS320F28379D

Valid communication between the isolated Delta-Sigma modulator and the MCU is described in the respective device data sheets by the setup and hold timing requirements. The setup time is the amount of time that the data signal must be valid and stable prior to a clock signal transition to capture the data signal in the MCU. Hold time is the amount of time that a signal must be held valid and stable after a clock signal transition occurs. Meeting the MCUs setup and hold time requirements is crucial as any violation can cause incorrect data to be captured. Incompatibility between the digital interface setup and hold timing requirements of the isolated Delta-Sigma modulator and the MCU can present a design challenge.

Figure 2-2 outlines the digital interface timing for setup and hold time of the AMC1306x which supports a recommended clock frequency (CLKIN) from 5 MHz to 21 MHz with a data hold time t_h(MIN) = 3.5 ns and a data delay time t_d (MAX) = 15 ns.

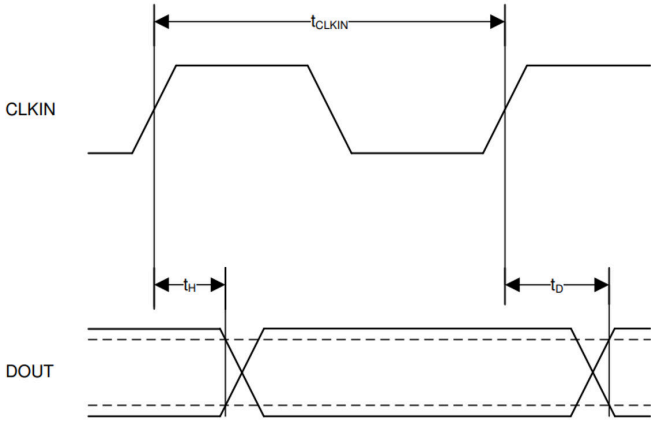


Figure 2-2. AMC1306x Digital Interface Timing

Figure 2-3 outlines the timing diagram, of the TMS320F28379D Sigma-Delta Filter Module (SDFM) for Mode 0. The data input at SDx_Dy needs to meet the minimum setup time $t_{su(SDDV-SDCH)M0}$ and minimum hold time $t_{h(SDCH-SDD)M0}$ with reference to the rising clock edge of the SDx_Cy signal in the SDFM module.

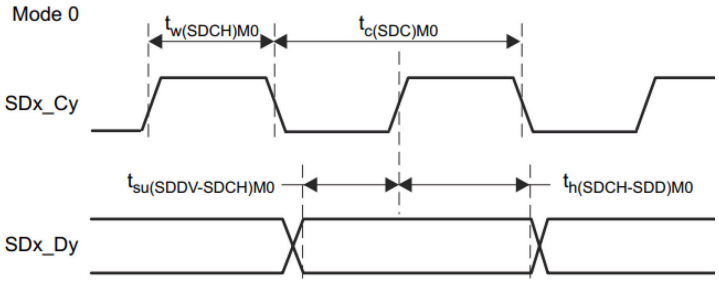


Figure 2-3. TMS320F28379D SDFM Timing Diagram – Mode 0

For the TMS320F28379D SDFM module in Mode 0, we recommend to use the SDFM operation with qualified GPIO (3-sample window). This mode provides protection against random noise glitches with the input clock signal (SDx_Cy) and data input (SDx_Dy) to avoid false comparator over-current trip and false Sinc filter output. The minimum setup and hold times for a 200 MHz system clock with TMD320F28379D are both 10 ns: $t_{su\ (SDDV-SDCH)M0}$ (MIN) = 10 ns and $t_{h(SDCH-SDD)M0}$ (MIN) = 10 ns.

This creates a design challenge as the AMC1306M25 minimum hold time t_h(MIN) is 3.5 ns, but 10 ns is required for the SDFM module to maintain correct acquisition at the data input SDx_Dy with reference to the rising clock edge of the SDx_Cy signal.

An additional challenge is that the propagation delay of additional components in the signal chain with the digital interface such as a clock buffer as well as the propagation delay of the clock and data signals introduced by the trace length on the PCB have an impact on the timings between SDx_Cy and SDx_Dy inputs and complicate the correct acquisition timing of the data input.

The same applies to Delta-Sigma modulators with a LVDS interface, such as the AMC1305L25. The only difference to AMC1306M25 Delta-Sigma modulators with CMOS interface type is that additional components like a LVDS driver and receiver are required with the digital signal chain to a MCU with CMOS interface, which contribute to further propagation delays. Figure 2-4 shows a simplified digital interface between the isolated Delta-Sigma modulator AMC1305L25 with LVDS interface and the MCU TMS320F28379D with CMOS interface.

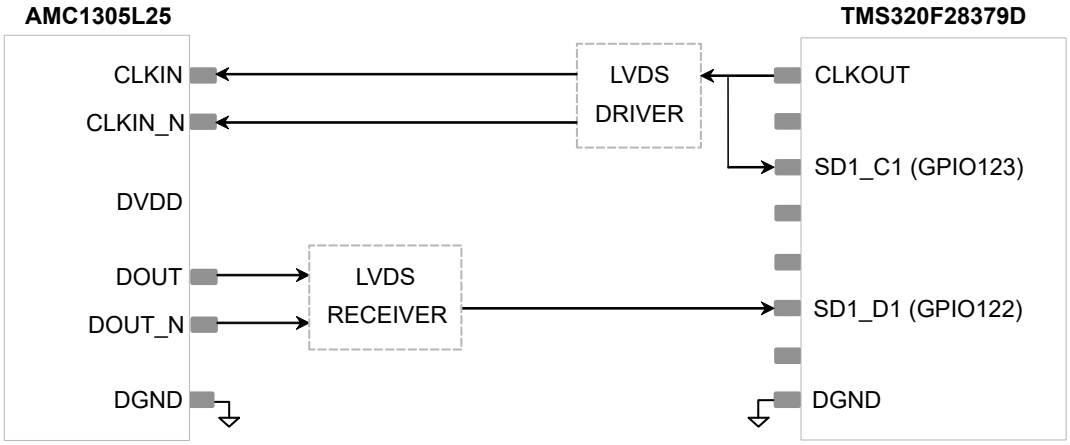


Figure 2-4. AMC1305L25 Digital Interface to TMS320F28379D

Figure 2-5 shows a simplified digital interface of an isolated Delta-Sigma modulator with internally-created clock source AMC1303Mx with CMOS interface to TMS320F28379D with CMOS interface. The internally generated clock signal CLKOUT of the AMC1303Mx is input to the MCUs Sigma-Delta Filter Module (SDFM) SD1_C1 (GPIO123). The isolated data output DOUT of the Delta-Sigma Modulator is directly connected to MCUs data input SD1_D1 (GPIO122) of the SDFM.

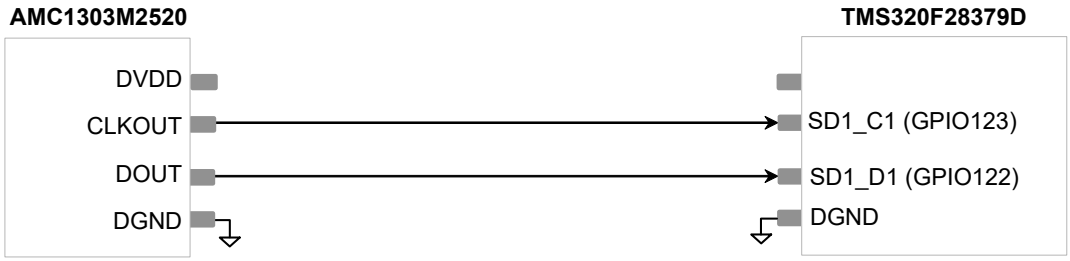


Figure 2-5. AMC1303M2520 3.3-V CMOS Digital Interface to TMS320F28379D

When using an isolated modulator with an internal clock, the digital interface challenge is limited to the different timing specifications of the isolated Delta-Sigma modulator and the MCUs setup and hold times. The propagation delay of clock and data signals introduced by the trace length on the PCB can be neglected if the clock and data signals are routed at the same length. Typically, the modulator is directly interfaced to the MCU and there's no need for a buffer or level-shifter, which adds additional propagation delay.

The AMC1303Mx hold time t_h(MIN) is 7 ns and the delay time t_d (MAX) is 15 ns for the 10 MHz and 20 MHz clock versions. The challenge is that the AMC1303Mx minimum hold t_h(MIN) is 7 ns, but 10 ns is required by the SDFM module for correct acquisition of the data input at SDx_Dy without any setup and hold time violations.

For isolated Delta-Sigma modulators with a Manchester encoded bitstream output, e.g. AMC1306E25, data and clock are transferred through a single-wire. So that the setup and hold time requirements of the receiving device versus the modulator clock do not have to be considered.

A commonly used method and compromise to meet the MCUs setup and hold time requirements is to reduce the clock frequency. However, reducing the clock frequency is also reducing the data output rate of the isolated Delta-Sigma modulator and increases the latency of the current measurement. A more suitable method is to use clock edge delay compensation which enables moving the clock edge of the clock signal to an ideal sample point of the data signal to meet the setup and hold timing requirements. By using this method, the clock frequency limitations are eliminated which allows the isolated Delta-Sigma modulator and the system to operate at full performance.

3 Design Approach With Clock Edge Delay Compensation

To meet and further optimize the MCUs setup and hold timing requirements for reliable data acquisition, clock edge delay compensation is recommended. Clock edge delay compensation can be implemented by various methods, summarized below and expanded upon in the following section:

1. Additional clock signal with software configurable phase delay
2. Clock signal with hardware configurable phase delay
3. Clock return
4. Clock inversion at MCU

3.1 Clock Signal Compensation With Software Configurable Phase Delay

Figure 3-1 shows the first compensation method, where an additional phase locked clock signal with a software configurable phase delay is used. For this compensation method the phase-shifted clock signal CLKOUT_delay is used as the clock input to SD0_CLK of the Sigma-Delta Filter Module (SDFM). For other types of Delta-Sigma Modulators and MCUs e.g. C2000 MCUs, the compensation method follows the same principle.

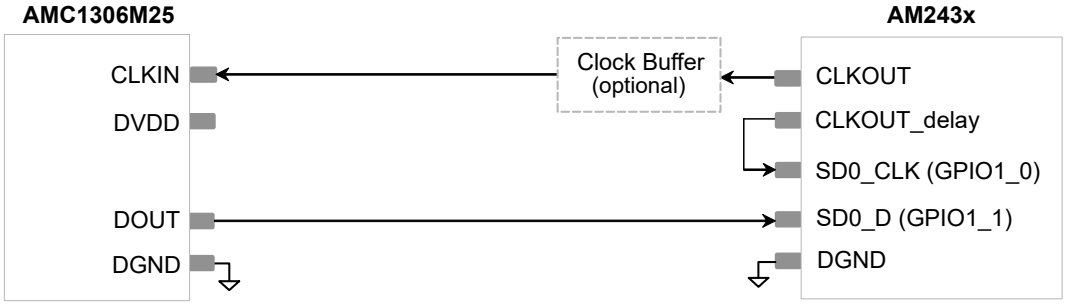


Figure 3-1. AMC1306M25 to AM243x MCU Interface With Software Configurable Clock Phase Delay

The implementation of a second phase-shifted clock signal offers the highest degree of freedom and user configurability. This means that various values for minimum hold time t_h(MIN) of various isolated modulators can be compensated by a simple change to the phase-shift value in software. The clock signals rising edge at the SD0_CLK input is phase-shifted such that the clocking signal complies with the data sampling point of the SDFM, as shown in Figure 3-2. The AM243x PRU_ICSSG PRU Timing Requirements in Sigma Delta Mode are 10 ns for minimum setup time $t_{su\ (SD\_D\text{-}SD\_CLK)}$ (MIN) = 10 ns and 5 ns for minimum hold time $t_{h(SD\_CLK\text{-}SD\_D)}$ (MIN) = 5 ns. This creates a need for compensation to maintain correct acquisition at the data input SDx_D with reference to the rising clock edge of the SDx_CLK signal as the AMC1306M25 minimum hold time t_h(MIN) is 3.5 ns, but 5 ns can be required. After this compensation method is applied, the 10-ns minimum setup and 5-ns hold timings for the Sigma Delta Mode of the AM243x PRU_ICSSG PRU timing requirements are met, see Figure 3-2.

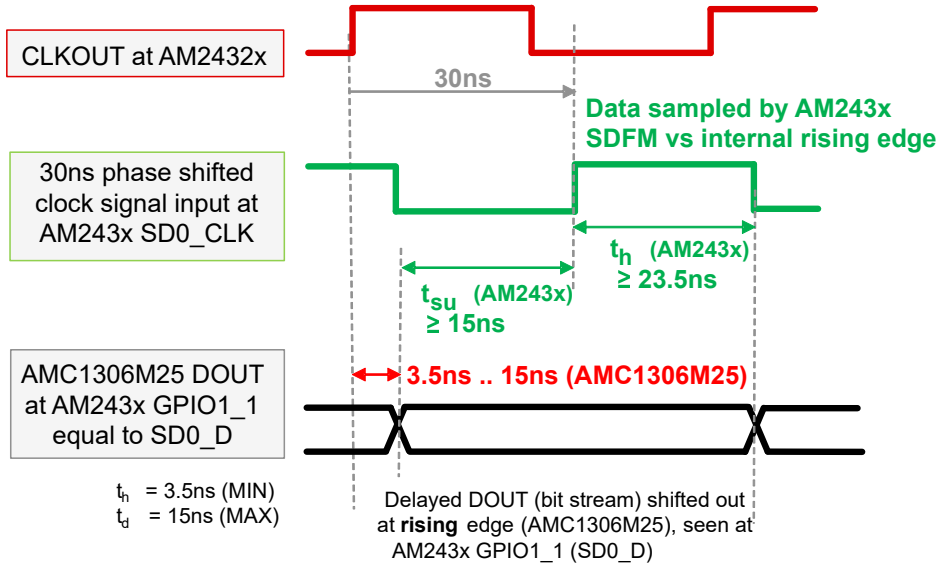


Figure 3-2. AM243x SDFM Timing With 30-ns Phase-Shifted Clock Signal Input at SD0_CLK (GPIO1_1)

3.2 Clock Signal Compensation With Hardware Configurable Phase Delay

Clock signal compensation with hardware configurable phase delay of the digital interface between AMC1306M25 and MCU is shown in Figure 3-3. With this compensation method a phase-shifted clock signal by a phase delay in hardware is connected to the clock input SDFM_CLKIN of the SDFM module of the MCU. This type of compensation works for any MCU with Sigma-Delta Filter Module, but is only recommended for isolated Delta-Sigma Modulator's with an external clock source and CMOS interface.

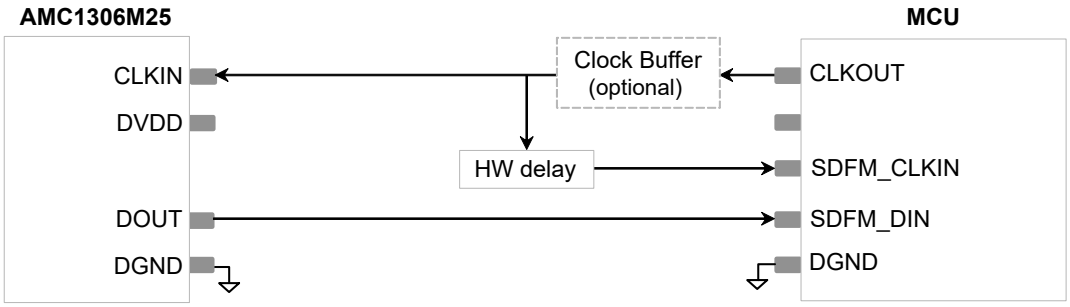


Figure 3-3. AMC1306M25 Digital Interface to MCU With Compensation by Hardware Configurable Phase Delay

To implement a phase delay in hardware, a logic gate or buffer can be used to introduce a propagation delay in the clock signal. However, when implementing a delay in hardware the value of the delay is strongly dependent on the propagation delay of the hardware block limiting the degree of freedom and user configurability. The working principle of the compensation by clock signal with hardware configurable phase delay follows the same principle described in Section 3.1.

3.3 Clock Signal Compensation by Clock Return

Clock Signal Compensation by Clock Return is shown in Figure 3-4. With this compensation method, the clock signal that is fed into CLKIN the clock input of the AMC1306M25, is routed back from the CLKIN Pin of the AMC1306M25 to the SDFM clock input SDFM_CLKIN of the MCU.

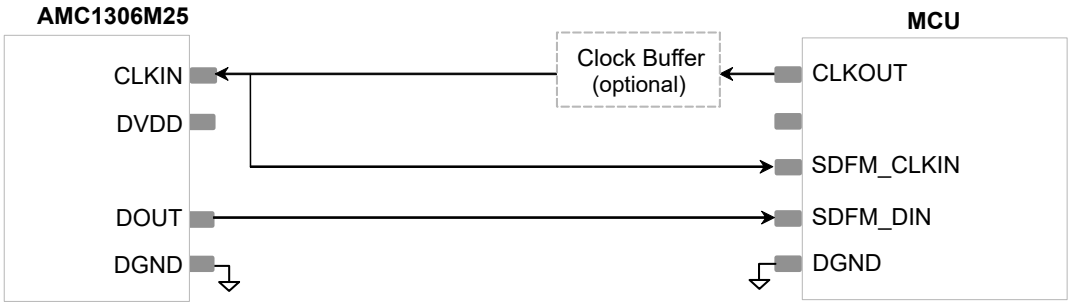


Figure 3-4. AMC1306M25 Digital Interface to MCU With Compensation by Clock Return

By using this method, the same propagation delay by the clock buffer and the propagation delay introduced by the PCB trace length is achieved for the clock and data signal. Therefore, these delays in the clock and data signals cancel each other out.

However, the AMC1306M25 digital interface timing for data hold time t_h(MIN) = 3.5 ns and data delay time t_d (MAX) = 15 ns remains. This means that the timing needs to be checked after the PCB has been built to verify that the setup and hold timing requirements of the MCU for the SDFM are met. This type of compensation method is only recommended for isolated Delta-Sigma modulator with external clock source and CMOS interface.

3.4 Clock Signal Compensation by Clock Inversion at the MCU

The last method for clock signal compensation is clock inversion at the MCU and works for Delta-Sigma modulators with external and internal clock source. In that case, the selected MCU must be capable of inverting the GPIO input. The TMS320F28379D GPIO inputs prior to the SDFM (Sigma Delta Filter Module) can be configured to invert the input signal at any GPIO, as shown in Figure 3-5. For example, the clock input signal is inverted at GPIO123, hence the SD1_C1 clock signal is inverted versus the AMC1303Mx clock signal. As a result, the SDFM samples the input data SD1_D1 versus the falling edge of the external clock signal at the input of GPIO123, as shown in Figure 3-6.

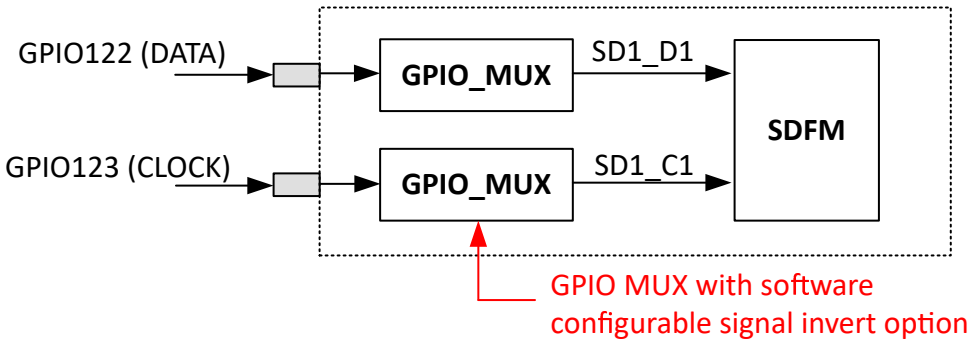


Figure 3-5. TMS320F28379D SDFM/GPIO Block Diagram

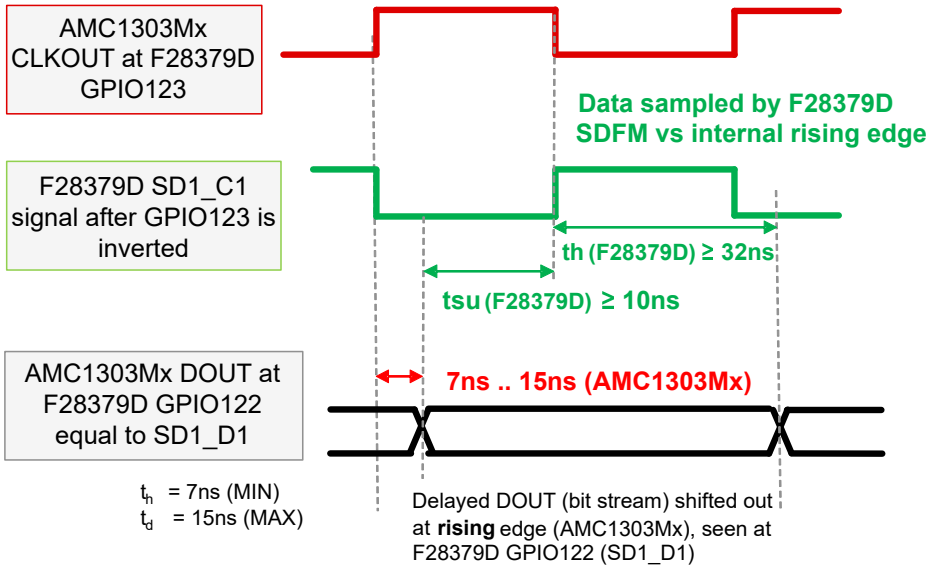


Figure 3-6. TMS320F28379D SDFM Timing With Inverted Clock at GPIO123

By inverting the clock input signal by using the GPIO a fixed delay of one-half of the clock period is added to the clock signal. Depending on the timing specifications and propagation delays of the system setup, this additional delay may be sufficient to meet the TMS320F28379D setup and hold timings of minimum 10 ns for the SDFM qualified GPIO (3-sample) mode 0. However, as this clock signal compensation method's additional delay time is fixed and cannot be changed, it must be verified for each system design that the resulting timings for setup and hold of the MCU for the SDFM qualified GPIO (3-sample) mode 0 are met.

This compensation method is also applicable to Sitara MCUs, where both the rising and falling edges of the external clock signal can be set as data acquisition point by software.

4 Test and Validation

The following sections present clock edge compensation test results using an additional clock signal with phase delay in software as described in Section 3.1 as well as clock inversion as described in Section 3.4. First, the test equipment and software are described, followed by the test setup, measurements and test results of the clock signal compensation methods.

4.1 Test Equipment and Software

The key test equipment for the measurements are listed in Table 4-1.

Table 4-1. List of Test Equipment

Description	Part Number
AMC1306 reinforced isolated modulator evaluation module	AMC1306EVM
F28379D LaunchPad™ development kit for C2000™ Delfino™ MCU	LAUNCHXL-F28379D
AM243x general purpose LaunchPad™ development kit for Arm®-based MCU	LP-AM243
High-speed oscilloscope	Tektronix MSO 4104
Single-ended probes	Tektronix P6139A

Software development and debugging is done with Code Composer Studio (CCS) version 12.4.0. CCS is an integrated development environment (IDE) that supports Texas Instruments microcontroller (MCU) and embedded processor portfolios. An internal TI test software was used for the TMS320F28379D based on the C2000WARE — C2000Ware for C2000 Microcontrollers. For the Sitara AM243x Launchpad an internal TI test software was used based on the AM243x software development kit (SDK) for Sitara™ microcontrollers MCU-Plus-SDK-AM243X Version 09.00.00.35. For specific implementation and software support of C2000 and Sitara refer to TI E2E support forums.

4.2 Testing of Clock Signal Compensation With Software Configurable Phase Delay

This measurement validates that the setup and hold timing requirements are met with clock signal compensation by using an additional clock signal with a software configurable phase delay. This test was performed and validated with both the C2000 TMS320F28379D Launchpad and Sitara AM243x Launchpad.

4.2.1 Test Setup

The test setup of the clock signal compensation by using an additional clock signal with a software configurable phase delay measurement with an AMC1306EVM and C2000 TMS320F28379D Launchpad is shown in Figure 4-1. For this measurement, single-ended probes are used to measure the clock signal at AMC1306EVM clock input CLKIN and the data output, DOUT, of the Delta-Sigma modulator measured at the MCUs data input, SD1_D1 (GPIO122), of the SDFM. The clock signal with software programmable phase delay is measured at the clock input of the MCUs Sigma-Delta Filter Module (SDFM) SD1_C1 (GPIO123). The input pins AINP and AINN of the AMC1306EVM are shorted together tied to ground such that a 50/50 1's and 0's density is output. The analog supply, AVDD, is generated using the isolated transformer circuit on the EVM. The isolated modulators digital power supply, DVDD (3.3V), is supplied from the C2000 TMS320F28379D Launchpad.

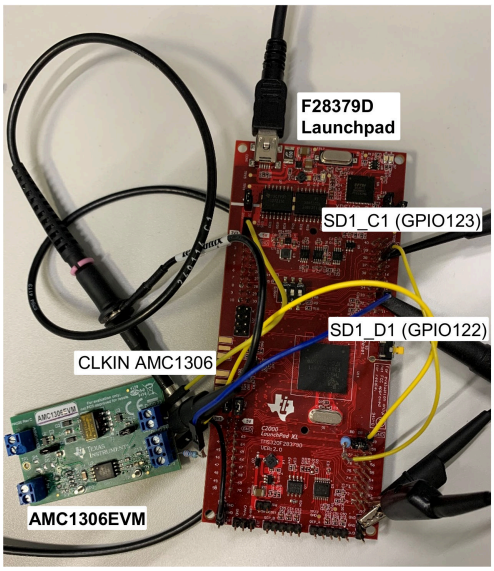


Figure 4-1. Test Setup of Clock Signal Compensation by Phase Delay in Software With AMC1306EVM and C2000 TMS320F28379D Launchpad

Figure 4-2 shows the same measurement setup with Sitara AM243x Launchpad with the corresponding measurement points.

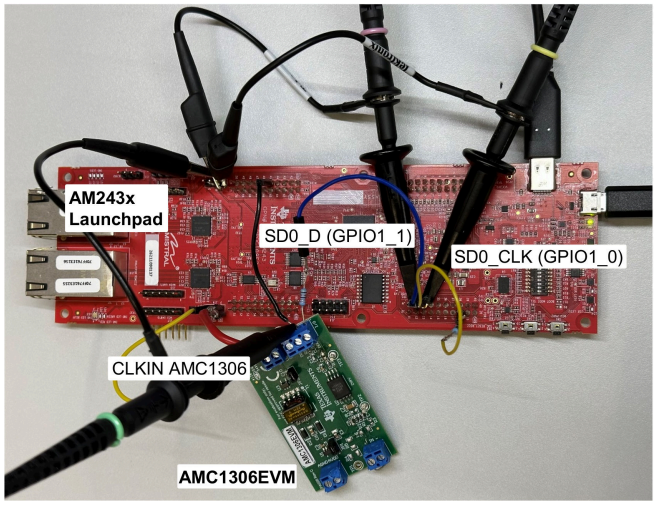


Figure 4-2. Test Setup of Clock Signal Compensation by Software Configurable Phase Delay With AMC1306EVM and Sitara AM243x Launchpad

4.2.2 Test Measurement Results

The TMS320F28379D was running an internal TI SDFM software project, where the two GPIOs GPIO122 and GPIO123 are configured for SDFM mode. The SDFM data filter is configured for Sinc3 with an oversampling ratio of 64 (OSR64). To conduct the test, a 20-MHz clock signal with a 50% duty cycle is generated with the ePWM4 module and fed into the CLKIN Pin of the AMC1306EVM. The ePWM5 module is configured to output a phase-locked 20-MHz clock signal with 50% duty cycle and 30-ns phase-shift. This signal is fed into SD1_C1 (GPIO123). Note that the AMC1306EVM DOUT data bitstream only changes at the rising clock edge, hence once per clock cycle as described in Section 7.11 *Switching Characteristics* of the AMC1306 data sheet.

Figure 4-3 shows the oscilloscope measurement and the interface diagram. The clock signal fed into the AMC1306EVM CLKIN Pin is represented by the green waveform on channel 3. The data signal output by the AMC1306EVM is the SD1_D1 (GPIO122) signal in red on channel 2. The phase-shifted clock signal fed into SD1_C1 (GPIO123) is the measured waveform in blue on channel 1. As the SDFM module samples the data

signal against the rising edge of the phase-shifted clock signal SD1_C1 (GPIO123), the resulting setup time is approximately 18 ns and the resulting hold time is approximately 24 ns. With that the TMS320F28379D setup and hold timing of minimum 10 ns for the SDFM qualified GPIO (3-sample) mode 0 is met. In addition, this design offers an optimum margin to allow tolerances for changes (positive or negative) in the system propagation delay.

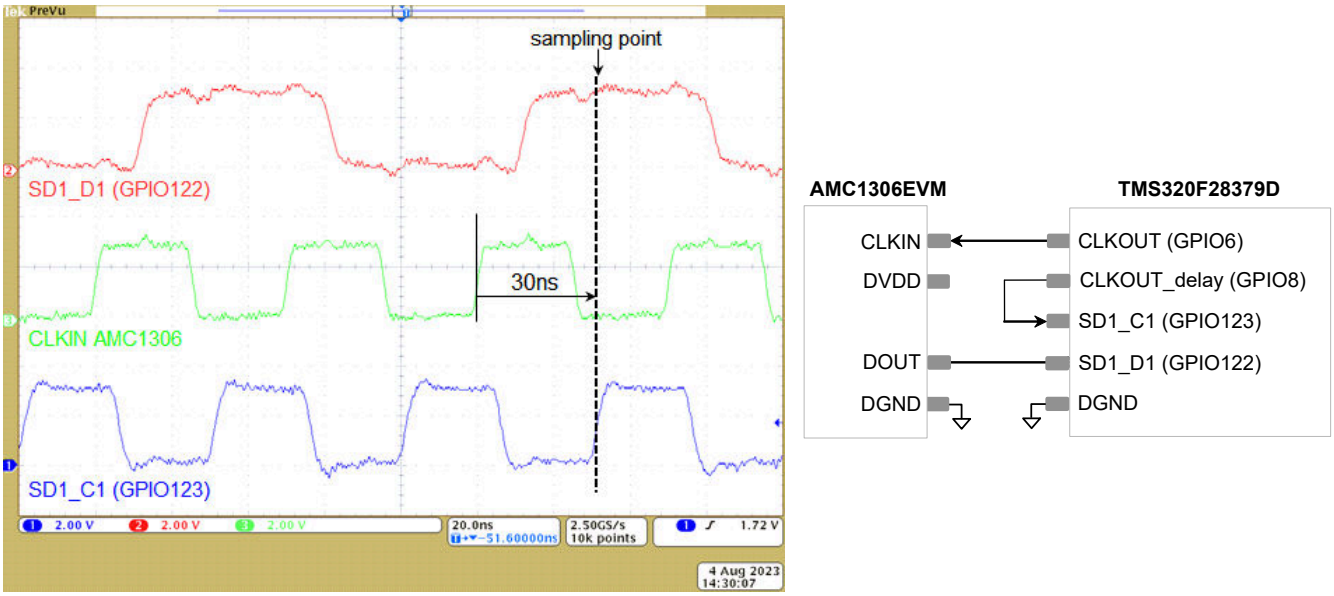


Figure 4-3. Measurement Results of Digital Interface Timing of AMC1306EVM and TMS320F28379D With Clock Signal Compensation by Software Configurable Phase Delay

Figure 4-4 shows the same measurement results for the test performed with the Sitara AM243x Launchpad. In conclusion the clock signal compensation by using an additional clock signal with a software configurable phase delay is an approved method to meet the MCUs setup and hold timing requirements. This method offers the highest degree of freedom, since not only the value of the phase shift is configurable, but this method also works for a wide range of MCUs due to only requiring an additional GPIO pin for the implementation of a phase shifted clock signal.

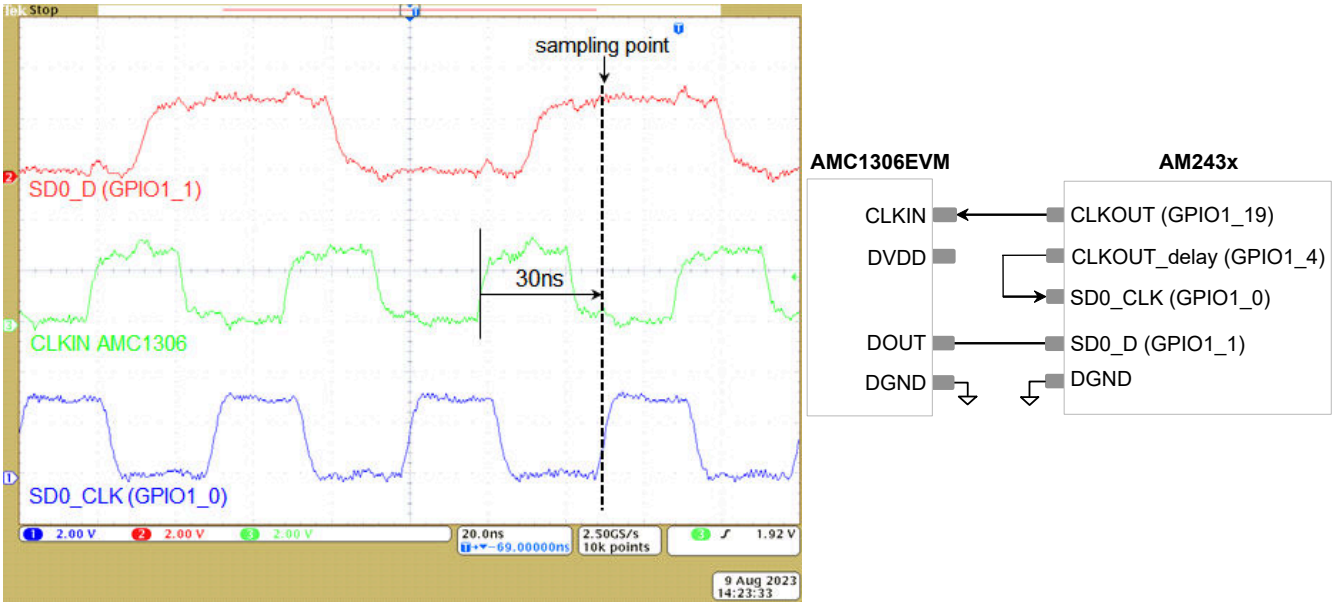


Figure 4-4. Measurement Results of Digital Interface Timing of AMC1306EVM and AM243x With Clock Signal Compensation by Software Configurable Phase Delay

4.3 Testing of Clock Signal Compensation by Clock Inversion at MCU

This configuration has been tested and validated with the C2000 TMS320F28379D Launchpad.

4.3.1 Test Setup

The test setup for clock signal compensation by clock inversion at the MCU using the C2000 TMS320F28379D Launchpad is shown in Figure 4-5. For this measurement two test signals are created by the MCU. One signal is connected to the clock input, SD1_C1, (GPIO123) of the MCUs SDFM and the other signal is connected to the data input, SD1_D1, (GPIO122) of the SDFM.

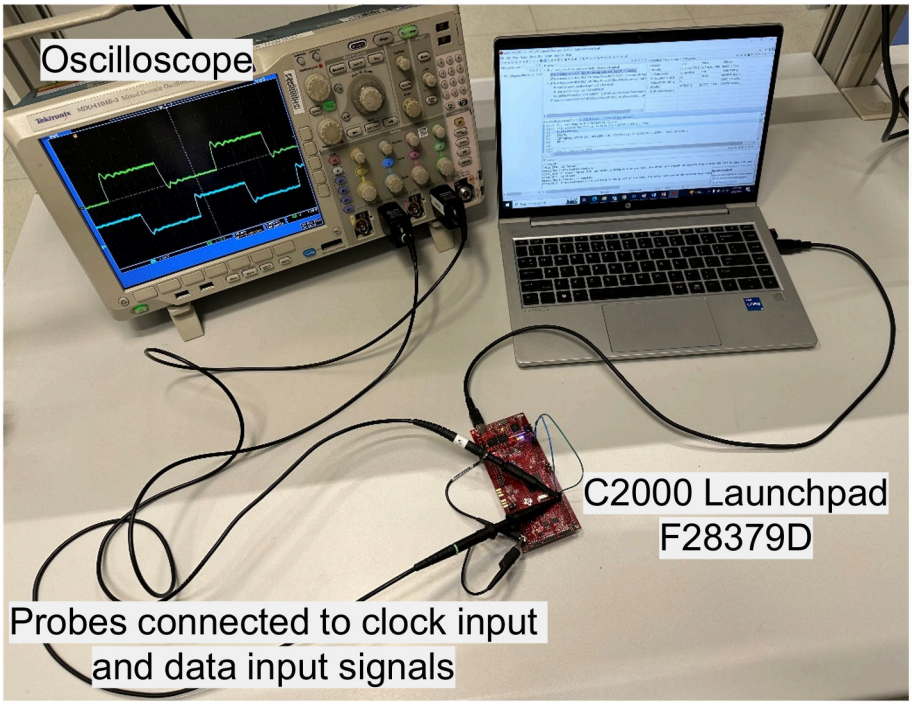


Figure 4-5. Test Setup of Digital Interface Timing Validation

4.3.2 Test Measurement Results

The TMS320F28379D was running an internal TI SDFM software project, where the two GPIOs GPIO122 and GPIO123 are configured for SDFM mode. The SDFM filter is configured for Sinc3 and OSR™ 64 filter. The Sinc3 OSR64 filter outputs a 16-bit two's complement integer number with a maximum full-scale range from +16384 to -16384.

To conduct the test, two 90-degree phase shifted 10-MHz clock signals with a 50% duty cycle are fed into GPIO123 (SD1_C1) and GPIO122 (SD1_D1) respectively. Note that the AMC1306EVM DOUT data bitstream only changes on the rising clock edge, hence once per clock cycle. For this test the SD1_D1 data toggles between 0 and 1 at every half clock cycle. This is different than the AMC1306EVM DOUT data signal, which changes at every clock cycle.

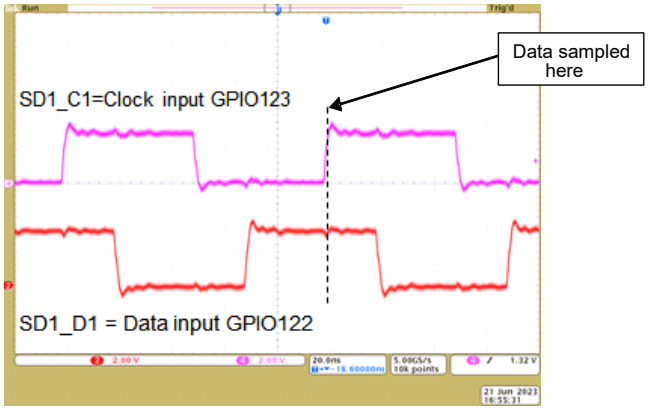
Due to applying this specific test signal, the input data at GPIO122 (SD1_D1) is always logic '1' at the rising clock edge of GPIO123 and always logic '0' at the falling edge. Hence the output of the Sinc3 filter with OSR 64 filter depends on which clock edge the test data is sampled in the SDFM and the Sinc3 OSR 64 filter output is either 16384 (always sampling '1') if there is no clock inversion at GPIO123 and -16384, if there is a clock inversion at GPIO123 (always sampling '0').

4.3.2.1 Test Result – No Clock Inversion of Clock Input at GPIO123

Figure 4-6 shows the oscilloscope measurement of the clock signal SD1_C1 which is input to GPIO123 and the phase shifted data signal SD1_D1 which is input to GPIO122. In this measurement GPIO123 is not inverted by the software, as shown below.

```
// Set 3-sample qualifier for GPIO122 and GPIO123 and do not invert GPIO123
GPIO_SetupPinOptions(122, GPIO_INPUT, GPIO_QUAL3);       // GPIO123 not inverted
GPIO_SetupPinMux(122,GPIO_MUX_CPU1,7); // MUX position 7 for SD1_D1
GPIO_SetupPinMux(123,GPIO_MUX_CPU1,7); // MUX position 7 for SD1_C1
```

The data SD1_D1 is sampled by the TMS320F28379D SDFM at the rising edge of SD1_C1. This corresponds to the rising edge of the non-inverted clock signal at GPIO123. The data sampled by the TMS320F28379D was always logic '1', validated through output of the Sinc3 OSR64 filter = +16384 in Code Composer Studio™ (CCS), as shown below.



Variables | Expressions | Registers

Expression	Type	Value	Address
GpioCtrlRegs.GPDINV.bit.GPIO123	unsigned int : 1	0	0x00007CD1@Data bit 11
SD1_D1_SincOSR64	int	16384	0x00014147@Data

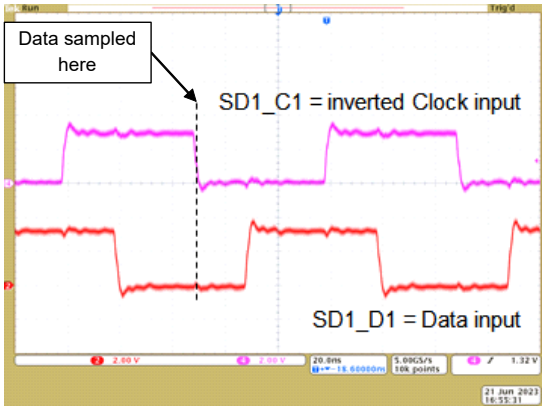
Figure 4-6. Clock and Data Input Test Signals (Non-Inverted GPIO123) and Sinc3 OSR 64 Filter Output in CCS

4.3.2.2 Test Result – Clock Inversion of Clock Input at GPIO123

Figure 4-7 shows the clock signal SD1_C1 which is input to GPIO123 and the phase shifted data signal SD1_D1 which is input to GPIO122. In this test setup GPIO123 is inverted by the software, as shown below.

```
// Set 3-sample qualifier for GPIO122 and GPIO123 and do not invert GPIO123
GPIO_SetupPinOptions(123, GPIO_INPUT, GPIO_INVERT | GPIO_QUAL3);
GPIO_SetupPinMux(122,GPIO_MUX_CPU1,7); // MUX position 7 for SD1_D1
GPIO_SetupPinMux(123,GPIO_MUX_CPU1,7); // MUX position 7 for SD1_C1
```

The data SD1_D1 is now sampled by F28379D SDFM at the falling edge of SD1_C1, which corresponds to the rising edge of the inverted clock signal at GPIO123 input. The data sampled by the F28379D was always logic '0', validated though output of the Sinc3 OSR64 filter = -16384 in Code Composer Studio, as shown below.



Variables | Expressions | Registers

Expression	Type	Value	Address
GpioCtrlRegs.GPDINV.bit.GPIO123	unsigned int : 1	1	0x00007CD1@Data bit 11
SD1_D1_SincOSR64	int	-16384	0x00014147@Data

Figure 4-7. Clock and Data Input Test Signals (Non-Inverted GPIO123) and Sinc3 OSR 64 Filter Output in CCS

In conclusion the method of clock signal compensation by inverting the clock input of the GPIO input in software was validated. By inverting the clock, a fixed delay of half of the clock period is added to the clock signal which can be sufficient to meet the TMS320F28379D setup and hold of minimum timings of 10 ns for the SDFM qualified GPIO (3-sample) mode 0. However, each system design needs to be checked individually if the resulting timings for setup and hold of the MCU for the SDFM qualified GPIO (3-sample) mode 0 can be met.

4.4 Digital Interface Timing Validation by Calculation Tool

A calculation tool was developed for simulation and validation purposes of the digital interface timings between an MCU and isolated Delta-Sigma modulators. The most common used isolated Delta-Sigma modulators AMC1306M25 and AMC1305L25 were selected for the digital interface timing analysis. AMC1305L25 has a LVDS interface type and requires LVDS driver and LVDS receiver when interfacing a MCU with CMOS interface. The MCU can be individually selected by the user, as only the setup and hold time requirements are entered into the calculation tool. In the following use of the calculation tool for the optimization of the digital interface timing between AMC1305L25 and C2000 MCU TMS320F28379D is shown step by step.

4.4.1 Digital Interface With No Compensation Method

The C2000 MCU TMS320F28379D is operated in SDFM GPIO input qualification (3-sample window) option in mode 0 at 200 MHz system clock. The minimum setup and hold time are both 10 ns: $t_{su\ (SDDV-SDCH)M0}$(MIN) = 10 ns and $t_{h(SDCH-SDD)M0}$ (MIN) =10 ns are entered into the calculation tool. Furthermore, propagation delays of LVDS driver DSLVDS1047 and LVDS receiver DSLVDS1048 are entered for reference. With a 20-MHz clock signal at the isolated Delta-Sigma modulator clock input, which is the maximum clock frequency specified in the data sheet, the MCUs setup time requirements are violated when the data delay time t_D of AMC1305L25 equals the minimum specification given in the data sheet with t_D (MIN) = 0 ns, as shown in table 2.

Table 4-2. Results for C2000 MCU TMS320F28379D Digital Interface Timings Using AMC1305L25 at 20-MHz Clock Frequency

Min. Setup Time @MCU	5.6 ns
Max. Setup Time @MCU	23.3 ns
Min. Hold Time @MCU	26.7 ns
Max. Hold Time @MCU	44.4 ns

4.4.2 Commonly Used Method - Reduction of the Clock Frequency

A compromise to meet the MCUs timing requirements is to reduce the modulator clock frequency. In this example a 17 MHz clock frequency allows the setup and hold timing requirements of the MCU to be met. The

calculated setup and hold times including minimum and maximum values at a clock frequency of 17 MHz are shown in Table 4-3. The margin for the minimum setup time to the MCUs setup time requirement is 0 ns. This means tolerances in the system can possibly lead to incorrect acquisition of data. A larger margin for tolerances in the system can be achieved by further reducing the clock frequency, but this has a negative effect on the system performance.

Table 4-3. TMS320F28379D Digital Interface Timings Using AMC1305L25 at 17-MHz Clock

Min. Setup Time @MCU	10.0 ns
Max. Setup Time @MCU	27.7 ns
Min. Hold Time @MCU	31.1 ns
Max. Hold Time @MCU	48.8 ns

4.4.3 Clock Edge Compensation With Software Configurable Phase Delay

The digital interface with clock edge compensation with software configurable phase delay is shown in Figure 4-8. The timing diagram shows a clock signal with a clock frequency of 20 MHz, representing the clock signal which is fed into the isolated Delta-Sigma modulator, as the first signal. The second signal plotted in the timing diagram represents the data output of the isolated Delta-Sigma modulator for typical specifications given in the data sheet. The third signal represents the 20-MHz clock signal phase-shifted by 10 ns in reference to the first signal which is fed into the clock input of the MCUs SDFM.

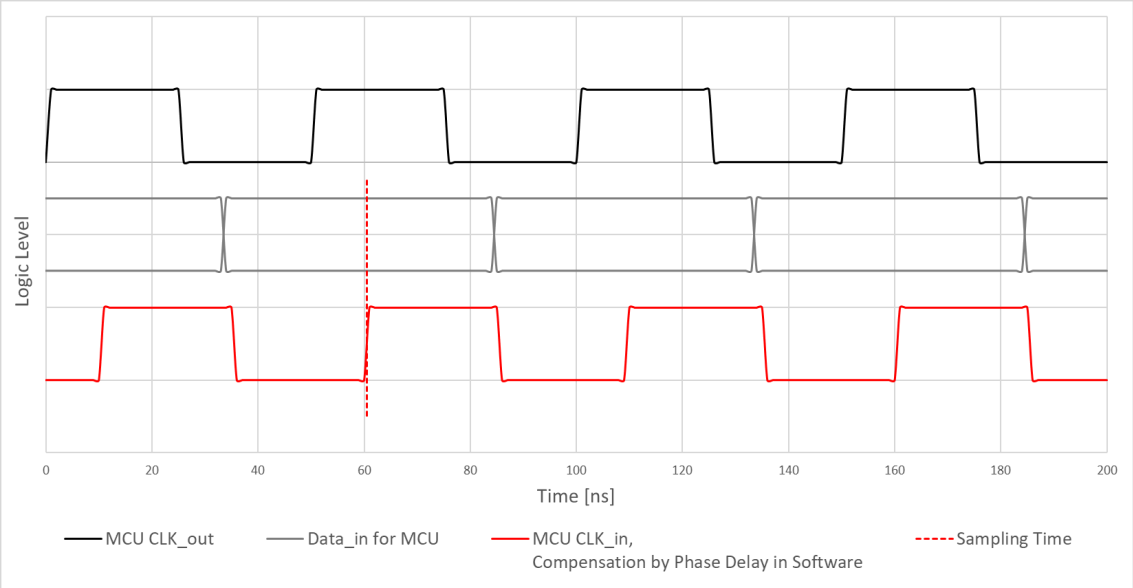


Figure 4-8. Timing Diagram C2000 Digital Interface to AMC1305L25 for Typical Specifications in the Data Sheet at 20-MHz Clock Frequency With Clock Edge Compensation With Software Configurable Phase Delay

The calculated setup and hold times including minimum and maximum values are shown in Table 4-4. As the phase delay is configurable in the software, the value of the phase delay can be selected such that the data acquisition timing is centered in the data signal. This allows the maximum possible margin to be available for setup and hold timing so that tolerances in the system do not affect the data acquisition. The calculation tool is providing the margin of the digital timing interface helping to understand the acceptable tolerances of the system. For a selected phase delay of 10 ns, the minimum setup time is 15.6 ns, resulting in a margin of 5.6 ns after subtracting the MCU setup time requirement of 10 ns. The margin for the minimum hold time is calculated accordingly and amounts to 6.7 ns.

Table 4-4. TMS320F28379D Digital Interface Timings With AMC1305L25 at 20-MHz Clock With Software Configurable Phase Delay

Phase Delay	Suggested Phase Delay		Selected Phase Delay
	min	4.4 ns	10.0 ns
	max	16.7 ns	
Min. Setup Time @MCU			15.6 ns
Max. Setup Time @MCU			33.3 ns
Min. Hold Time @MCU			16.7 ns
Max. Hold Time @MCU			34.4 ns

5 Conclusion

Clock edge delay compensation helps to meet setup and hold time requirements with isolated Delta-Sigma modulators and the MCUs digital interface without the necessity of reducing the modulator clock frequency. This allows the system to operate at full performance.

The clock edge delay compensation can be implemented by various methods these are compensation by:

- Additional Clock Signal with software configurable phase delay
- Clock Signal with hardware configurable phase delay
- Clock Return
- Clock Inversion at MCU

Compensation methods such as additional clock signal with software configurable phase delay and clock inversion at MCU were analyzed in more detail for the most common used isolated Delta-Sigma modulator variants and validated with AMC1306EVM evaluation module and C2000 TMS320F28379D Launchpad as well as Sitara AM243x Launchpad chosen as MCUs. The test results hold true for MCUs with CMOS interface and SDFM as well as for Sitara MCUs with no SDFM when working with PRU.

Table 5-1 shows the benefits and drawbacks of each clock signal compensation method. In the following the abbreviations SW Phase Delay and HW Phase Delay are used for compensation with software configurable phase delay and hardware configurable phase delay.

Table 5-1. Comparison of clock edge compedation methods

Method	Benefits	Drawbacks
SW Phase delay	• Compensation of any propagation delays • Allows the use of the maximum clock frequency enabling highest reliable communication • Implementation of precise phase delays • Change during run-time possible • No additional BoM cost	• One additional MCU GPIO and internal phase locked clock source is required • Additional MCU software
HW Phase delay	• No change of MCU software • No additional MCU GPIO is required	• Compensation dependent on implemented hardware delay hardware • Tolerance in the precision of phase delay by hardware components • No changes during run-time possible • Adds BoM cost
Clock Return	• No software and hardware efforts	• Does not work for all configurations • Adaptation of the layout • Longer clock signal more sensitive to transient noise

Table 5-1. Comparison of clock edge compedation methods (continued)

Method	Benefits	Drawbacks
Clock Inversion	• Simple implementation, if compensation by one half of the clock period solves the timing differences	• Does not work for all configurations • Fixed compensation by one half of the clock period only • MCU needs to be capable of inverting the clock signal at the GPIO input

Depending on the type of the Delta-Sigma Modulator, differentiated by external or internal clock source and CMOS or LVDS interface, different clock signal compensation methods can be better than others. Table 5-2 compares the suggested compensation methods for each type of Delta-Sigma modulator which are commonly used.

Table 5-2. Suggested clock edge compensation methods for modulators with internal or external clock

Method	AMC1306M25 external clock (CMOS)	AMC1305L25 external clock (LVDS)	AMC1303M2520/10 internal clock (CMOS)
Software Phase Delay	+	+	N/A
Hardware Phase Delay	o	o	o
Clock Return	o	-	N/A
Clock Inversion	o	o	+

For modulators which require an external clock, the clock signal compensation with software configurable phase delay offers the best performance, followed by the clock inversion at the MCU, if a fixed one-half of clock cycle meets the requirements. Both of these clock signal compensation methods help to meet the setup and hold timing requirements of the MCU especially at higher modulator clock frequencies. The following calculation tool can be used to validate the setup and hold timing requirements of the MCU when using the Delta-Sigma modulator AMC1306M25 and AMC1305L25.

6 References

- Texas Instruments, *Achieving Better Signal Integrity With Isolated Delta-Sigma Modulators in Motor Drives* application report
- Texas Instruments, High-performance isolated ADCs for high-voltage systems, overview
- Texas Instruments, *Comparing isolated amplifiers and isolated modulators* white paper
- Texas Instruments, *AMC1306x Small, High-Precision, Reinforced Isolated Delta-Sigma Modulators With High CMTI* data sheet
- Texas Instruments, *AMC1305x High-Precision, Reinforced Isolated Delta-Sigma Modulators* data sheet
- Texas Instruments, *AMC1303x Small, High-Precision, Reinforced Isolated Delta-Sigma Modulators With Internal Clock* data sheet
- Texas Instruments, *TMS320F2837xD Dual-Core Microcontrollers* data sheet
- Texas Instruments, *TMS320F2837xD Dual-Core Microcontrollers* technical reference manual
- Texas Instruments, *AM243x Sitara™ Microcontrollers* data sheet
- Texas Instruments, *MCU-PLUS-SDK-AM243X Software development kit (SDK)* tool

7 Revision History

Changes from Revision * (December 2023) to Revision A (January 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated calculation tool hyperlink	16

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265