

RNSEM-3P-RNS802 LTE and 5G O-RAN Small Cell Outdoor Radio Design Overview



Product Summary

The RNSEM-3P-RNS802 is a 5G NR and LTE small cell outdoor O-RU reference design. This platform is designed for seamless interfacing and evaluation of AFE77xxD with RANsemi's RNS802R for split 7.2 Radio Unit (O-RU) with low PHY functionality. This reference design solves essential design challenges to expedite development. The digital board contains TI's AFE77xxD RF transceiver with integrated Digital Pre-distortion (DPD), Crest Factor Reduction (CFR), and a single RNS802 chip, which is connected to a co-processor (TI Sitara™ AM64xx processor). This design includes baseline software architecture for 7.2x split, precision time protocol (PTP) stack and servo, PA biasing and protection, and VSWR. This can expedite time to market for a customer.

Overall Architecture

The different subsystem boards are designed and provided to achieve high performance, noise isolation, and thermal management.

- Digital board
 - Analog front end: [AFE7769D](#) (TI)
 - 5G small cell O-RU SoC: [RNS802R](#) (RANsemi)
 - Co-processor: [AM6412](#) (TI)
 - Clock synchronizer: [LMK5C33414A](#) (TI)
- High power RF front end board
 - Outdoor 5W small cell
 - Pre-amplifier: [LMH9135](#) (TI)
 - Pre-driver: [MAAM-011324](#) (Macom)
 - Power amplifier: [A5M36TG140](#) (NXP)
 - Power amplifier monitor and controller: [AFE10004](#) (TI)
- Cavity filter
 - Cavity filter with a frequency range of 3.4GHz to 3.6GHz
- Mechanical enclosure, heat sinks, and appropriate shielding

Key Features

- TI AFE7769D 4T4R integrated transceiver
- RANsemi RNS802R 5G small cell O-RU SoC
- TI Sitara AM6412 processor
- Synchronization and clocking on board through IEEE-1588 PTP with TI LMK5C33414A Network synchronizer
- RFFE tuned and designed for N78 TDD Duplex Mode (3.5GHz center frequency)
- RF board using NXP A5M36TG140 PA
 - Dual stage module designs integrating LDMOS integrated circuit as driver and GaN as a final stage amplifier.
- SFP+ connector for 25-G data transfer for front haul communication eCPRI

- Three UART serial interfaces which facilitate micro-USB port access, sync control for the GNSS receiver, and debug headers.

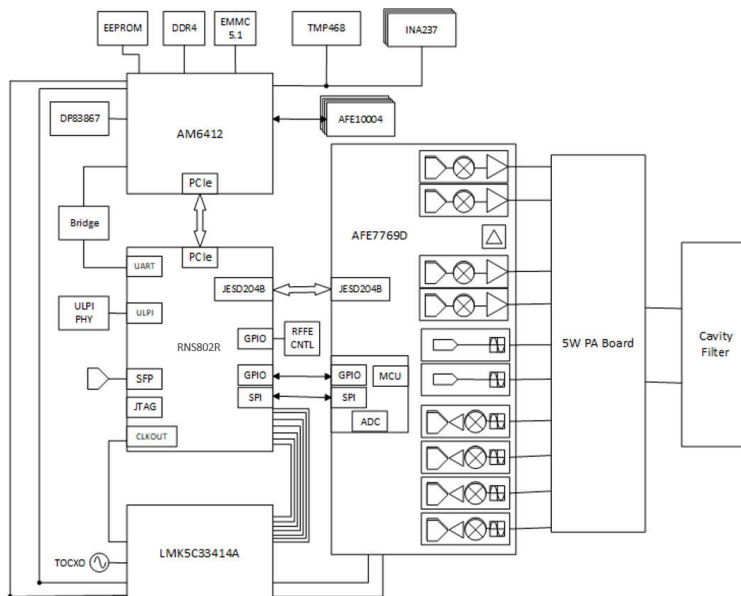


Figure 1. Reference Design Block Diagram

Related Documentation

Documentation	Description	Location
Reference design user's guide	Provides details supporting reference design including the use case, hardware and software setup, and pinout.	RANsemi Third-party page on ti.com
Schematic	Schematic files	Secure resources
Design layout	Layout files	Secure resources

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