Application Note

Improve SFDR Using Calibration in High-Speed ADCs

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ABSTRACT

In modern highly-integrated digital systems for data acquisition, high-speed analog-to-digital converters (ADCs) play a major role in transforming signals into their digital representation. As ADCs are a vital component of the overall system signal chain of wireless communications, electronic warfare, radar systems, medical imaging, and other applications, they must perform effectively to maintain a high spurious-free dynamic range (SFDR), establishing a distinguishable signal from noise. Therefore, ADC calibration is of utmost importance to improving SFDR by reducing noise and enhancing signal distinguishability. Specifically, calibration reduces errors, consequently allowing for SFDR improvement. This application note discusses different approaches for ADC calibration commonly found in most modern converters, including one-time calibration, background calibration, and foreground calibration.

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Trademarks

1 Introduction

High-speed ADCs play a crucial role in modern highly-integrated digital systems; however, these ADCs are prone to introducing a range of errors, which significantly impacts the accuracy of the sampled signal. Among these errors are gain errors, offset errors, and linearity deviations, which cause distortion of the obtained data. Fortunately, calibration can effectively minimize these errors and enhance the performance of the ADC, bringing it closer to the expected behavior.

Calibration has become an essential aspect of modern ADC designs, driven by the adoption of more advanced process nodes (such as 0.18 µm or smaller). These process nodes allow for additional digital feature integration within the ADC architecture. By introducing serial registers to enable or disable specific features, the concept of digital trimming emerged as a replacement for the traditional method of laser trimming the bias currents of a device for improved INL and linearity.

Reflecting on the past when laser trimming of internal ADC bias currents was the norm, the ADC performance of the ADC was fixed at the highest speed or sampling rate for which it was trimmed. Any deviation from this intended sample rate resulted in compromised performance. This limitation drove the push towards multiple speed grades of a device within an ADC device family, catering towards different sampling rate requirements.

As technology advanced further, reaching 65 nm and below, the space for digital features on a data converter has grown significantly, enabling the incorporation of more digital components and features. This expansion opens up new possibilities for real-time calibration and allows for dynamic trimming of the ADC.

Real-time calibration has become the standard approach for linearizing ADC performance at various sample rates and input frequencies. These calibration methods act to provide flexibility to system designers, allowing for a tailored ADC performance in their specific application. By providing a seemingly unlimited amount of flexibility, calibration enables the system designer to achieve optimal performance regardless of the variation in sampling rate or input frequency (a significant advancement over laser trimming). As a result, the same ADC delivers excellent performance across many different applications, enabling reconfigurable systems.

2 Achieving Accuracy Through Calibration

Several factors can contribute to the degradation or loss of calibration in a high-speed ADC. These factors can affect the accuracy and performance target of the ADC, leading to a point where re-calibration is necessary. The following section discuss some common factors that can cause a high-speed ADC to become uncalibrated.

2.1 Temperature Variations

Temperature variations can affect the internal circuitry of the ADC reducing its performance, necessitating a re-calibration to maintain accuracy. Figure 2-1 below compares the signal-to-noise ratio (SNR) and SFDR versus temperature in different calibration modes. The FG25 trace acts as a baseline and represents performance if the ADC12DJ5200RF is calibrated only at 25 °C. All other traces are calibrated at each recorded temperature proving various calibration methods as effective.

Additionally, these changes in ambient and or board temperature can alter the electrical characteristics of front-end components, resulting in an unexpected ADC input impedance and likely degradation of second or third-order harmonics (HD2 and HD3).

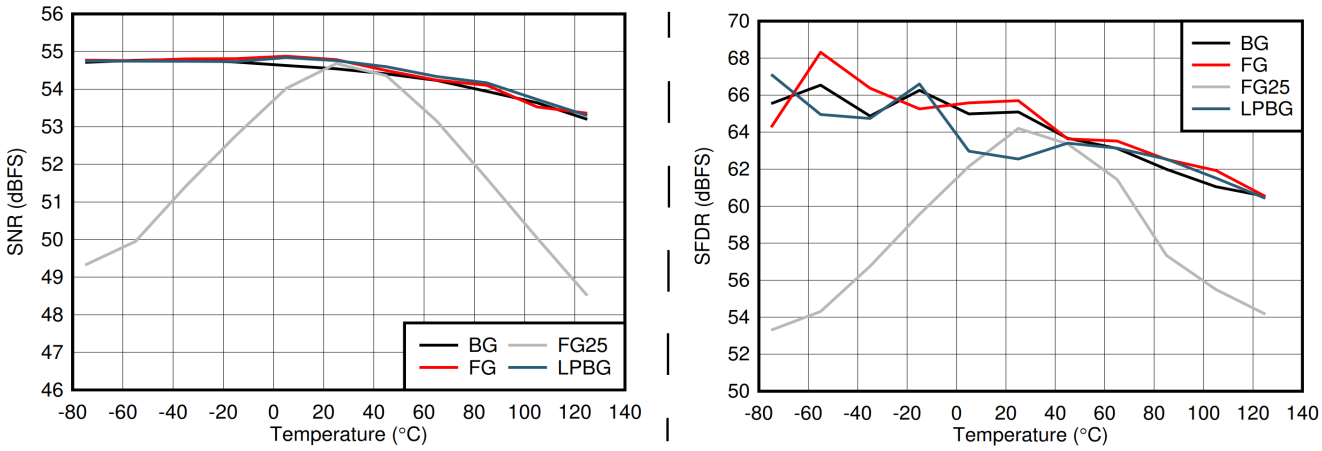

Figure 2-1. ADC12DJ5200RF Performance Versus Temperature in Different Calibration Modes

2.2 External Noise

External factors, such as electromagnetic interference (EMI), noise, and power supply fluctuations, can degrade the performance of the ADC and ADC calibration. Electrical noise sources, including powerful radio frequency (RF) signals or power supply noise, can introduce errors and degrade the performance of the ADC, requiring a re-calibration to restore optimal and accurate measurements.

2.3 Unstable Power Supply

Exceeding the maximum voltage or current limits specified by the ADC data sheet can lead to non-ideal behavior, significant performance degradation, or even device failure. Operating the ADC beyond the recommended range can result in the gain and or offset errors significantly degrading SFDR. In such an event, upon the return of normal power conditions, a re-calibration can make sure that accurate measurements return, however, reprogramming of the device can be required to guarantee system performance.

2.4 Mechanical Stress

Mechanical stress or vibration can impact the stability of the internal wire bonds of the ADC, causing calibration drift. When under physical stress, the temperature characteristics of the ADC or package can behave in unexpected ways, thus a frequent calibration is recommended. Additionally, mechanical stresses on front-end components can alter electrical characteristics, resulting in degradation of the matching network. As a result, any physical shocks, stresses, or vibrations can require a re-calibration before the ADC performance resumes as expected.

2.5 Manufacturing Variations

Variations in the manufacturing process is not abnormal, and results in inconsistencies between different individual ADCs. As each die on a wafer is uniquely fabricated, the performance between two ADCs is never exactly the same, only behaving similarly. Some examples where this shows across devices is in gain error, linearity behavior, and reference voltage drift. Each ADC can have slightly different package or manufacturing parasitics as well, all of which are resolved through calibration.

2.6 Avoiding Errors

Proper design, layout, shielding, and environment control measures help to minimize the impact of these factors and maintain the calibration of a high-speed ADC for a longer period of time. By implementing robust design measures, such as proper grounding, shielding techniques, and thermal management, the adverse effects of temperature variations, external factors, and mechanical stress or vibration can be mitigated. These measures help ensure the long-term accuracy and performance of high-speed ADCs, optimizing their functionality within digital systems and reducing the need for frequent re-calibration.

3 Calibration Techniques

3.1 One-Time Calibration

The process of one-time calibration involves performing calibration only once during the initial bring-up sequence of the data converter. In the specific case of the ADC32RF55, a dual-channel, 14-bit, 3 GSPS RF-sampling ADC, the initial bring-up sequence is performed to calibrate all of the internal sub-ADC cores, allowing for data sheet performance to be realized. Without performing this one-time calibration, the converter is severely degraded and there is no worthwhile data to be processed as shown in Figure 3-1. However, after this one-time calibration, the FFT is as expected as shown in Figure 3-2.

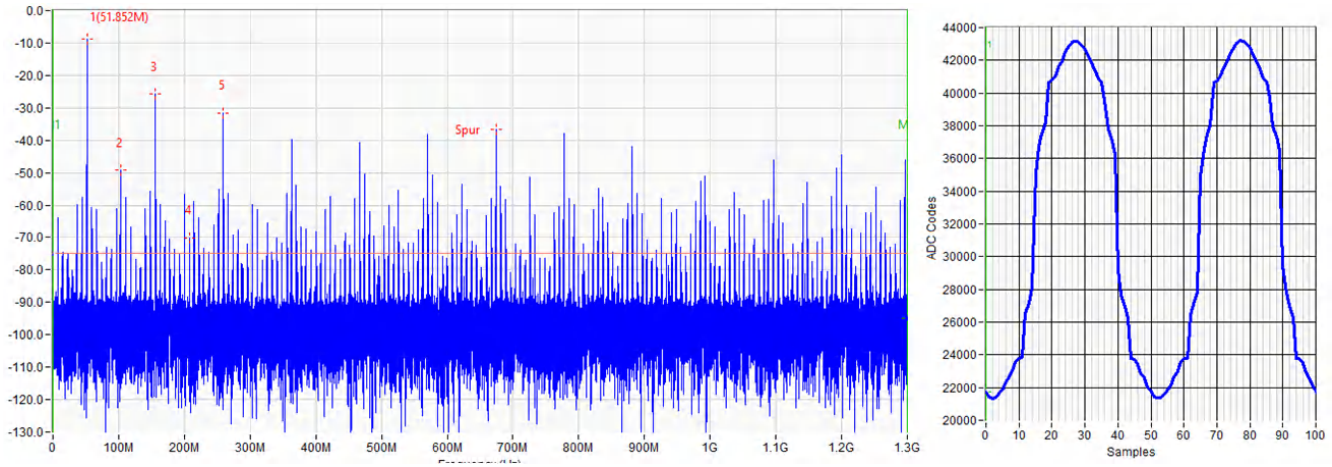

Figure 3-1. ADC32RF55 Output Without One-time Calibration

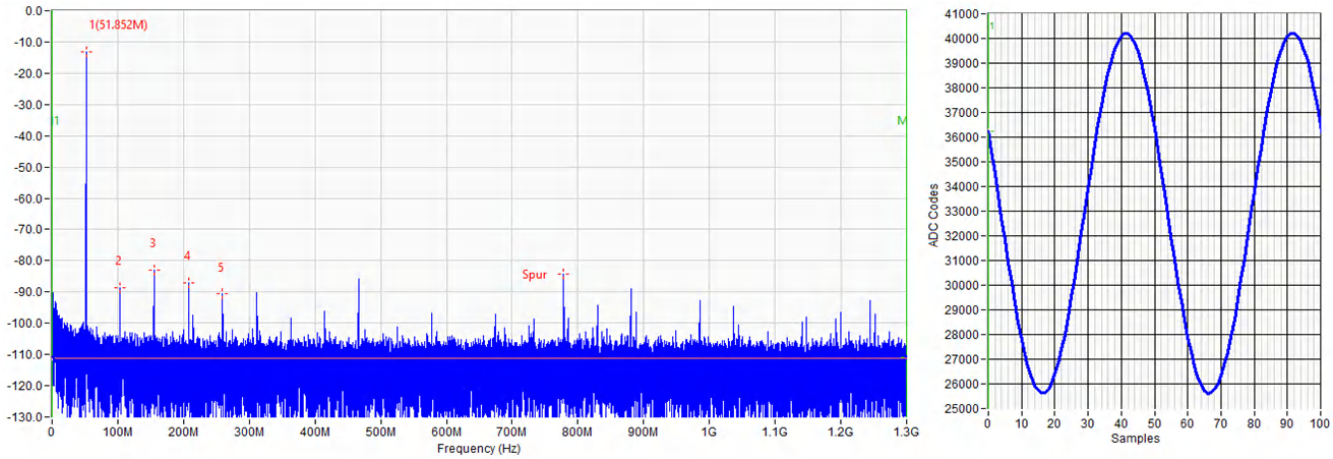

Figure 3-2. ADC32RF55 Output With One-time Calibration

Similarly, the ADC12DJ5200RF, a dual-channel, 12-bit, 5.2GSPS RF-sampling ADC, also requires a one-time calibration such, that the gain and the offset of the sub-ADC cores are matched, thereby reducing interleaving spurs and improving SFDR. One-time calibration is performed by the serial peripheral interface (SPI) during the initial programming of both the ADC32RF55 and the ADC12DJ5200RF devices.

3.2 Foreground Calibration

Foreground calibration, also known as real-time calibration, resembles that of the one-time calibration in Section 3.1, however instead of taking place before valid data is transmitted, foreground calibration occurs while the device is actively sending data. The resulting data at the downstream processor or FPGA can appear distorted during calibration and does not always resemble the input signal. Foreground calibration requires that the downstream processor or FPGA determine when a calibration is required by monitoring performance of the converter in real-time. In the case of foreground calibration for the ADC32RF55, additional ADC cores (the

specific number of additional cores is mode dependent) are continuously calibrated behind the scenes and the moment foreground calibration takes place, the uncalibrated ADC core is swapped out with one of the calibrated ADC cores. As a result, a single sample can be dropped as shown in Figure 3-3. Foreground calibration can often be triggered using the SPI interface or through a general purpose hardware input (GPIO).

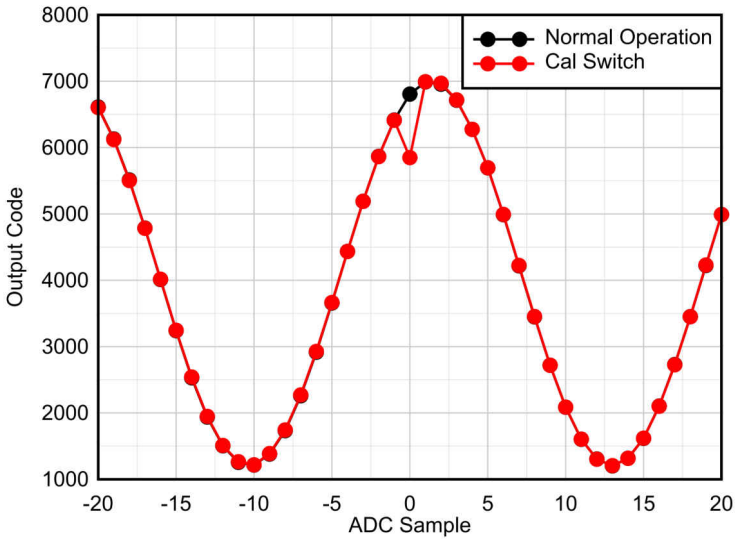

Figure 3-3. ADC32RF55 Output Codes During Foreground Calibration

3.3 Background Calibration

Background calibration is a continuous process taking place during the operation of the ADC. Background calibration involves the continual use of an out-of-calibration spare ADC core. Once this spare ADC core is calibrated, the ADC core is swapped with (one of) the active ADC cores. As a result, background calibration maintains the accuracy of the ADC across various environments, such as rapidly changing temperatures, in real-time. However, background calibration consumes more power than other calibration modes since the spare ADC core is always powered on and undergoing a continuous swapping with an active ADC core.

In the case of the ADC32RF55, the background calibration function is referred to as continuous calibration in the data sheet. During the continuous calibration, one of the five internal ADC cores (per channel) is swapped out approximately every 27 ms, equating to approximately every 81 million samples if the device is operating at 3 GSPS. Figure 3-4 shows a comparison of the internal ADC core swap during foreground calibration (the first two GPIO1 pulses indicate two separate foreground calibrations) versus how the ADC cores swap during a continuous calibration (the longer GPIO1 pulse is used to represent a continuous calibration).

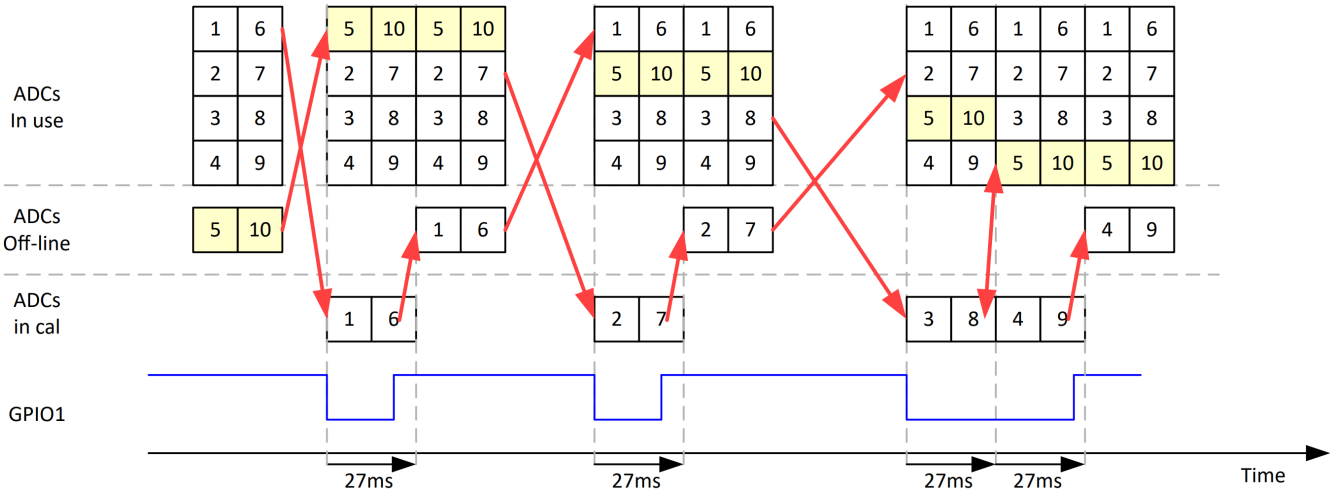

Figure 3-4. ADC32RF55 Core Swap During Background Calibration

Background calibration must be configured using SPI by a register field. Some devices, such as the ADC12DJ5200RF support a low-power background calibration (LPBG) mode (as shown previously in Figure 2-1) reducing the overall power used during background calibration, but can increase the transient requirements of the device power supply. In the instance of the ADC32RF55, a GPIO can be configured to temporarily freeze the background calibration, reducing power dissipation during periods of low activity.

4 Summary

High-speed ADCs are essential components in modern digital systems, but ADC accuracy can be compromised by various errors. Calibration, which addresses gain, offset, linearity, and spurious components such as HD2 and HD3, plays a crucial role in improving the spurious-free dynamic range or SFDR of the ADC. Achieving a high SFDR is particularly important in systems operating at lower transmit powers or over longer distances, as a high SPDR helps distinguish desired signals from unwanted spurious components. Internal ADC calibration schemes have emerged as effective solutions to minimize these errors and enhance ADC performance. However, factors like temperature variations, power supply fluctuations, and IC process shifts can degrade or compromise calibration. One-time calibration establishes a solid starting point, while foreground and background calibrations maintain accuracy in the presence of varying environmental conditions. System designers must understand and implement the appropriate calibration technique to reduce harmonic distortion, improve SFDR, and achieve accurate measurements with high-speed ADCs in future designs.

5 References

- Texas Instruments, *ADC32RF5x Dual Channel 14-bit 2.6 to 3-GSPS RF Sampling Data Converter,* data sheet.
- Texas Instruments, *ADC12DJ5200RF 10.4-GSPS Single-Channel or 5.2-GSPS Dual-Channel, 12-bit, RF-Sampling Analog-to-Digital Converter (ADC)* , data sheet.

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