Application Brief

High-Speed Data Interface for Precision High-Speed ADC in Semiconductor Test

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Introduction

In semiconductor test systems, a faster sampling rate ADC (Analog-to-Digital Converter) can provide several benefits, including:

1. *Reduced noise*: Faster sampling rates can reduce noise in the signal, as the ADC can capture more samples of the signal, and the ADC can average the signals to reduce noise.
2. *Better detection of transient events*: Transient events in a signal, such as spikes or glitches, can occur for a very short time and be missed by slower ADCs. With a wide-bandwidth and faster sampling rate ADC, these events can be captured more accurately, providing a better understanding of the signal's characteristics.
3. *Improved testing speed*: Faster sampling rate ADCs can also enable faster testing speeds, as the ADC can acquire and process more data per unit time.
4. *Compatibility with high-speed devices*: Faster and more complex devices generate signals with higher bandwidths. To accurately capture and test these signals, faster sampling rate ADCs are required.
5. *Flexibility in testing multiple signals*: With faster sampling rate ADCs, multiple signals can be tested at once, as the ADC can rapidly switch between signals to capture data.

All of these benefits of a high-speed ADC can help improve the accuracy and efficiency of testing electronic devices. A high-speed ADC requires a high-speed data interface with the controller of the system for transmission of digital data. This application note describes a source-synchronous data interface for high-speed data transmission from ADC to controller in semiconductor test systems.

Source-Synchronous Data Interface

The ADS9817 is an eight-channel data acquisition (DAQ) system based on a dual, simultaneous-sampling, 18-bit successive approximation register (SAR) analog-to-digital converter (ADC). The ADS981x supports 2 MSPS/channel sampling rate at every analog input channel. A high-speed digital interface supporting 1.2-V to 1.8-V operation enables the ADS9817 to be used with a variety of host controllers. Refer to *Precision ADC for Measuring Analog Outputs of Parametric Measurement Unit (PMU)* on precision ADC for measuring the analog outputs of parametric measurement unit (PMU) in semiconductor test.

The clock speed for 20-bit data transfer using single-edge of data clock is given by Equation 1.

$$\text{Data clock speed} = \frac{2\ \text{MSPS/channel} \times 8\ \text{channels} \times 20\ \text{bits/sample}}{4\ \text{serial outputs}} \quad (1)$$

$$\text{Data clock speed} = 80\text{MHz} \quad (2)$$

The ADS9817 data sheet features a source-synchronous data interface to enable high-speed ADC interface. A source-synchronous interface is a type of interface where the data is output by the ADC synchronously with a dedicated clock signal that is transmitted along with the data. This process is in contrast to a regular serial peripheral interface (SPI), where the data is transmitted asynchronously with respect to the clock signal. The following are some advantages of source-synchronous interface over regular SPI:

1. *Improved timing*: Source-synchronous interface helps to mitigate timing issues, such as skew and jitter, that can cause timing violations in asynchronous interfaces like SPI. The dedicated clock output signal in a source-synchronous interface synchronizes the data and arrives at the receiver at the correct time.

2. *Higher data rates*: Source-synchronous interfaces can support higher data rates than regular SPI. This outcome is because synchronous interfaces can transmit data along with the clock signal, whereas SPI transmits data one bit at a time. This outcome can be particularly advantageous in high-speed communication applications.
3. *Easier PCB Layout*: Source-synchronous interface is generally easier to lay out on a printed circuit board (PCB) than regular SPI. This outcome is because the timing requirements are less stringent, and there are fewer interconnects to manage.
4. *Easier Interface with FPGA*: FPGA logic can use logic primitives like flip-flop to capture the source-synchronous data with clock. In regular SPI, the FPGA captures ADC output data with a clock locally generated by the FPGA that can result in reduced timing margin.

Figure 1 shows the delays associated with regular SPI that adversely impact timing margin. The serial interface clock is generated by the FPGA that propagates along the transmission distance with delay (t_{P_D}). The clock is further delayed by the input buffer (t_{IP_D}). The ADC responds with data that is delayed by the output buffer (t_{OP_D}) and the same transmission distance (t_{P_D}) before being received by the FPGA. Hence the ADC output data received by the FPGA is considerably delayed with respect to the SPI clock generated by the FPGA. This delay reduces the timing margin available to the FPGA to capture ADC data.

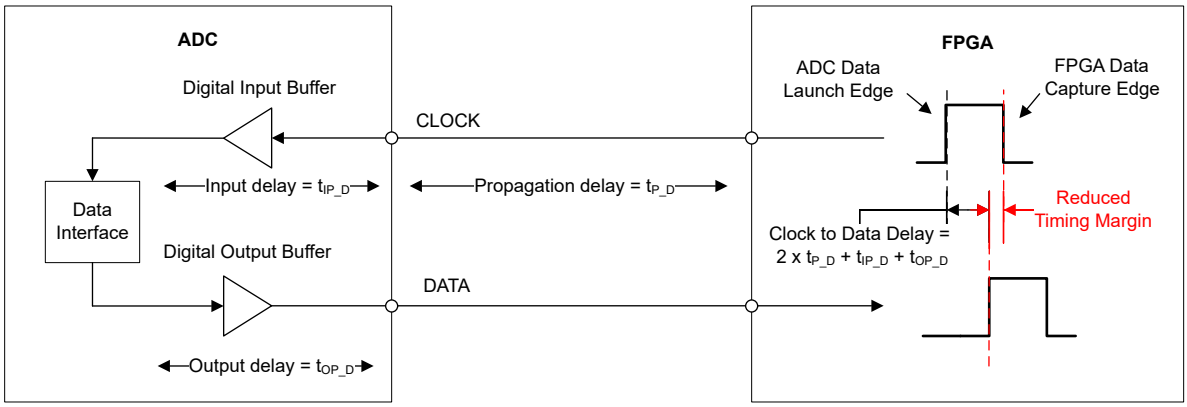

Figure 1. Timing Margin in Regular SPI

The ADS9817 generates the output data and data-clock as shown in Figure 2. There is no clock-to-data delay as both data and data-clock are generated by the ADC. Overall, source synchronous interface can offer improved performance and simpler design compared to regular SPI.

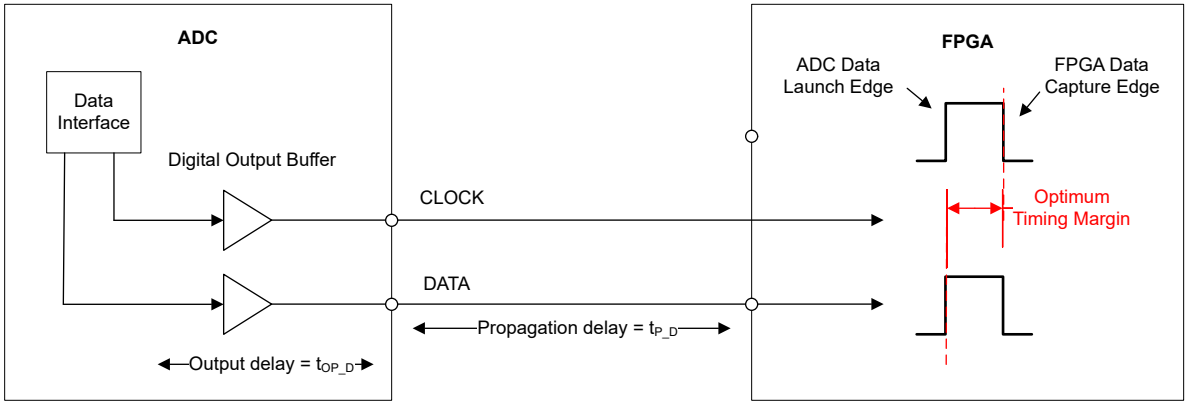

Figure 2. Timing Margin in Source Synchronous Serial Interface

Minimizing Impact of Data Communication on ADC Performance

The interference of ADC data interface on analog performance can be a significant challenge in mixed-signal designs. Interference between ADC data interface and circuits can result in errors, noise, and other undesirable effects in the converted digital data. The following are some ways in which the ADC data interface can affect analog performance:

1. *Ground bounce*: The ground connection in the ADC data interface can create ground loop currents, which can introduce noise and affect the analog performance.
2. *Electromagnetic interference*: The ADC data interface can generate electromagnetic interference (EMI), which can be coupled into the analog circuitry and cause noise or other performance issues. EMI can arise from a variety of sources, including clock signals, data lines, power supply lines, and ground connections.
3. *Crosstalk*: Crosstalk can occur when signals on one channel interfere with signals on another channel. This process can be particularly problematic when the ADC data interface is placed in close proximity to the analog circuitry.
4. *Power supply noise*: The power supply for the ADC can generate noise, which can be coupled into the analog circuitry and cause performance issues.

To mitigate the interference of ADC data interface on analog performance, the ADS9817 features separate IOVDD and IOGND pins for proper grounding and shielding of the data interface for layout optimization. Carefully choose the placement and routing of the ADC data interface in relation to the analog circuitry.

The ADS9817 also features a bit scrambling feature that decorrelates the ground loop current of the data interface from the analog circuits. When the bit-scrambling feature is enabled, the ADC conversion result is bit-wise XOR with the least significant bit (LSB) of the conversion result as shown in Figure 3. The LSB of the ADC conversion result has equal probability of being either 1 or 0 because of thermal noise. Hence the randomized result after the XOR operation is uncorrelated with the input voltage of the ADC. The ground bounce created by the transmission of this randomized result over the data interface is uncorrelated with the analog input voltage.

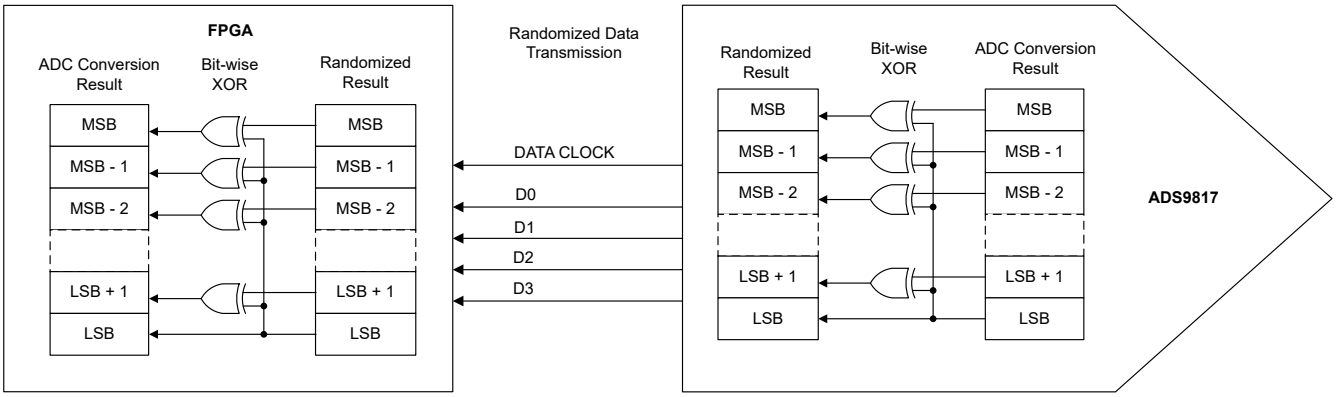

Figure 3. Bit Scrambling to Reduce Interference Between Data Interference and Analog Performance

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