Application Note

Implementing the External DC Offset Correction Block in the ADS54J60

Amy Weatherby

ABSTRACT

Interleaving is a powerful technique in which multiple analog-to-digital converters (ADC) are cascaded together to greatly increase the sampling rate of the converter. However, implementing an interleaving architecture comes at the expense of undesired spectral spurs. These spurs arise from gain, offset, timing and bandwidth mismatches between the individual converters. The ADS54J60 contains four interleaved ADC cores that each produce different spur offsets. Environmental temperature variations cause even larger differences in the spur offset values. This application note demonstrates how to implement the external offset correction block to maintain the amplitude of the interleaving spurs over temperature changes.

Table of Contents

1 Introduction 2
2 Interleaving Architecture 2
3 DC Offset Correction 3
3.1 DC Offset Correction Architecture 3
3.2 Freezing the DC Offset Correction 3
3.3 Effect of Environmental Temperature Fluctuations 4
3.4 Effect of Input Frequency on Interleaving Spur 4
4 External Offset Correction 5
5 Configuring External DC Offset Correction (Channel A) 5
5.1 Device Default Configuration 5
5.2 Baseline HSDC Pro Capture 6
5.3 Freezing the Interleaving Engine and DC Offset Values 6
5.4 Reading the Frozen DC Offset Values 7
5.5 Loading the DC Offset Values 7
5.6 Confirm HSDC Pro Capture 8
6 Summary 9
7 References 10
8 Revision History 11

List of Figures

Figure 2-1. Functional Block Diagram 2
Figure 3-1. DC Offset Corrector Architecture (one ADC Core) 3
Figure 3-2. Interleaving Spur vs. Temperature 4
Figure 3-3. Interleaving Spur vs. Input Frequency 4
Figure 5-1. Load Configuration Files 5
Figure 5-2. Baseline Capture (Default Offset Correction) 6
Figure 5-3. ADS54J60 GUI Register R/W Feature 7
Figure 5-4. Modified Configuration File with Values 7
Figure 5-5. External Offset Correction 8

List of Tables

Table 5-1. Recorded Frozen DC Offset Values 7

Trademarks

1 Introduction

The ADS54J60 is a dual channel device. Each channel contains four interleaved ADC cores that each produce different DC offset values. These differing ADC core offsets are the source of the interleaving spurs appearing at DC, $f_s/4$, and $f_s/2$ in the spectrum. A DC offset correction feature was created to reduce the amplitude of these interleaving spurs. Environmental temperature variations produce larger discrepancies in the DC offset values between the interleaved cores. The external DC offset correction was developed to calibrate the interleaving spurs over temperature changes, and the process to implement this option is detailed in Section 5.

2 Interleaving Architecture

Figure 2-1 highlights the area of interest within the part containing the DC offset correction feature. The four internal interleaved ADC cores in each channel can sample up to 250 MSPS, resulting into an output data stream of up to 1 GSPS (or Nyquist bandwidth of 500 MHz).

The amplifier in the first pipeline stage increases the DC offset mismatch between the cores and generates higher interleaving spurs. The spur at DC arises due to the average offset of the four cores. To reduce the mismatch between cores, each interleaved ADC core has an individual DC offset correction block that aims to bring the core offset to a mid-code value. The corrected data from each core is then combined into the interleaving engine block.

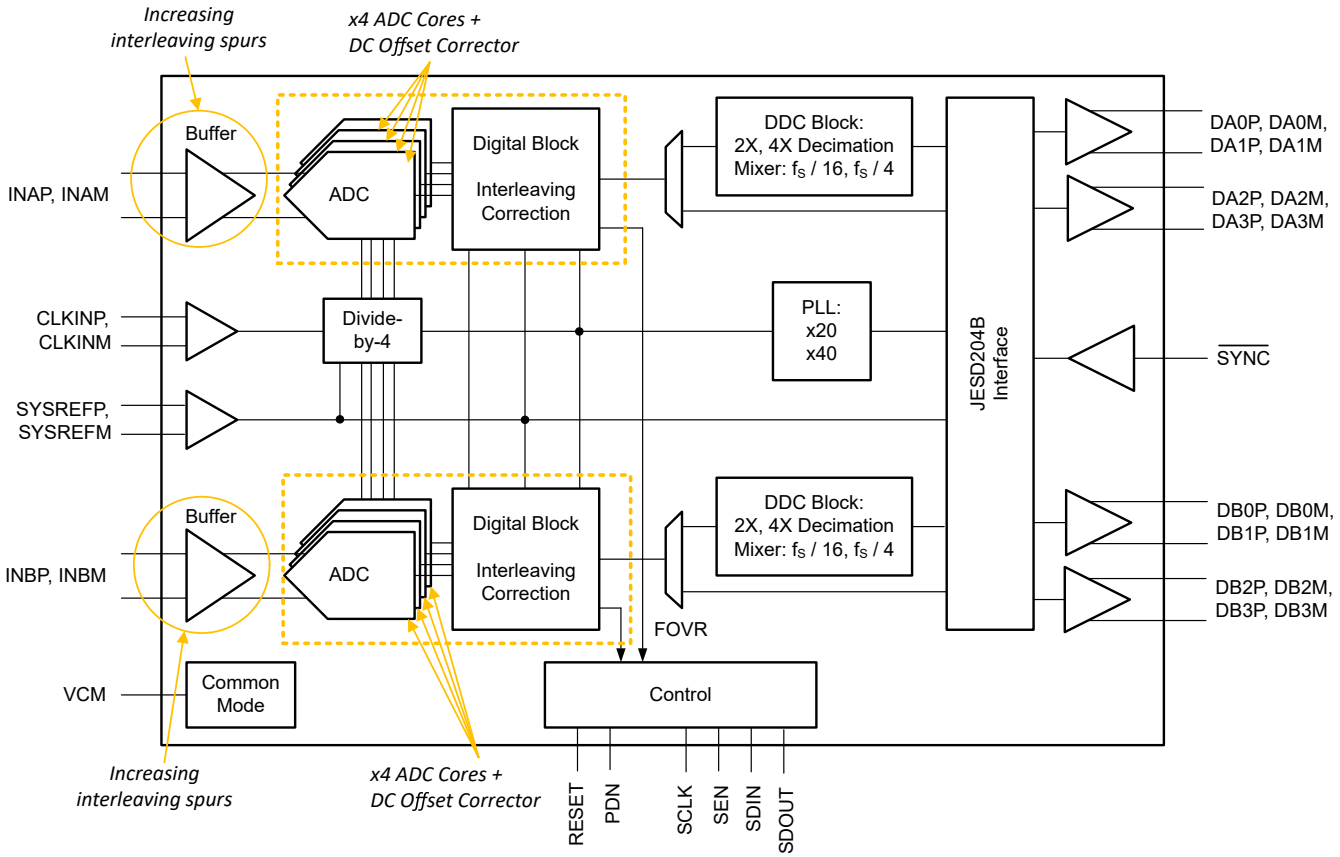

Figure 2-1. Functional Block Diagram

3 DC Offset Correction

3.1 DC Offset Correction Architecture

3.1.1 Default Configuration

The DC offset correction block is enabled by default. In this state, the corrector continuously estimates and subtracts the average from the data stream. This block acts as a high-pass filter that removes the DC content of the incoming data stream prior to combining the interleaved data. While this feature reduces the interleaving spurs to the best-case performance, these spurs are not entirely eliminated in the spectrum.

3.1.2 Bypassing the DC Offset Correction

The DC offset corrector cannot distinguish the external DC signal from internal DC offset for applications that use an amplifier driver to dc-couple to the ADC. This feature, shown in Figure 3-1, can be bypassed through SPI. Bypassing results in a histogram with multi-modal output codes and interleaving spurs as large as -40 dBFS in the spectrum at DC, $f_s/4$, and $f_s/2$.

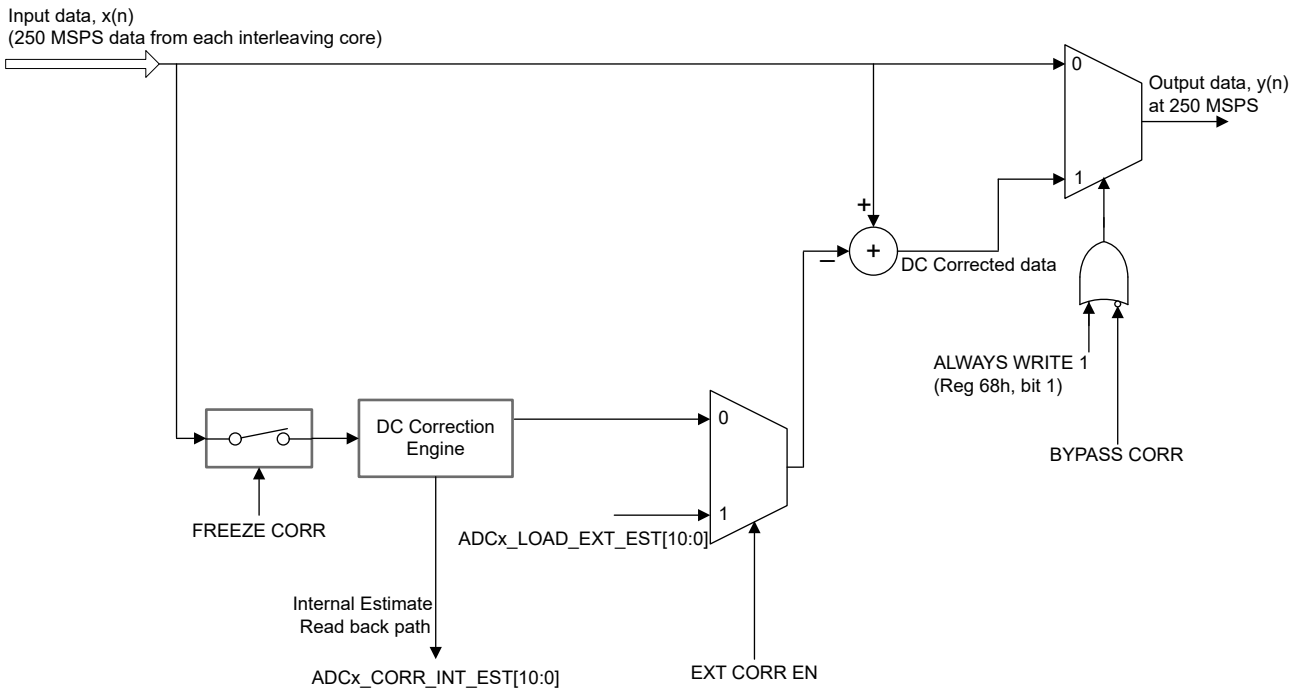

Figure 3-1. DC Offset Corrector Architecture (one ADC Core)

3.2 Freezing the DC Offset Correction

When the DC offset corrector is frozen, the DC offset holds the last estimated value obtained from each ADC core. While new estimates are not captured, the frozen average continues to be subtracted from the data stream.

3.3 Effect of Environmental Temperature Fluctuations

Under environmental temperature changes, there is greater variability in the DC offsets between the four interleaving cores. The DC offset correction block is not stable over temperature variations, and the $f_s/4$ and $f_s/2$ spurs will increase without another correction method. The external offset correction option was created to address this.

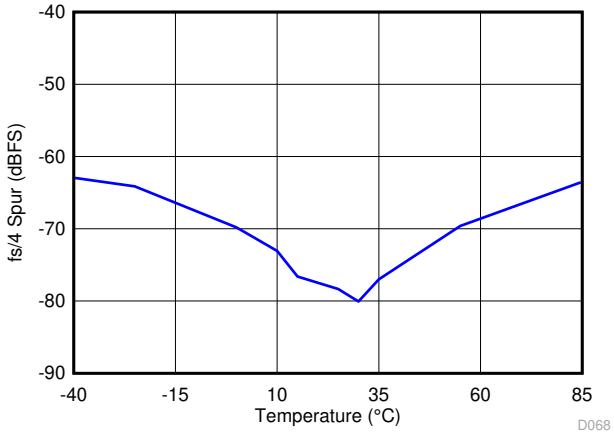

Figure 3-2. Interleaving Spur vs. Temperature

3.4 Effect of Input Frequency on Interleaving Spur

Note that the interleaving spur is frequency dependent. In general, the spurs increase in amplitude as the input frequency is increased. The example provided in Section 5 was performed with no input tone.

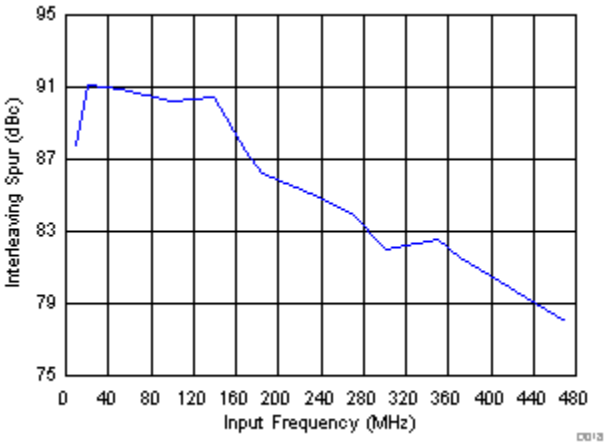

Figure 3-3. Interleaving Spur vs. Input Frequency

4 External Offset Correction

The external offset correction feature is an option for system applications that cannot tolerate large variations in the DC, $f_s/4$, and $f_s/2$ interleaving spurs over environmental temperature variations. The internal DC offset can be frozen, read, and loaded externally to calibrate the DC offset over temperature to maintain (but not further improve) the amplitude of the spurs to the levels seen in Figure 3-2 and Figure 3-3.

Section 5 details the required SPI register writes to correctly implement this option. Four configuration files have been created with the writes to further simplify the process.

5 Configuring External DC Offset Correction (Channel A)

The following section describes the process to calibrate the internal DC offset mismatch by utilizing the external DC offset correction feature. The offset correction values are 11-bit signed values estimated by the engine. Each register holds 8-bit values, so two registers are used to obtain the full 11-bit offset correction value.

5.1 Device Default Configuration

Per the ADS54J60 user guide, install and launch the ADS54JXX GUI. Load the default configuration files to program the LMK (onboard clocking chip) and the ADC.

1. Load LMK_Config_Onboard_983p04_MSPS.cfg
2. Perform a hard reset the ADC, using the onboard pushdown
3. Load ADS54J60_LMF_8224.cfg
   a. Can load any other desired ADC configuration file, depending on the desired mode of operation

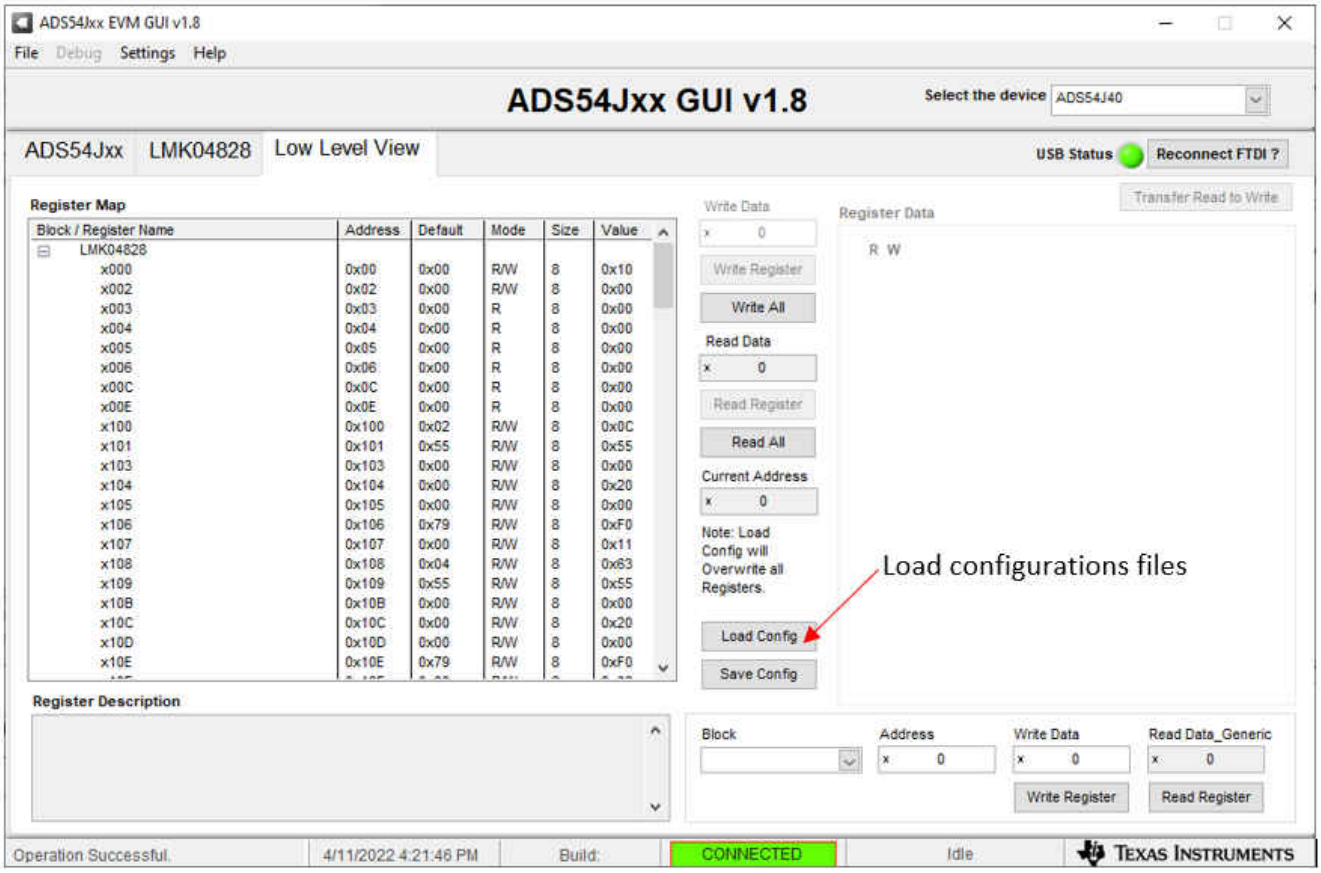

Figure 5-1. Load Configuration Files

5.2 Baseline HSDC Pro Capture

By default, the DC offset correction block is enabled. This results in reduced interleaving spurs with amplitudes visible above the noise floor.

- Download the correct firmware to the TSW14J56 capture card (in this example, select ADS54J60_LMF_8224)
- Take a capture of the noise floor
- Confirm that the interleaving spurs are in the range of -90 to -85 dBFS

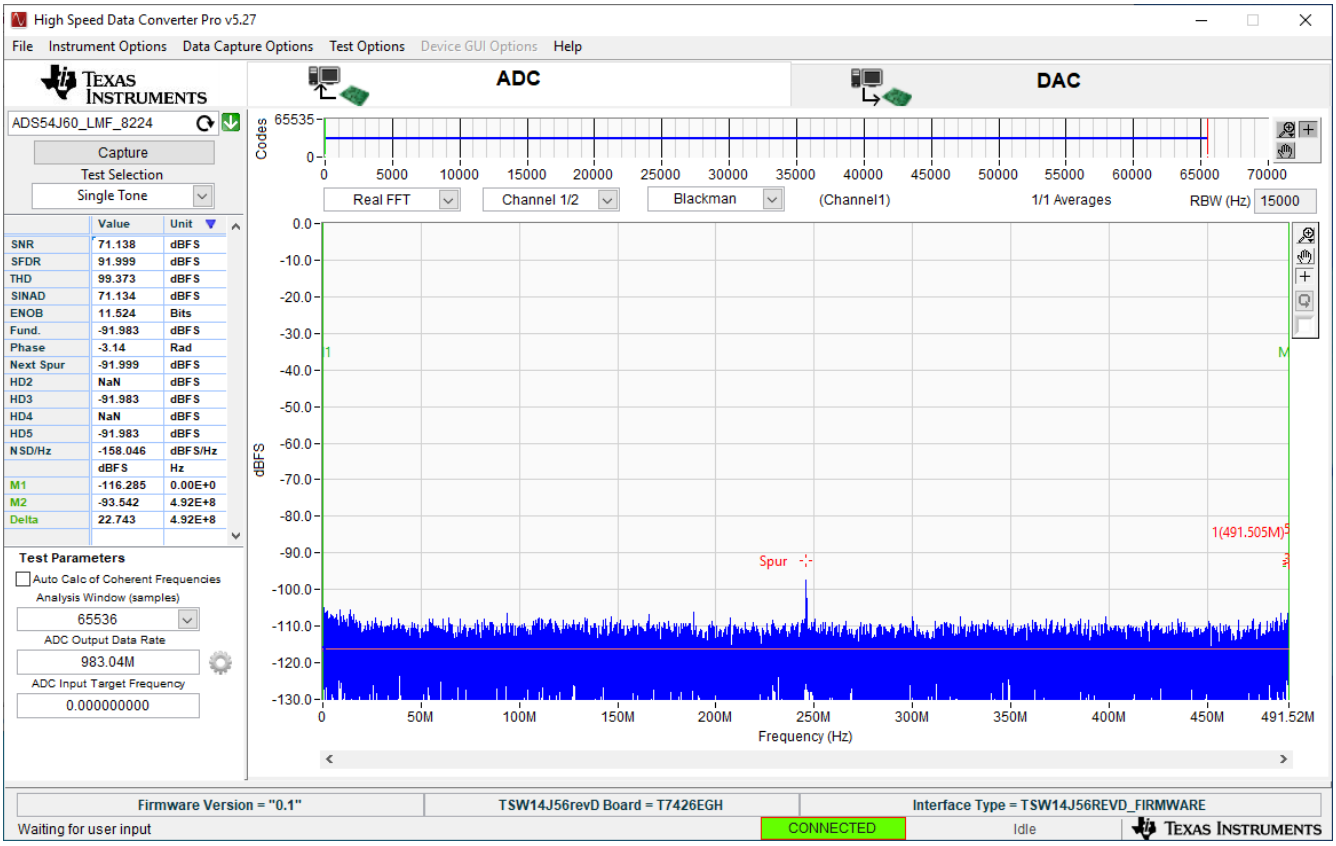

Figure 5-2. Baseline Capture (Default Offset Correction)

5.3 Freezing the Interleaving Engine and DC Offset Values

The required low-level register writes to freeze and read the DC offset values are compiled into the following files. These three configuration files address the required 500 ms delay after setting the DC calibration bandwidth, freezing the interleaving calibration engine, and freezing the DC correction value.

1. **DC Calibration Bandwidth**: DC_IL_Freeze1.cfg
   a. Sets the DC calibration bandwidth for both channels to 5 (or 9 Hz)
   b. This increases the accuracy of the estimated DC offset value
2. **Freeze Interleaving Engine**: DC_IL_Freeze2.cfg
   a. Enables the interleaving block freeze/unfreeze option
   b. Freezes the interleaving calibration engine
3. **Freeze DC Offset Correction Block**: DC_IL_Freeze3.cfg
   a. Freezes DC offset correction block for both channels
   b. Enables a single channel register write (reads the values from each individual channel; otherwise, the frozen values will be incorrectly read back)

5.4 Reading the Frozen DC Offset Values

The DC offset correction values are setup to be read and recorded. Using the ADS54JXX GUI, navigate to the 'Low Level View' tab. Select the ADS54Jxx_LowLevel block. The 11-bit DC offset correction values can be read and recorded from addresses 0xE074 through 0xE07B for Channel A, and from 0xF074 through 0xF07B for Channel B.

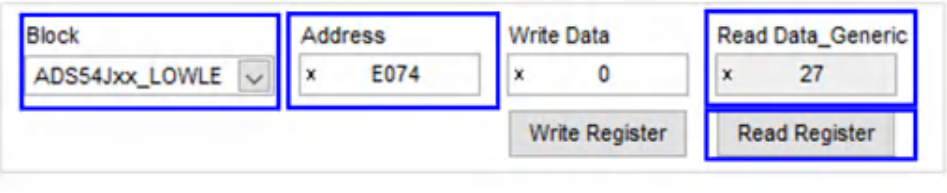

Figure 5-3. ADS54J60 GUI Register R/W Feature

Table 5-1. Recorded Frozen DC Offset Values

Address (CHA)	DC Offset Correction Value (this example)	Address (CHB)	DC Offset Correction Value
0xE074	0x27	0xF074	*(value)*
0xE075	0x07	0xF075	*(value)*
0xE076	0x3A	0xF076	*(value)*
0xE077	0x07	0xF077	*(value)*
0xE078	0xCC	0xF078	*(value)*
0xE079	0x00	0xF079	*(value)*
0xE07A	0xCC	0xF07A	*(value)*
0xE07B	0x00	0xF07B	*(value)*

5.5 Loading the DC Offset Values

The fourth configuration file contains the register writes to load the DC offsets values externally. This file requires user modifications to load the values recorded read at the address in the previous section.

1. Modify the DC Offset Values
   a. Open the pre-load_write.cfg file
   b. Modify the file with the values recorded from the addresses in Table 5-1

```
ADS54Jxx_LOWLEVEL
0x6069 0x01 // Enable external offset correction
0x4005 0x01 // Enable single Ch reg write
0x4004 0x61 // Page select
0x4003 0x00 // ...
0x4002 0x05 // ...
0x4001 0x00 // ...
0x6000 0x27
0x6001 0x07
0x6004 0x3A
0x6005 0x07
0x6008 0xCC
0x6009 0x00
0x600C 0xCC
0x600D 0x00
```

Figure 5-4. Modified Configuration File with Values

2. Load DC Offset Values: pre-load_write.cfg (load into the GUI)
   a. Enables the external offset correction load option
   b. Sets the correct page to load the offset correction values externally
   c. Contains the modified values from Figure 5-4.

5.6 Confirm HSDC Pro Capture

Take another capture in HSDC Pro. The spur should remain unchanged if the values were correctly frozen, read, and loaded.

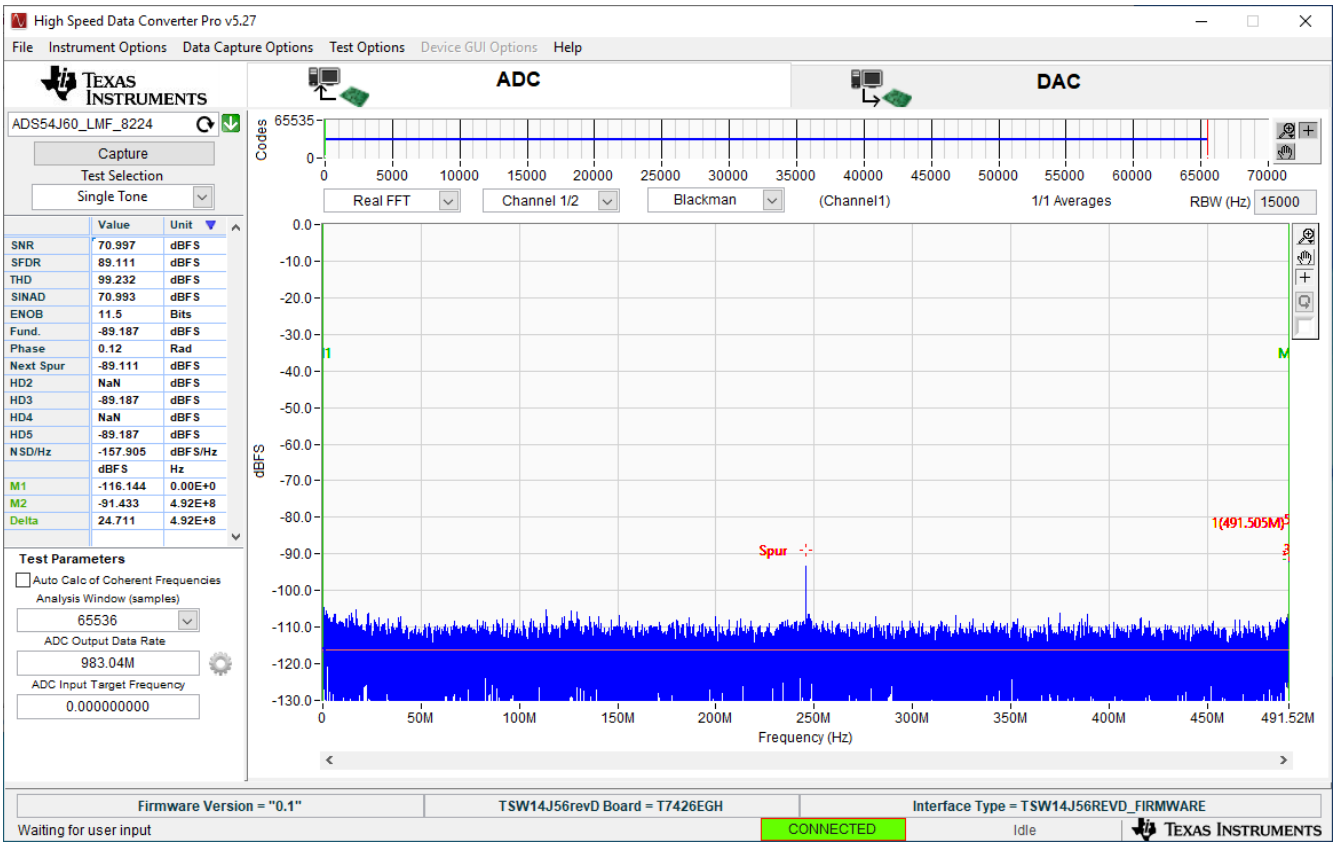

Figure 5-5. External Offset Correction

6 Summary

Interleaving is an effective way to greatly increase the sampling rate of the converter and Nyquist bandwidth. However, this architecture comes with the practical challenge of introducing undesired interleaving spurs into the spectrum. The ADS54J60 uses an DC corrector block that corrects for these spurs in the default configuration. For system applications where environmental temperature variations are of concern, this application note demonstrates how to implement the external offset correction feature to maintain the amplitude of the interleaving spurs.

7 References

1. Texas Instruments, *ADS54J60 Dual-Channel, 16-Bit, 1.0 GSPS Analog-to-Digital Converter*, data sheet.

8 Revision History

Changes from Revision * (May 2023) to Revision A (June 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed *ADC54JXX GUI* to *ADS54JXX GUI*	7

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265