Analog Engineer's Circuit

ADS9218 Power-Optimized Signal Chain Circuit

Data Converters *Art Kay*

Design Goals

Input		Output		Supply	
V_{inDif}	V_{cmi}	V_{outDif}	V_{cmo}	V_{cc}	V_{ee}
±3.64 V	–2.05 V to 5.35 V	±3.64 V	+2.048 V	5 V	0 V

Design Description

For most successive approximation register (SAR) analog-to-digital converters (ADCs), optimizing the input amplifier and RC filter is the most challenging part of the design process. The problem is challenging because large high-frequency current transients are present on the ADC input. For this type of circuit, the amplifier bandwidth needs to be sufficient to respond to the transient charge kickback from the ADC. The RC filter is tuned to minimize the charge kickback issue and generally does not act as an effective antialiasing filter. The ADS9218 is a new-style SAR ADC that incorporates an internal high-impedance buffer, so that the external drive circuit no longer needs to respond to the current transients. An added benefit of this circuit is that the filter and amplifier bandwidth requirements can be adjusted to act as an antialiasing filter. The circuit configuration shown in this document is optimized for a 100-kHz input signal range. This document explains design tradeoffs and methods so that the circuit operation can be adjusted to meet requirements. Semiconductor test, battery test, and data acquisition (DAQ) are a few examples of power-sensitive systems that benefit from this SAR ADC design.

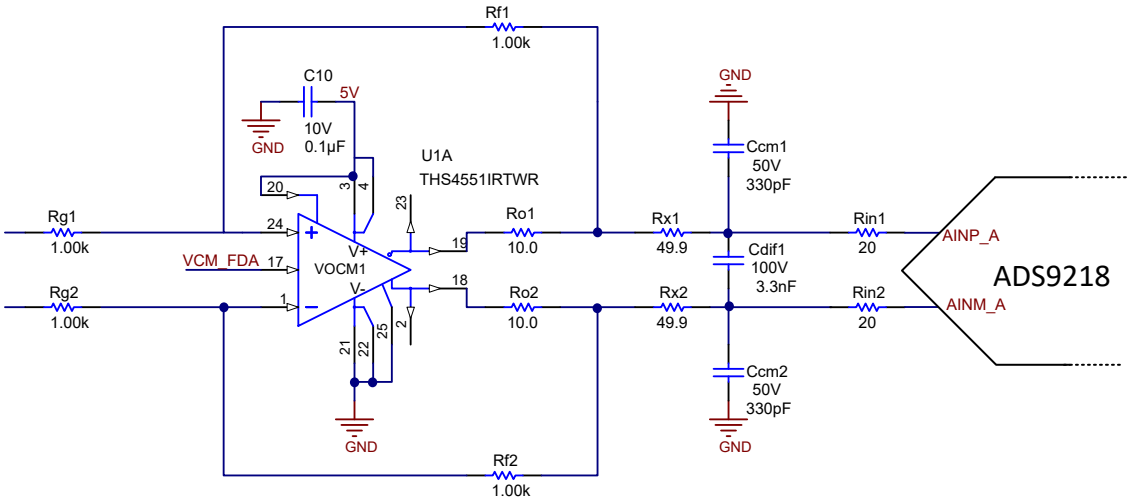

Figure 1-1. Differential Front End for ADS9218

Design Notes

1. Use 0.1% 20-ppm/°C film resistors or better for the gain set resistors: Rf1, Rf2, Rg1, and Rg2. This minimizes distortion, improves gain accuracy, and minimizes drift.
2. Select COG capacitors for all filter components to minimize distortion: Cf1, Cf2, Cdif, Ccm1, and Ccm2. Other types of capacitors have large voltage and temperature coefficients that introduce distortion.
3. The THS4551 and associated components were selected as the driver amplifier to get low distortion to 100 kHz. The THS4541 can be used to achieve low distortion to higher frequencies (for example, 1 MHz) at the cost of higher power consumption. The THS4561 is a low-power option that can be used for lower-bandwidth applications (for example, 20 kHz).
4. The THS4552 is a dual-channel version of the THS4551. This device is a good option for the ADS9218 because the ADS9218 is also a dual-channel device. This document references the single-channel THS4551 for comparison to other product families that are only available in single channels.
5. Ro1 and Ro2 are set to 10 Ω to flatten the open loop output impedance of the THS4552. This improves the stability of the amplifier for driving capacitive load.
6. Rin1 and Rin2 are input ADC isolation resistances. These resistors isolate the ADC from external capacitive loading and were empirically tuned to 20 Ω for the best performance on the ADS9218. Use these resistors on all similar designs for best THD.
7. The output filter Rx1, Rx2, Cdif1, Ccm1, and Ccm2 is an antialiasing filter. Traditional SAR drive requires this filter to be selected to respond to charge kickback transients. In the traditional designs, the filter normally cannot act as an effective antialiasing filter as the cutoff is generally set wider than the ADC sampling rate. The ADS9218 family has a high input impedance and no charge kickback, so the filter cutoff can be set according to antialiasing requirements.

Design Steps

1. Choose the gain, and feedback network. The value of R_g is set to 1 kΩ for peak performance on THS4551. Other amplifiers can use other resistors for best SNR and stability.

$$G = \frac{V_{outDif}}{V_{inDif}} = \frac{\pm 3.2\ V}{\pm 3.2\ V} = 1$$

$$Let\ R_g = 1\ k\Omega$$

$$R_f = R_g G = 1\ k\Omega$$

2. Find the maximum output differential signal based on the output high and output low swing. V_{cmo} is generated by the ADS9218 and used by the THS4551 for peak performance. The ADS9218 has an input range of ±3.2 V, so the linear output range of the THS4551 is sufficient.

$$V_{outHigh} = (V_{s+} - 0.23\ V) = 4.77\ V$$

$$V_{outLow} = (V_{s-} + 0.23\ V) = 0.23\ V$$

$$V_{cmo} = 2.048\ V$$

$$V_{outDif(high)} = 2\left(V_{outHigh} - V_{cmo}\right) = 2(4.77\ V - 2.048\ V) = 4.44\ V$$

$$V_{outDif(low)} = 2(V_{cmo} - V_{outLow}) = 2(2.048\ V - 0.23\ V) = 3.64\ V$$

$$V_{outDif} = min\left(V_{outDif(high)}, V_{outDif(low)}\right) = 3.64\ V$$

3. Find the common mode limits for the input signal (V_{cmi}) is based on: the common mode limits of the FDA (V_{cmFDA}), the common mode of the output signal (V_{cmo}), the differential input signal, and the gain (G). In this example the input signal common mode can range from –2.048 V to 5.352 V.

$$V_{cmFDA(max)} = (V_{s+} - 1.3\ V) = 3.7\ V$$

$$V_{cmFDA(min)} = V_{s-} = 0.0\ V$$

$$V_{cmo} = 2.048\ V$$

$$V_{cmi(max)} = \left(1 + \frac{1}{G}\right)V_{cmFDA(\max)} - \frac{1}{G}V_{cmo} = 5.352\ V$$

$$V_{cmi(min)} = \left(1 + \frac{1}{G}\right)V_{cmFDA(\min)} - \frac{1}{G}V_{cmo} = -2.048\ V$$

4. Choose the bandwidth limit of the amplifier and output filter. This filter frequency can be adjusted to act as a good antialiasing filter. In this example, achieving some attenuation by the Nyquist frequency is desired, but also have minimal attenuation up to 100 kHz. The sampling rate is 10 MHz so the Nyquist frequency is $f_s/2$ = 5 MHz. Choose an attenuation of 0.1 V/V at the Nyquist frequency. Using the following equation, the cutoff needs to be 502 kHz. The gain at 100 kHz is calculated to be 0.981 V/V or –0.17 dB, which is a reasonable error for the example design. In your application, if greater attenuation at the Nyquist frequency is required then move the cutoff to a lower frequency or increase the order of the filter.

$$f_c = \frac{f_{Nyq}}{\sqrt{\left(\frac{1}{G}\right)^2 - 1}} = \frac{5\ MHz}{\sqrt{\left(\frac{1}{0.1\ V/V}\right)^2 - 1}} = 502\ kHz$$

$$G_{100\ kHz} = \frac{1}{\sqrt{\left(\frac{f}{f_c}\right)^2 + 1}} = \frac{1}{\sqrt{\left(\frac{100\ kHz}{502\ kHz}\right)^2 + 1}} = 0.981$$

5. Select the components in the passive output filter. The resistor Rx1 and Rx2 were set to 49.9 Ω to minimize bias current errors. Set the cutoff frequency of the amplifier filter to 502 kHz according to *step 4*. Set the differential cutoff frequency of the passive filter to 5 MHz. The common mode filter capacitor is normally set to 10 × less than the differential frequency to minimize common mode to differential conversion.

$$C_{dif1} = \frac{1}{2\pi f_c R_{f1}} = \frac{1}{2\pi(502\ kHz)2(49.9\ \Omega)} = 3.18\ nF = 3.3\ nF\left(standard\ value\right)$$

$$C_{cm1} = C_{cm2} = \frac{C_{dif1}}{10} = 330\ pF$$

6. Some cases are not practical or necessary to set the output filter cutoff using the previously-shown approach. In this case, set the cutoff at least five times the maximum applied frequency. For example, if the maximum applied frequency was 1 MHz, then make the cutoff at least 5 MHz to minimize gain error and distortion.

Signal Chain Power vs Performance Tradeoff

This document focuses mainly on the power optimized signal chain using the THS4551 amplifier. This option provides very good performance to signal frequencies of 100 kHz at an I_Q of 1.37 mA. The THS4541 can be used to achieve good performance to 1 MHz at the cost of additional power dissipation (I_Q = 10.1 mA). The circuit components used in the THS4541 option are shown in the following schematic. The same considerations given in the design notes and design steps were used in selecting these component values.

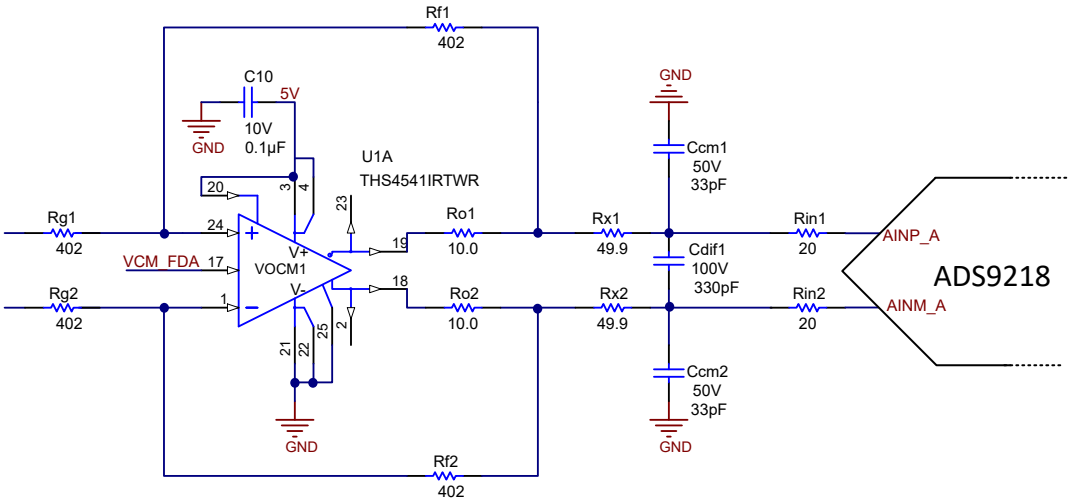

Figure 1-2. Signal Chain Optimized for 1 MHz With THS4541

Spice Model

The simulations given use the TINA SPICE model for the THS4552 and the ADS9218. The output of the amplifier and the output of the ADC are provided for all simulations.

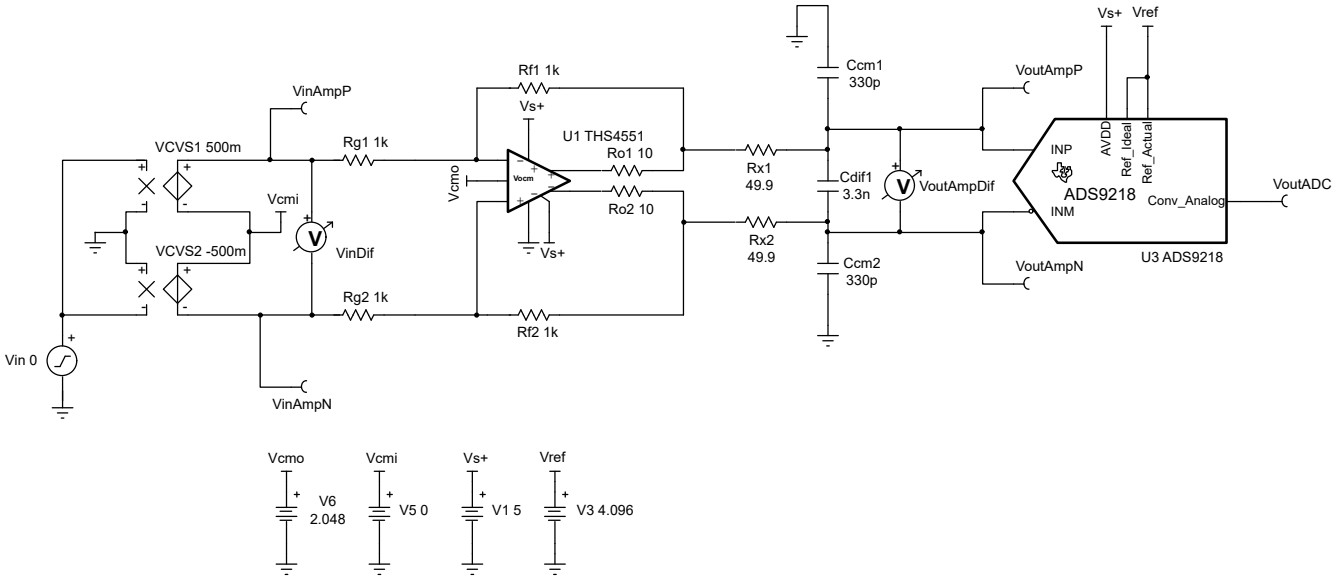

Figure 1-3. TINA Spice Model

AC Transfer Characteristics

The bandwidth of the amplifier (432 kHz) is set by the common mode and differential output filter (Rx1, Rx2, Cdif, Ccm1, and Ccm2). This filter pertains to the THS4551 circuit as shown in the *TINA Spice Model section*.

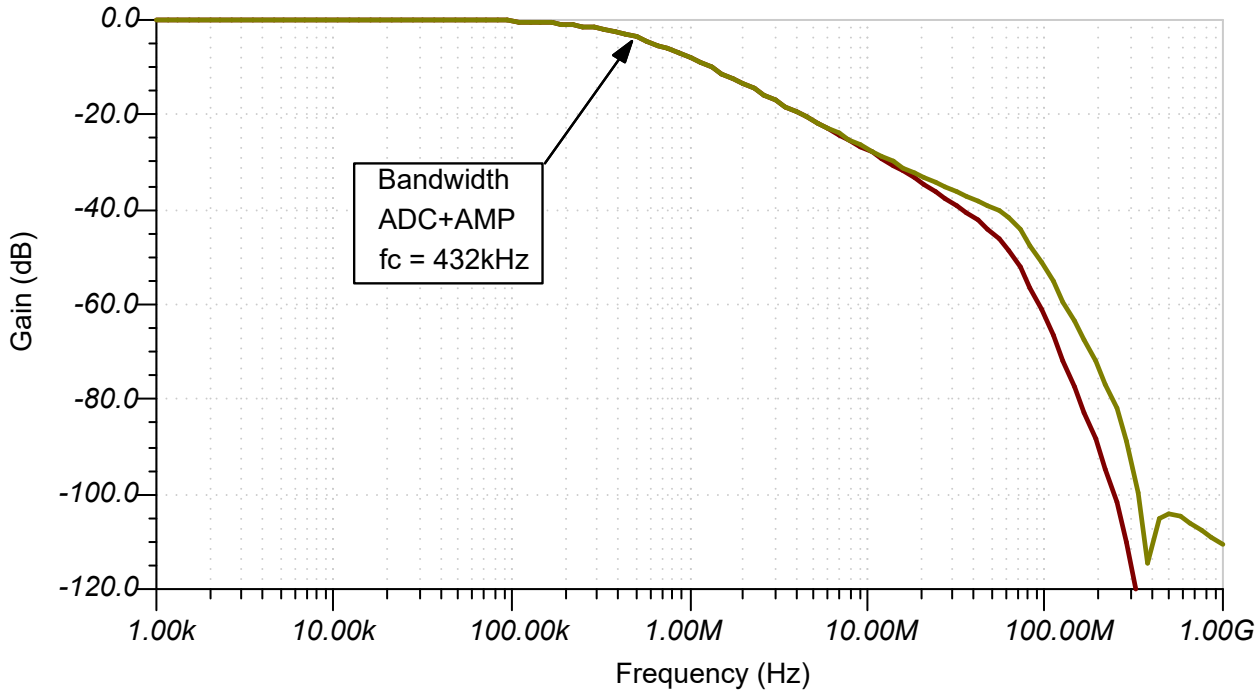

Figure 1-4. AC Transfer Characteristics (f_c = 432 kHz)

DC Transfer Characteristics

The following graph shows the DC transfer characteristics for the amplifier and ADC. Notice that the output swing of the amplifier is approximately ±4.4 V due to the output swing limitations of the THS4552. This matches the expected swing from ***Design Step 2***. The simulated ADC range is limited ±3.2 V, which matches the data sheet specification for this device. The absolute maximum ranges from AGND-0.3 V to AVDD+0.3 V, or –0.3 V to 5.3 V in this example. Note that VinM and VinP does not violate the ABS maximum specification.

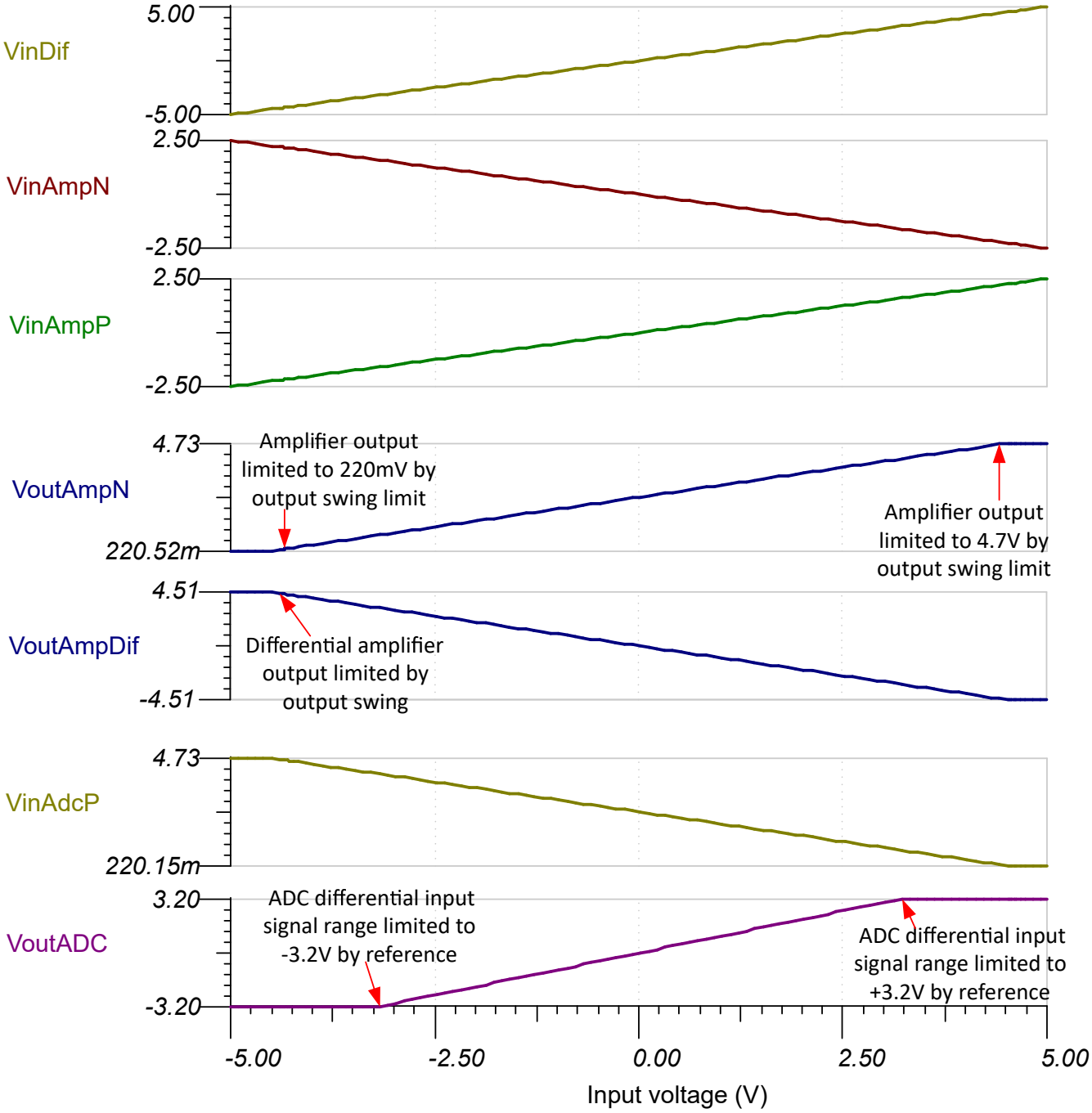

Figure 1-5. DC Transfer Characteristics (V_{cmi} = 0.0 V, V_{cmo} = 2.048 V, V+ = 5 V)

Noise

The amplifier noise is determined by the noise density of the amplifier, the feedback resistance, and the bandwidth limitations. The output filter limits the noise from the amplifier to 3.7 μV_{RMS}. The ADS9218 also contributes noise and bandwidth limitations. The noise simulation shows that the total noise from both the amplifier and ADC is 39.7 μV_{RMS}.

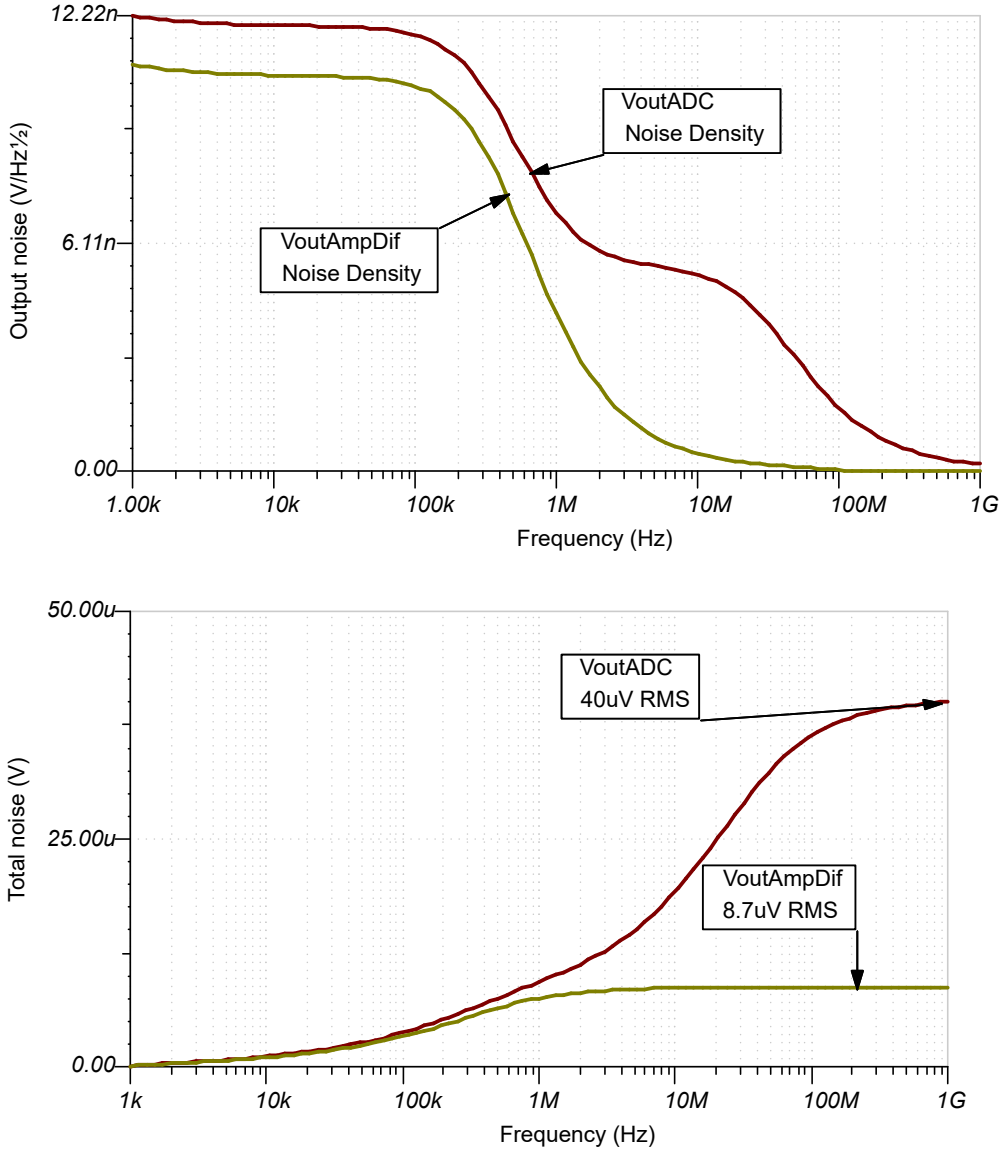

Figure 1-6. RMS Noise at Amplifier Output and ADC Output

Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS9218	Dual, Simultaneous Sampling, 18-bit, 10-MSPS SAR ADC with Fully Differential ADC Input Driver	www.ti.com/product/ADS9218	www.ti.com/adcs
THS4552	Dual-Channel, Low-Noise, Precision, 150-MHz, Fully Differential Amplifier	www.ti.com/product/THS4552	www.ti.com/opamp
THS4541	THS4541 Negative Rail Input, Rail-to-Rail Output, Precision, 850-MHz Fully Differential Amplifier	www.ti.com/product/THS4541	www.ti.com/opamp

Design References

1. Texas Instruments, *Analog Engineer's Circuit Cookbooks*

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