User's Guide

EMC Compliance Testing for Precision ADC Systems

Dale Li *Precision ADC*

ABSTRACT

This application note introduces electromagnetic compatibility (EMC) testing including a brief introduction and test setup specified for IEC 61000-4-x and CISPR 11 test standards. The test solution for collecting data through optical fibers from the ADS8686S EMC test board in this design has been proven to be reliable and feasible. The test results also demonstrate a robust EMC design solution based on the ADS8686S for industrial applications. The testing methods and data collection solution can be used in any similar IEC 61000-4-x and CISPR 11 testing for precision ADC systems.

Table of Contents

1 Introduction 3
2 Circuit Design and Test System 4
2.1 Design Description 4
2.2 Test System 7
2.3 Standards and Test Criteria 8
3 Test Details and Results 9
3.1 Electrical Fast Transients (EFT) 9
3.2 Electrostatic Discharge (ESD) 11
3.3 Surge Immunity (SI) 13
3.4 Conducted Immunity (CI) 15
3.5 Radiated Immunity (RI) 16
3.6 Radiated Emissions (RE) 18
4 Schematics 23
5 PCB Layouts 29
6 Bill of Materials 32
7 Acknowledgments 34
8 References 34
9 Revision History 34

List of Figures

Figure 1-1. ADS8686S EMC Test Board 3
Figure 2-1. ADS8686S EMC Test Board Circuit 5
Figure 2-2. PCB Layout Design – Plane Edge on Inner Negative Layer 6
Figure 2-3. General EMC Test Setup 7
Figure 3-1. Diagram of Laboratory Setup for EFT Test 9
Figure 3-2. Photograph of Laboratory Setup for EFT Test 10
Figure 3-3. Diagram of Laboratory Setup for ESD Test 11
Figure 3-4. Discharges to the HCP and VCP With ESD Gun 1 and 2 12
Figure 3-5. Photograph of Laboratory Setup for ESD Test 12
Figure 3-6. Diagram of Laboratory Setup for Surge Test 13
Figure 3-7. Photograph of Laboratory Setup for Surge Test 14
Figure 3-8. Diagram of Laboratory Setup for Conducted Immunity Test 15
Figure 3-9. Photograph of Laboratory Setup for Conducted Immunity Test 15
Figure 3-10. Diagram of Laboratory Setup for Radiated Immunity Test 16
Figure 3-11. Photograph of Laboratory Setup for Radiated Immunity Test 17
Figure 3-12. CISPR 11 Radiated Emission Limits for Class A and B Group 1 Equipment 18
Figure 3-13. Diagram of Laboratory Setup for Radiated Emission Test 19
Figure 3-14. Photograph of Laboratory Setup for Radiated Emission Test 19
Figure 3-15. Test 1 - Measured Radiated Emission, Horizontal Antenna Polarization 20

Figure 3-16. Test 2 - Measured Radiated Emission, Horizontal Antenna Polarization..... 20
Figure 3-17. Test 3 - Measured Radiated Emission, Vertical Antenna Polarization..... 21
Figure 4-1. Schematic – ADC..... 23
Figure 4-2. Schematic – Input of ADC - A..... 24
Figure 4-3. Schematic – Input of ADC - B..... 25
Figure 4-4. Schematic – Digital Isolation..... 26
Figure 4-5. Schematic – Power Supply..... 27
Figure 4-6. Schematic – Hardware..... 28
Figure 5-1. Layout – Top Layer..... 29
Figure 5-2. Layout – Inner Ground Layer..... 29
Figure 5-3. Layout – Inner Power Layer..... 30
Figure 5-4. Layout – Bottom Layer..... 30
Figure 5-5. Top Silkscreen..... 31
Figure 5-6. Bottom Silkscreen..... 31

List of Tables

Table 2-1. Test Criteria..... 8
Table 3-1. EFT Test Result..... 10
Table 3-2. ESD Test Result..... 12
Table 3-3. Surge Test Result..... 14
Table 3-4. Conducted Immunity Test Result..... 16
Table 3-5. Radiated Immunity Test Result..... 17
Table 3-6. CISPR 11 Electromagnetic Radiation Disturbance Limits (Quasi - Peak)..... 18
Table 3-7. Radiated Emission Test Result..... 22
Table 6-1. Bill of Materials..... 32

Trademarks

1 Introduction

The ADS8686S is a 16-channel, 16-bit, 1-MSPS, dual simultaneous-sampling, successive approximation register (SAR) analog-to-digital converter (ADC) with an integrated analog front-end (AFE) for single-ended, bipolar inputs up to ±12-V range with an overrange configuration. The integrated AFE with 1-MΩ input impedance eliminates requirements for an external ADC driver. These characteristics makes this ADC suitable for industrial automation applications including grid infrastructure and analog input modules. Figure 1-1 illustrates the ADS8686S EMC test board.

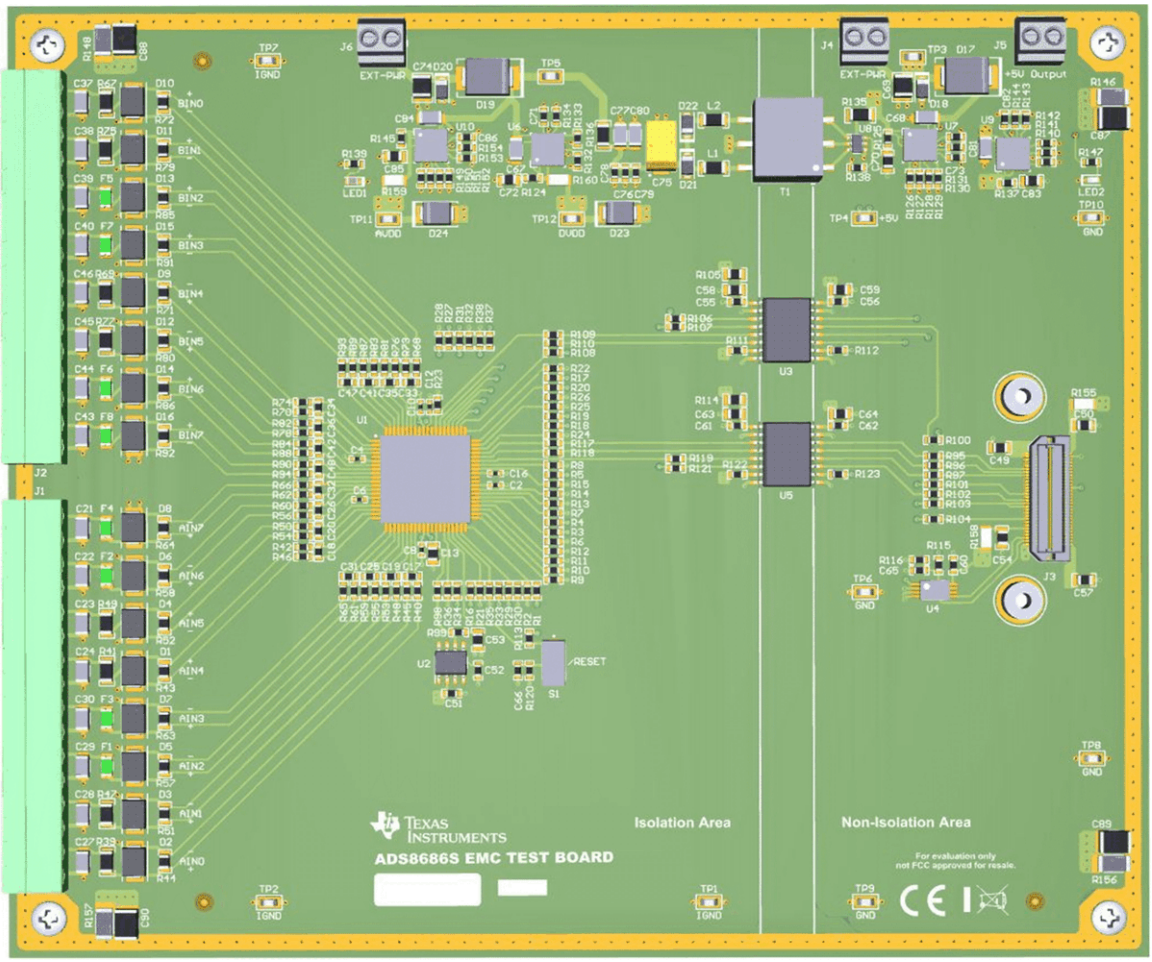

Figure 1-1. ADS8686S EMC Test Board

2 Circuit Design and Test System

2.1 Design Description

This circuit is designed with 16 analog input channels, isolated power supplies, and an isolated digital serial peripheral interface (SPI) that interfaces with a precision host interface (PHI) controller card for monitoring conversion data from the ADS8686S. The printed circuit board (PCB) layout is designed to satisfy the IEC 61000-4-x and CISPR 11 standards for working in a harsh electromagnetic environment. An external protection circuitry is designed on each analog input to protect the ADS8686S from electrical overstress (EOS) failure, and also surge (IEC61000-4-5), electrostatic discharge (ESD) (IEC61000-4-2), electrical fast transient (EFT) (IEC61000-4-4) transient signals.

2.1.1 Input Protection

The analog input on each channel of the ADC is protected with a bidirectional transient voltage suppressor (TVS) diode (SMBJ10CA from Littelfuse®) from a transient signal, and a positive temperature coefficient (PTC) resettable fuse (PTS120660V010 from Eaton®) is placed in series with the analog input to limit the transient current under an EMC test condition. The PTC fuse is a device that exhibits a low resistance under a normal condition and exhibits a high resistance in response to an overcurrent. The PTC stands for Positive Temperature Coefficient, so the PTC resistance increases with the increase of temperature. Under a test condition with high transient signals, the self-heating of the resistor causes the resistance to pass a trip point and the resistance dramatically increases. The large tripped resistance effectively limits the high transient current. Once the fault condition is removed, the PTC returns to a low-resistance state; however, the device has a hysteresis and it takes some time to reach a low-resistance value.

A 250-V, high-voltage, C0G type, 15-nF ceramic capacitor is designed on each analog channel of the ADC and placed next to the input terminal blocks so that the transient energy can be discharged to the ground through the shortest path.

2.1.2 Power Supply Design and Protection

The design and protection of the power supply is managed from either the non-isolation or isolation side of the circuit:

- Non-isolation side

  The low-dropout regulator (LDO), TPS7A4700 (U7), is designed to step down a 6- to 12-V input to +5 V for powering the circuits on the non-isolation side on the test board including the SN6505 (U8) which is a low-noise, low electromagnetic interference (EMI) push-pull transformer driver. A second TPS7A4700 (U9) regulates the U7 output to +3.3 V for the ISO7742 digital isolators (U3 and U5) on the test board.

  A bidirectional TVS diode (MBJ15CA, D18) is used to clamp any high transient or fault signal from external power supply that is applied to the terminal block (J4). The TVS diode is able to clamp a transient voltage higher than 15 V (nominal). A Schottky diode (MBRS4201, D17) is inserted after the D18. Both diodes are intended to prevent potential miswiring from an external power supply connection to the power supply input on J4. The same protection scheme is designed for the power supply on the isolation side.
- Isolation side

  The power supplies (+3.3 V and +5 V) on the isolation side are generated from two low-dropout regulators (LDOs), U6 and U10, which regulate the output from the transformer (T1) and the SN6505 (U8) which is a low noise, low EMI push-pull transformer driver on the non-isolation side on the test board.

  The TPS7A4700 (U6) generates +5-V power supply for the ADS8686S ADC and REF5025 (U2) voltage reference. The second TPS7A4700 (U10) generates +3.3-V power supply for the ADS8686S (U1) and the digital isolators (U3 and U5) on the isolation side of the test board. The +5-V power supply is protected with a 5.6-V TVS diode (D24), and also the +3.3-V power supply is protected with a 3.9-V TVS diode (D23).

The power supply circuits on the ADS8686S EMC test board are intentionally designed to be compatible with the robust design in a typical industrial system. The ADS8686S EMC test board has an alternative solution powered by two DC power supplies to provide the necessary supplies separately on the isolation and non-isolated side of the test board.

2.1.3 Digital Isolation Design

This circuit is designed with ISO7742 digital isolators to isolate the data communication. The ISO7742 isolator is reinforced with high-immunity, a 5-kV_{RMS} isolation voltage, 8-kV_{PK} maximum transient isolation voltage and 6-kV_{PK} maximum surge isolation voltage. This isolator supports signal rate up to 100 MSPS with a typically low propagation delay (10.7 ns) and a wide supply range (2.35 V to 5.5 V).

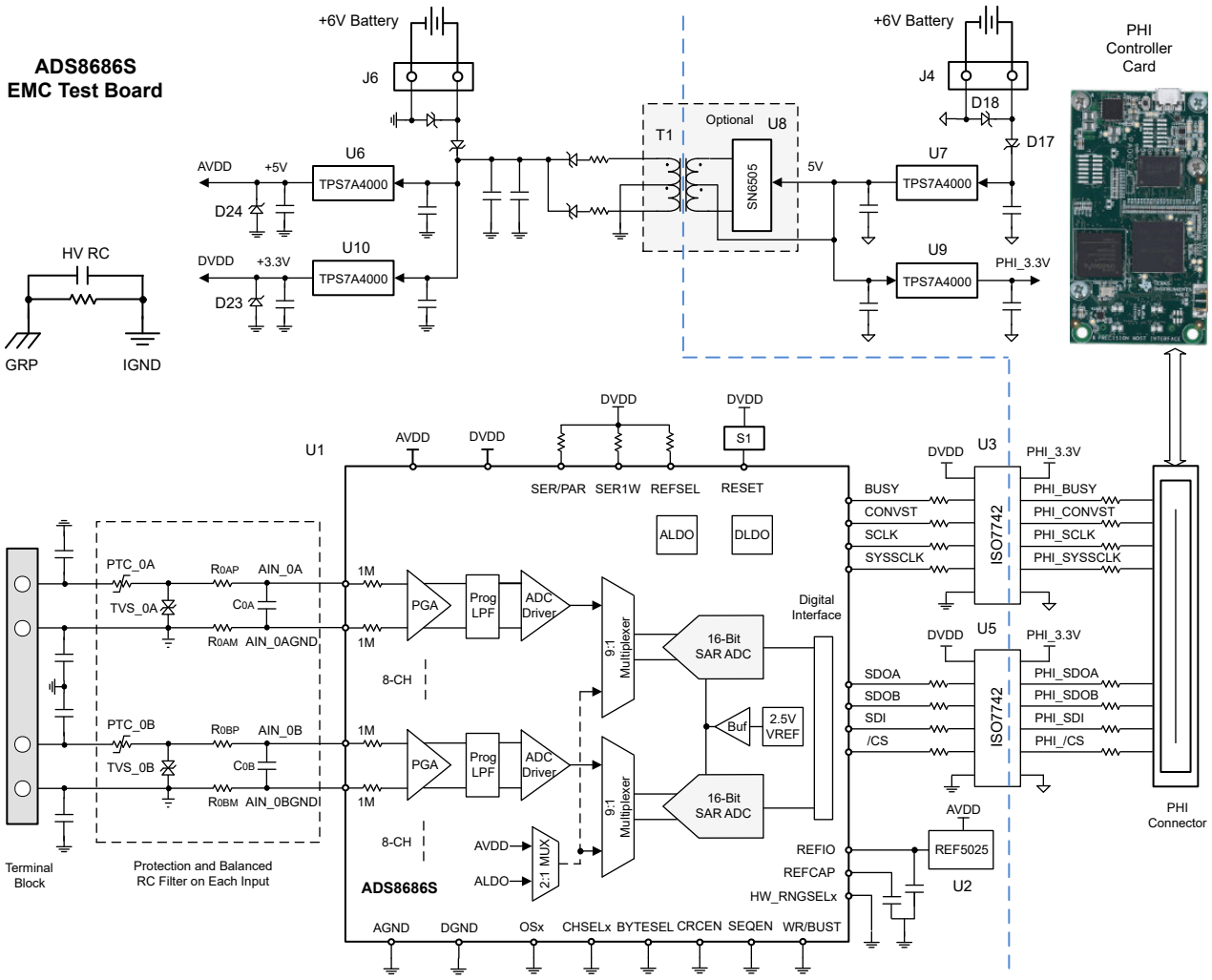

Figure 2-1. ADS8686S EMC Test Board Circuit

2.1.4 Component Selection and Layout Considerations

On the isolation side of the test board, a high-voltage 3-kV, 2.2-nF capacitor in parallel with a 2.2-kV, 3.3-MΩ resistor is placed between the protected ground and the earth ground for providing a path to discharge the transient energy. There are two discharge paths on the isolation side. The same scheme is used in the non-isolation area on the test board.

The 49.9-Ω damping resistors on the digital lines between the ADS8686S and the precision host interface (PHI) controller board are designed to attenuate the electrical transient signals and slow down fast logic edges to minimize EMI (Electromagnetic Interference) or RFI (Radio Frequency Interference) problems.

The decoupling capacitors are placed as close as possible next to the device where it requires decoupling, and they are connected to the ground plane using vias. Power planes are used instead of individual traces to reduce the inductance and provide better decoupling to the ground plane.

The ADS8686S is a single-ended input ADC; however, it samples the difference between the positive pin (AIN_nA/B) and the negative input pin (AIN_nA/BGND). In this design, the traces for these two signals in each channel are routed closely to each other as a differential pair so that any external any interference and

noise intervening with these two traces add the same amount of disturbance into both traces. Therefore, the induced noise signal is a common-mode signal which the ADC will reject within the common-mode rejection ratio (CMRR) specification limits.

The vias or via holes in multilayer PCBs should be avoided as much as possible because each via introduces capacitance and inductance. Also, the critical traces such as clocks should be routed on the same layer without the use of a via to minimize radio frequency (RF) emissions and susceptibility. In this design, no via is used for analog signal routing purposes across layers and all traces for analog signals are routed on the top layer.

The ADS8686S EMC test board is built on a four-layer PCB which is a minimum stack-up as a practical recommendation. The second layer is the inner ground (GND and IGND) layer for good decoupling and ground returns as an adjacent layer. The noise on the power and ground planes that reaches the edge of the circuit board can radiate out of the board. The guard ring on the PCB edge surrounding the entire circuit board is a grounding technique that can reflect the noise back into the circuit board and isolate the noisy environment outside of the ring because there is no current flowing through the guard ring in a normal operation. The guard ring is usually connected to the chassis and earth ground. The guard ring on the ADS8686S EMC test board is designed on both top and bottom layers, and the edge guard on these layers are linked together with vias every 100-mil space to attenuate emissions of high frequency signals up to GHz.

The space across the isolation barrier on the EMC test board is designed as wide as possible to maintain high-voltage isolation requirements for IEC testing. The plane that is exposed at the edge of a PCB board can provide a breakdown path especially when the plane is terminated at the edge of the circuit board in a sharp corner shape, where it enhances electric fields and becomes a location for arcing. A good PCB design example in Figure 2-2 shows that the sharp corners of inner planes are rounded off and the planes are moved back from the edge to enhance the isolation design and avoid potential breakdowns.

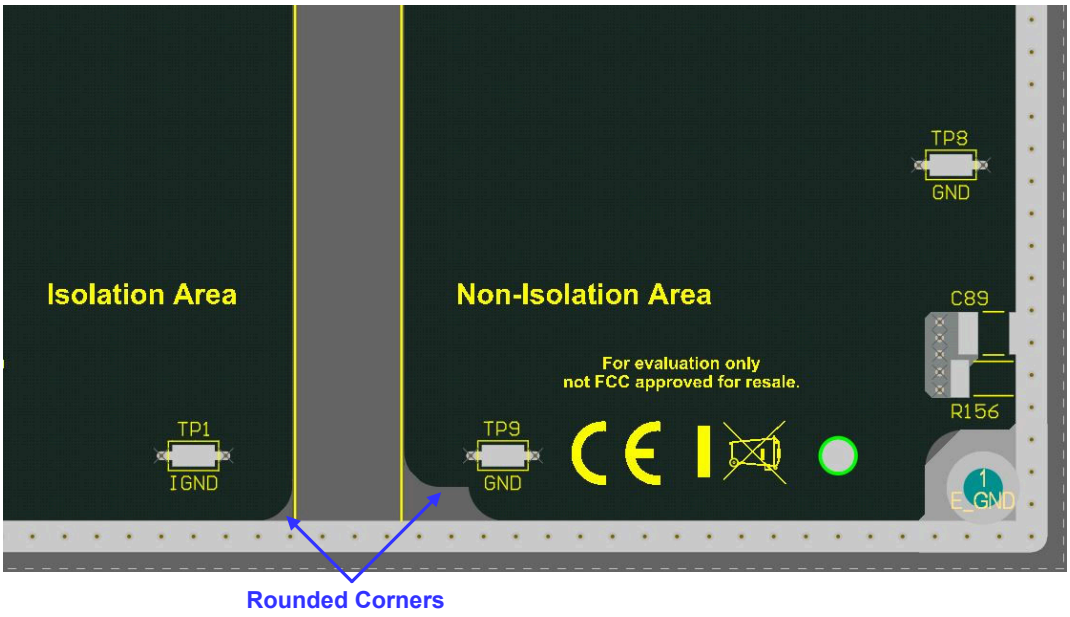

Figure 2-2. PCB Layout Design – Plane Edge on Inner Negative Layer

2.2 Test System

Figure 2-3 shows the general setup of the ADS8686S EMC test board for EMC testing. A software script is developed to configure the running parameters on a laptop, such as serial peripheral interface (SPI), clock frequency configuration, ADC mode selection, data capture and analysis, data monitoring and exporting for post-processing. In each EMC test, the data is captured by the software and the PHI controller to verify the test system and the equipment under test (EUT) before the EMC event. The data is continuously monitored during the EMC test, and the data is captured to check the EUT functionality after the EMC test.

The PHI controller card provides a necessary communication interface between the ADS8686S EMC test board and the laptop over a USB 2.0 (or higher) interface for digital input and output. An optical transceiver pair (bit-driver) is used between the laptop and the PHI controller card to isolate the harsh transient signals and test environment and provide an additional layer of protection for the user equipment.

2.2.1 Reference

The following equipment and software is needed to test the circuit:

- ADS8686S EMC test board
- PHI controller card from Texas Instruments
- Optical transceiver pair (bit-driver) with fiber optic cables
- 2-m twisted wire pair with a precision load resistor (100 Ω)
- ZEUS® 6-V battery 1 and 2
- Specific equipment for each EMC test
- Laptop running Microsoft® Windows® 10, 64-bit version
- Software script which is developed for EMC testing

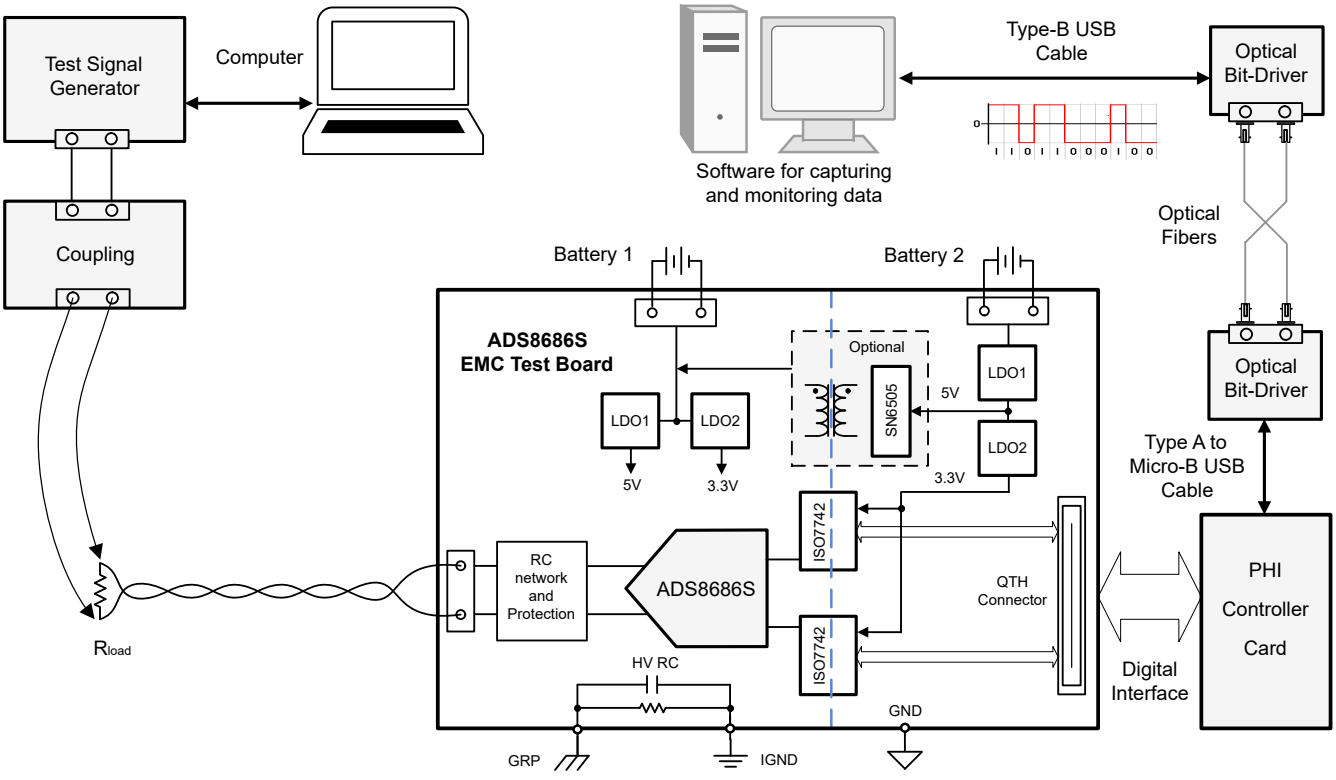

Figure 2-3. General EMC Test Setup

2.3 Standards and Test Criteria

The ADS8686S EMC test board is designed to meet the EMC and EMI test standard and criteria for industrial applications. According to the standard, the following six tests are selected:

- IEC 61000-4-2: Electrostatic Discharge (ESD)
- IEC 61000-4-3: Radiated Immunity (RI)
- IEC 61000-4-4: Electrical Fast Transients (EFT)
- IEC 61000-4-5: Surge Immunity (SI)
- IEC 61000-4-6: Conducted Immunity (CI)
- CISPR 11: Radiated Emissions for EMI from industrial, scientific and medical (ISM) equipment

The test criteria is described in Table 2-1.

Table 2-1. Test Criteria

Criteria	Description
A	Normal performance within specified limits
B	Temporary performance loss which can recover after disturbance ends
C	Temporary function or performance loss which can recover with user's intervention
D	Permanent function or performance loss due to damage or loss of data

3 Test Details and Results

3.1 Electrical Fast Transients (EFT)

The IEC 61000-4-4 standard specifies the details about the EFT test in terms of the test signals and the requirements. The purpose of the test is to verify the EFT immunity to burst stream of transient signals with short duration and fast rise time that can couple into the signal line. The standard defines four test voltage levels with two repetition frequencies for signal and control ports; 0.25 kV, 0.5 kV, 1 kV, and 2 kV at 5-kHz and 100-kHz repetition frequency. Each test covers positive and negative polarity discharge. The ADS8686S EMC test board was tested with the standard 1 kV and 2 kV, and also was tested at 4-kV levels, which are higher than required, but sometimes requested. The 100-kHz repetition frequency EFT testing is less commonly requested and more aggressive than 5 kHz. The ADS8686S EMC test board was tested at both frequencies. The EFT transient burst consists of 75 fast pulses followed by a break interval, and the burst stream is defined and tested as 15 ms for 5 kHz and 0.75 ms for 100 kHz with bursts repeated every 300 ms. Each individual burst pulse is a double exponential waveform with a rise time of 5 ns and a total pulse duration of 50 ns. The total test time for each test is approximately one minute.

Figure 3-1 shows the diagram of the setup and connection for the EFT immunity test. In this setup, the EFT threat is applied to the analog input of the ADS8686S EMC test board by running 2 m of twisted pair input wires through a 1-m length standard capacitive EFT clamp. All the cables in the test setup are kept in the insulation support. The EUT is placed on top of a ground reference plane (GRP) and isolated from the GRP by an insulating support material in 0.1-m height.

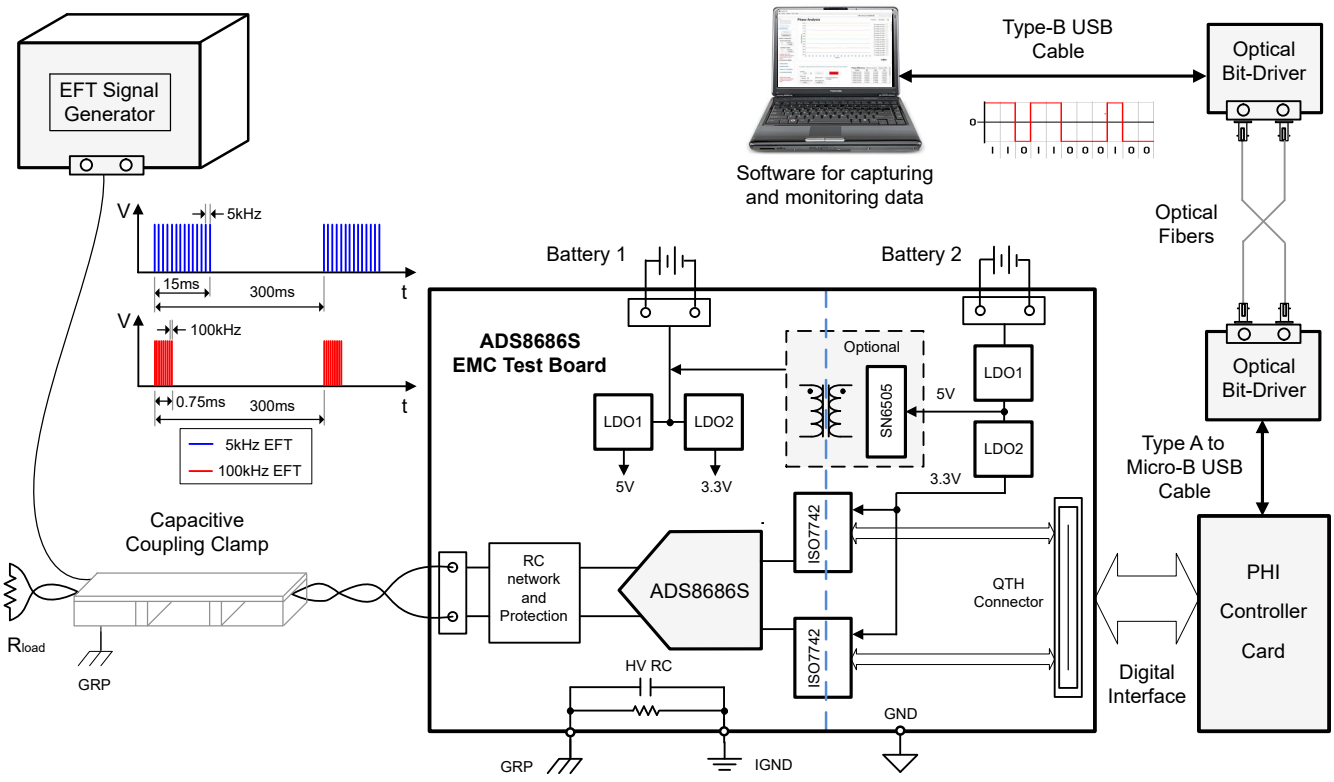

Figure 3-1. Diagram of Laboratory Setup for EFT Test

Figure 3-2 shows a photograph of the actual setup for the EFT test.

Figure 3-2. Photograph of Laboratory Setup for EFT Test

Table 3-1 shows the results of the EFT test.

Table 3-1. EFT Test Result

Test	IEC Standard	Test Signal		Test Level	Criterion	Test Result
		Voltage	Frequency			
EFT	IEC 61000-4-4	±1 kV	5 kHz	2	A	Pass
		±2 kV		3	B	Pass
		±4 kV		4	B	Pass
		±1 kV	100 kHz	2	A	Pass
		±2 kV		3	B	Pass
		±4 kV		4	B	Pass

3.2 Electrostatic Discharge (ESD)

The IEC 61000-4-2 standard specifies the details for ESD test including the test criterion and setup requirements. The main purpose of IEC 61000-4-2 test is to determine the immunity of EUT to external ESD events during operation. Figure 3-3 shows the diagram of the setup and connection for the ESD test. A 0.8-m high wood table stands on the GRP ground. A 1.6 m × 0.8 m horizontal coupling plane (HCP) is placed on the table. The EUT is tested and isolated on a 0.5-mm thick insulating mat that is placed on top of the HCP. The EUT is placed 0.1-m away from the vertical coupling plane (VCP) which has 0.5 m × 0.5 m dimensions and is placed on the insulating mat.

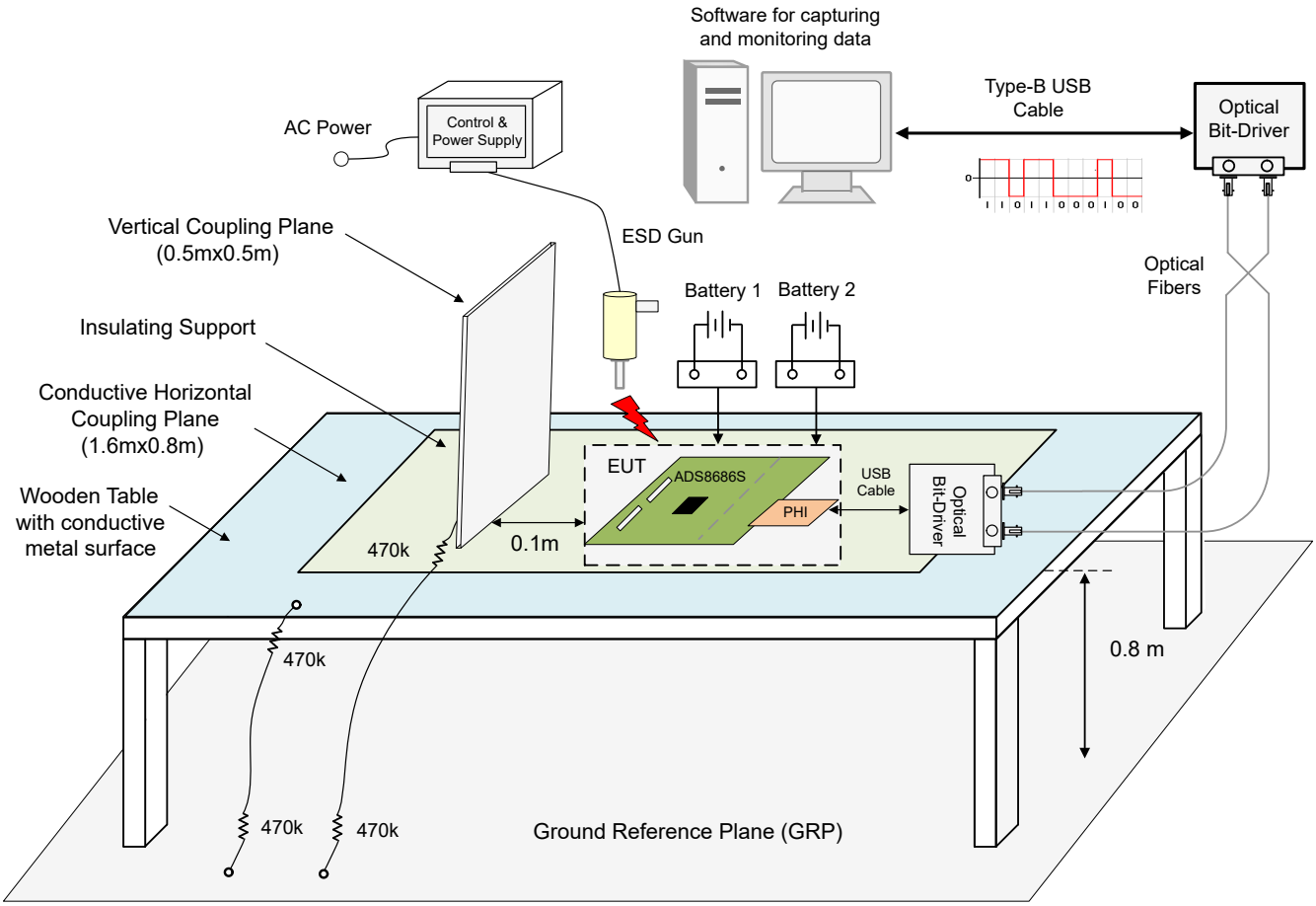

Figure 3-3. Diagram of Laboratory Setup for ESD Test

There are two types of ESD tests: contact discharge and air discharge. The contact discharge test is the most aggressive direct discharge test and the tip of the ESD gun is placed to conductive screws of the input terminal blocks (J1 and J2) on the ADS8686S EMC test board. Air discharge tests are run three different ways: direct air gap discharge, indirect discharge to the horizontal coupling plane (HCP), and vertical coupling plane (VCP). In the air gap discharge test, the tip of the ESD gun is placed near insulating surfaces of the input terminal blocks (J1 and J2) on the ADS8686S EMC test board. In the discharge test to the HCP and VCP, the ESD signal is discharged into a nearby conductive plane, representing an ESD strike onto the rack of equipment the design is mounted in. Figure 3-4 shows a zoomed-in view where the ESD strikes are applied. The discharges to the HCP and the VCP are individually done with the ESD gun 1 and the ESD gun 2 in the contact discharge mode. The ESD gun is held in the plane of the coupling plane and perpendicular to edge, then the ESD strikes are discharged into the edge of the plane.

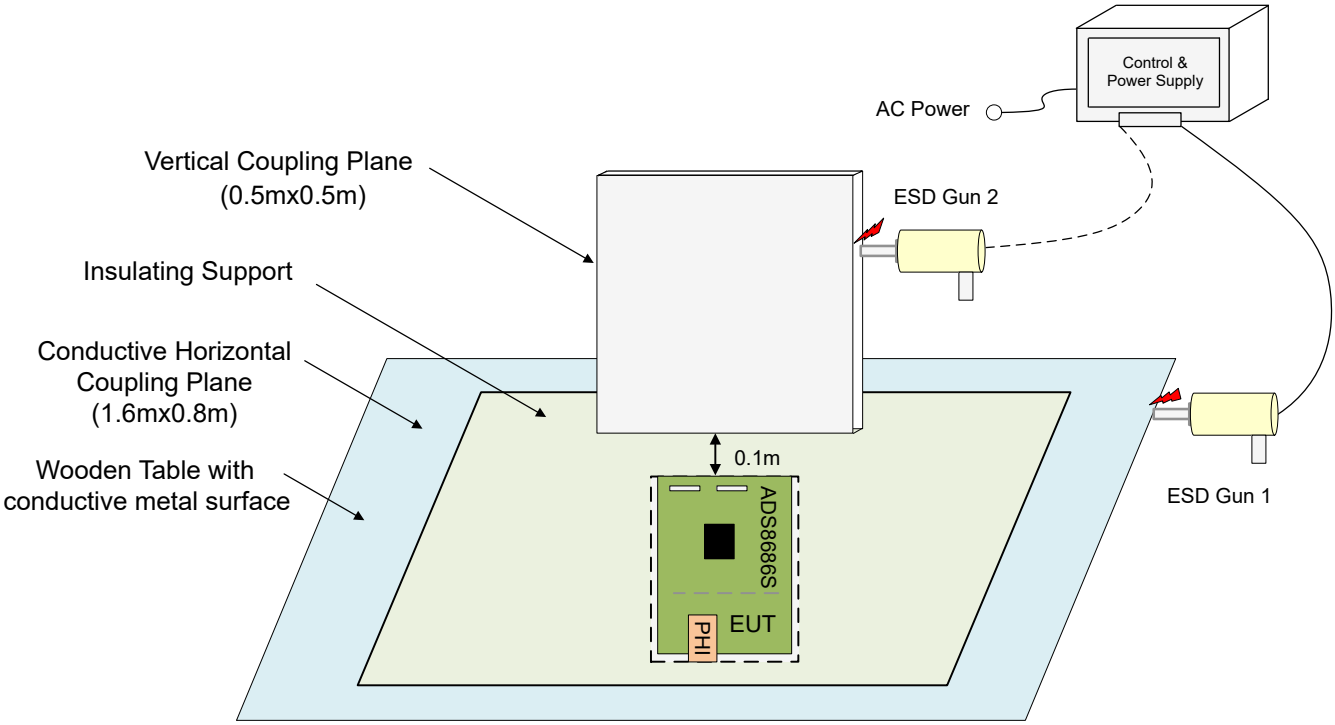

Figure 3-4. Discharges to the HCP and VCP With ESD Gun 1 and 2

Figure 3-5 shows a photograph of the actual setup for the ESD test.

Figure 3-5. Photograph of Laboratory Setup for ESD Test

For the ESD test, the EUT is tested with at least 20 discharges at each rating, 10 discharges each at a positive and negative polarity. Table 3-2 shows the results of the ESD test.

Table 3-2. ESD Test Result

Test	IEC Standard	Type	Test Voltage	Test Level	Criterion	Test Result
ESD	IEC 61000-4-2	Contact Discharge	+8 kV	4	A	Pass
			–8 kV		A	Pass
		Air Discharge	+15 kV	4	A	Pass
			–15 kV		A	Pass

3.3 Surge Immunity (SI)

The IEC 61000-4-5 standard details the test equipment and procedures for performing surge testing at a specific source impedance and coupling mode (line-to-line or line-to-ground). The test is to verify the EUT immunity on both power and data lines to high-energy surges caused by switching of power systems from load changes and short circuit faults, direct or indirect lighting strikes. The IEC 61000-4-5 specifies two types of combination wave generators (CWGs). The 10 µs / 700 µs CWG is specifically used to test the ports of symmetrical telecommunication lines. The 1.2 µs / 50 µs CWG is used for all other cases. The surge for all other cases combines a 1.2 µs / 50 µs (1.2-µs rising time with 50-µs pulse width) open-circuit voltage waveform and 8 µs / 20 µs (8-µs rising time with 20-µs pulse width) short-circuit current waveform. The EUT is subject to 5 positive and 5 negative surges at each rating. The surge is repeated at least once per minute. A coupling and decoupling network (CDN) is required by the surge test. The IEC 61000-4-5 defines the impedance and capacitance used in the coupling network in different cases. The EUT is tested with the surge through a coupling and decoupling network (CDN117) with a 0.5-µF capacitor and a twisted cable.

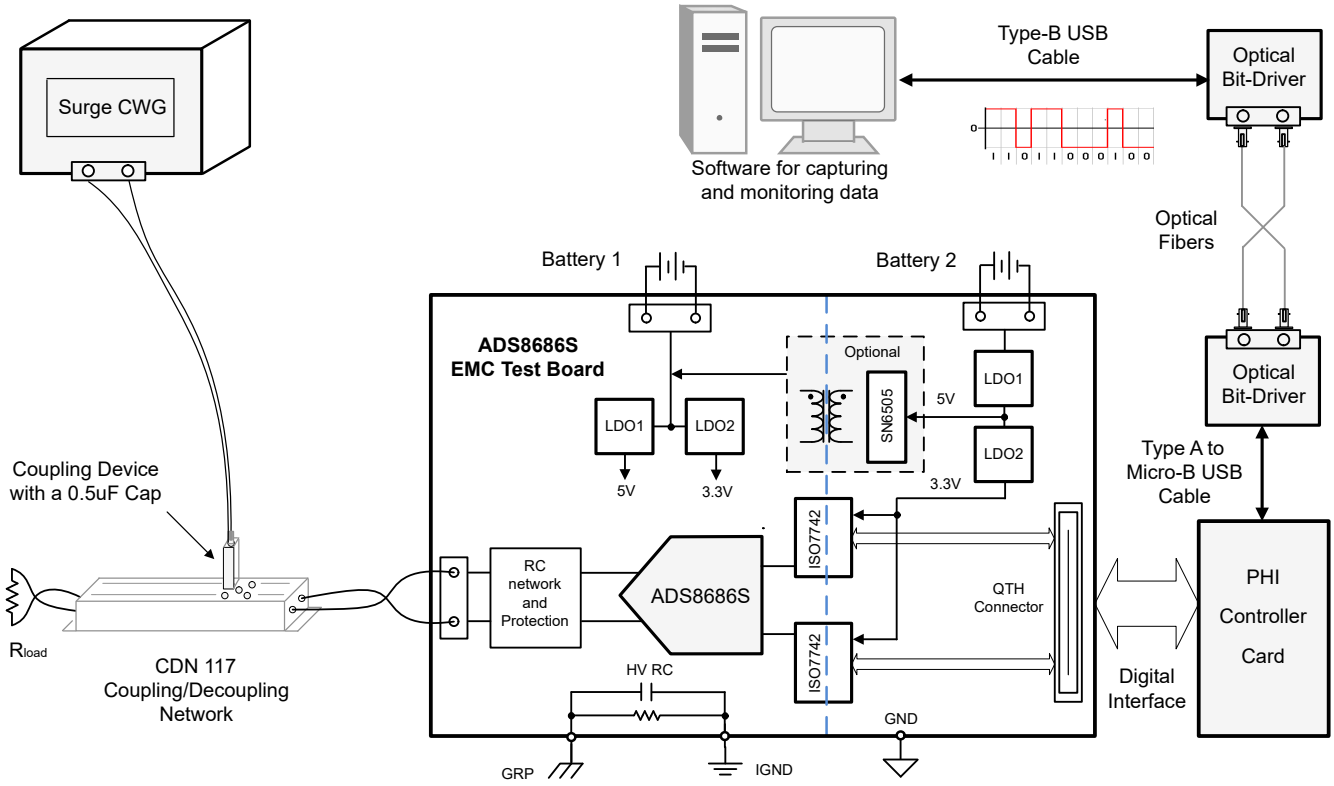

Figure 3-6. Diagram of Laboratory Setup for Surge Test

Figure 3-7 shows a photograph of the actual setup for the surge test. An oscilloscope is intended to monitor the output signal from surge signal generator during testing.

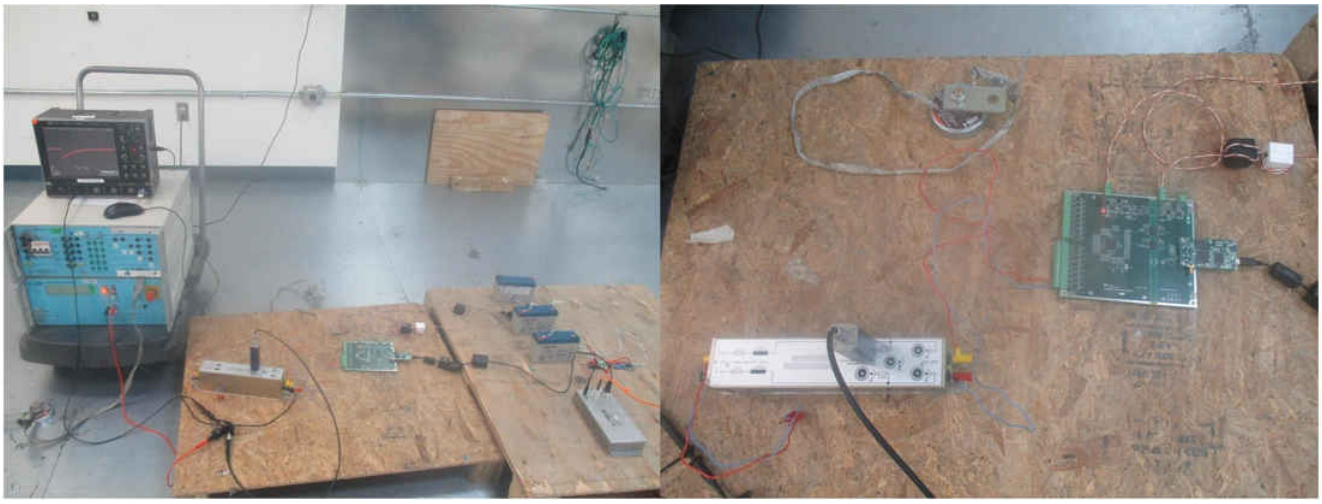

Figure 3-7. Photograph of Laboratory Setup for Surge Test

Table 3-3 shows the results of the surge test.

Table 3-3. Surge Test Result

Test	Standard	Type	Impedance	Test Voltage	Test Level	Criterion	Test Result
Surge	IEC 61000-4-5	Line-to-Line	42 Ω (2-Ω source impedance + 40 Ω from coupling network)	500 V	1	A	Pass
		Line-to-Ground	42 Ω (2-Ω source impedance + 40 Ω from coupling network)			B	Pass
		Line-to-Line	42 Ω (2-Ω source impedance + 40 Ω from coupling network)	1 kV	2	A	Pass
			2-Ω source impedance only(1)			B	Pass
		Line-to-Ground	42 Ω (2-Ω source impedance + 40 Ω from coupling network)			B	Pass
			2-Ω source impedance only(1)			B	Pass

(1) The test has a higher peak current (250 A for level 1 and 500 A for level 2) and is more aggressive than other tests in the table.

3.4 Conducted Immunity (CI)

The IEC 61000-4-6 standard specifies the details about the conducted immunity test. The test is to verify the EUT immunity to conducted electromagnetic disturbances induced onto the EMC board input terminals. The test signal is generated from an RF signal generator and RF power amplifier equipment is used to amplify the test signal to a specified level. The test signal is injected to the EMC board input with an injection probe. The spectrum analyzer 1 is used to monitor the output of the power amplifier, and the spectrum analyzer 2 is used to monitor and verify the injected signal with a monitoring probe. The signal frequency is swept from 150 kHz to 80 MHz with a disturbance signal of 80% amplitude that is modulated with a 1-kHz sinusoidal signal. Two field strength levels are applied and tested: 3 V/m and 10 V/m.

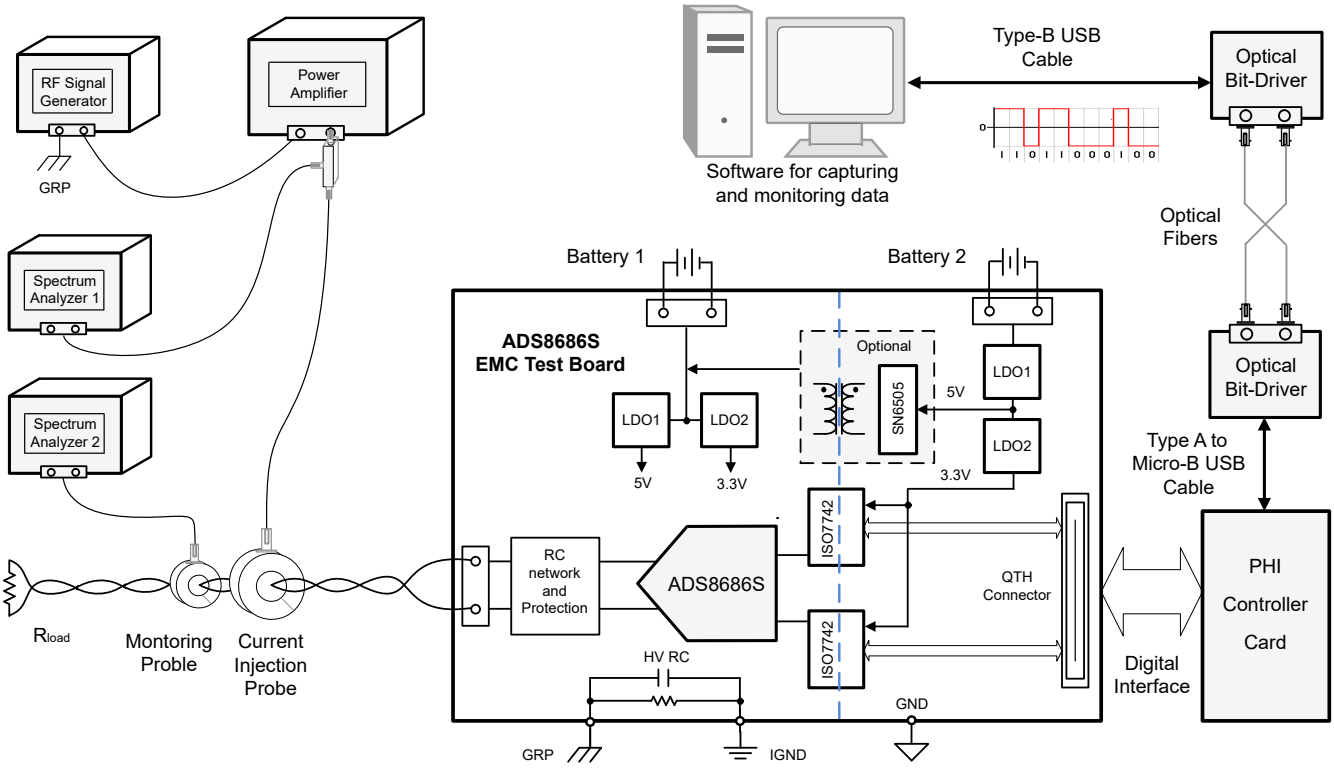

Figure 3-8. Diagram of Laboratory Setup for Conducted Immunity Test

Figure 3-9 shows a photograph of the actual setup for the conducted immunity test.

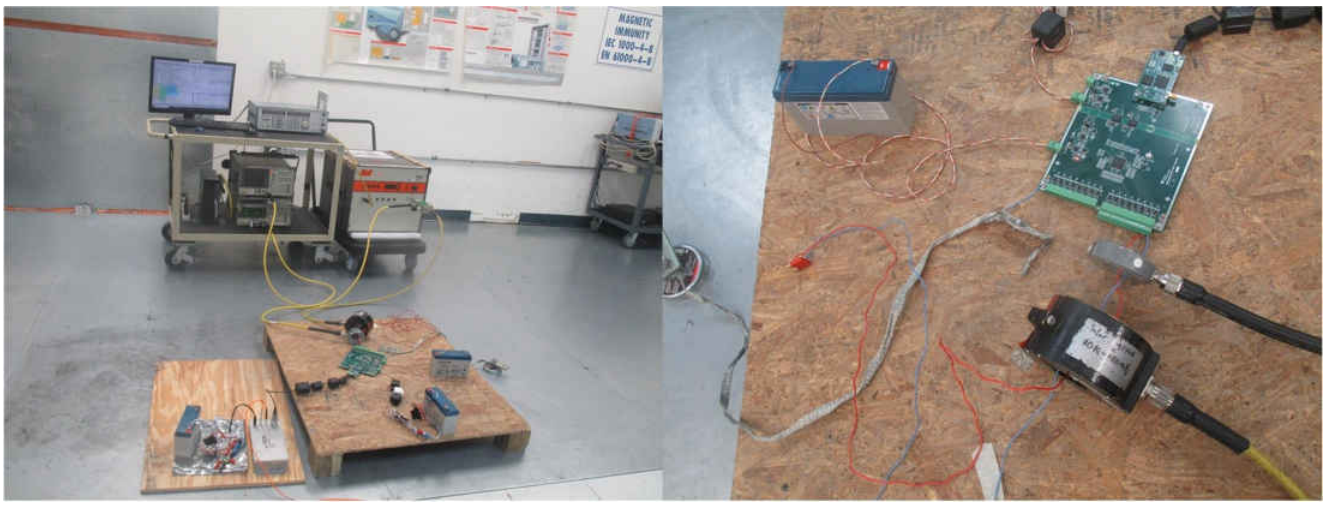

Figure 3-9. Photograph of Laboratory Setup for Conducted Immunity Test

Table 3-4 shows the results of the conducted immunity test.

Table 3-4. Conducted Immunity Test Result

Test	IEC Standard	Test Signal		Test Level	Criterion	Test Result
		Field Strength	Frequency			
Conducted Immunity (CI)	IEC 61000-4-6	3 V/m	150 kHz–80 MHz	2	A	Pass
		10 V/m	150 kHz–80 MHz	3	A	Pass

3.5 Radiated Immunity (RI)

The IEC 61000-4-3 standard specifies the details about the radiated immunity test. The purpose of this test is to verify the EUT immunity to electromagnetic radiation that are generated by radio transmitters, cellular phones, and other industrial electromagnetic sources. The test is performed in an anechoic chamber and the EUT is placed on a non-conductive table at 0.8-m height. The test distance between the EUT and the antenna is 3 m. The EUT is exposed and tested in the field of horizontal and vertical polarity at each rating. The RF test signal is swept from 80 MHz to 1 GHz, and from 1 GHz to 2.7 GHz with a disturbance signal of 80% amplitude modulated with a 1-kHz sinusoidal signal. The field strength is 10 V/m and 18 V/m for each frequency range. The conversion data is captured from the EUT by the PHI controller card and sent to the laptop running the software script outside the chamber through the fully isolated optical fiber cables.

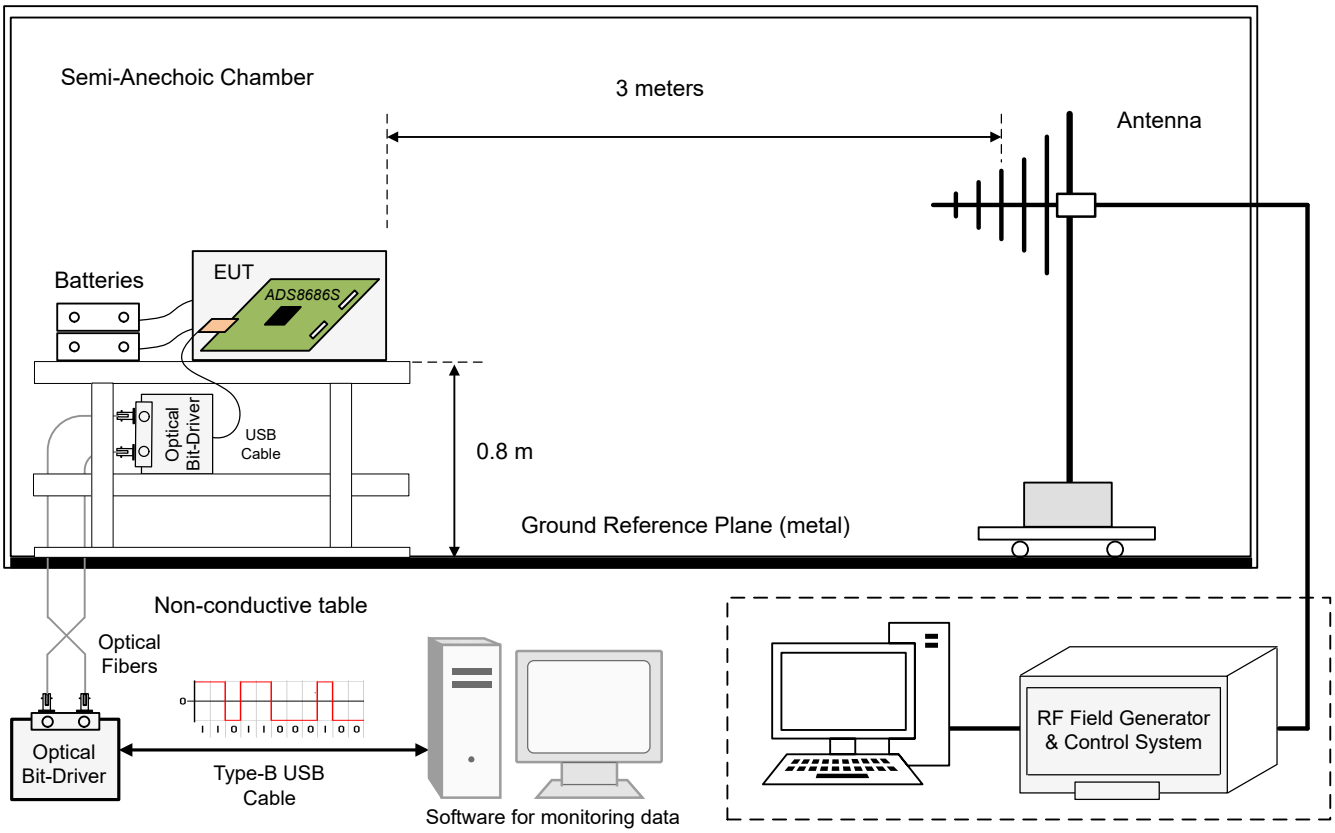

Figure 3-10. Diagram of Laboratory Setup for Radiated Immunity Test

Figure 3-11 shows a photograph of the actual setup for the radiated immunity test.

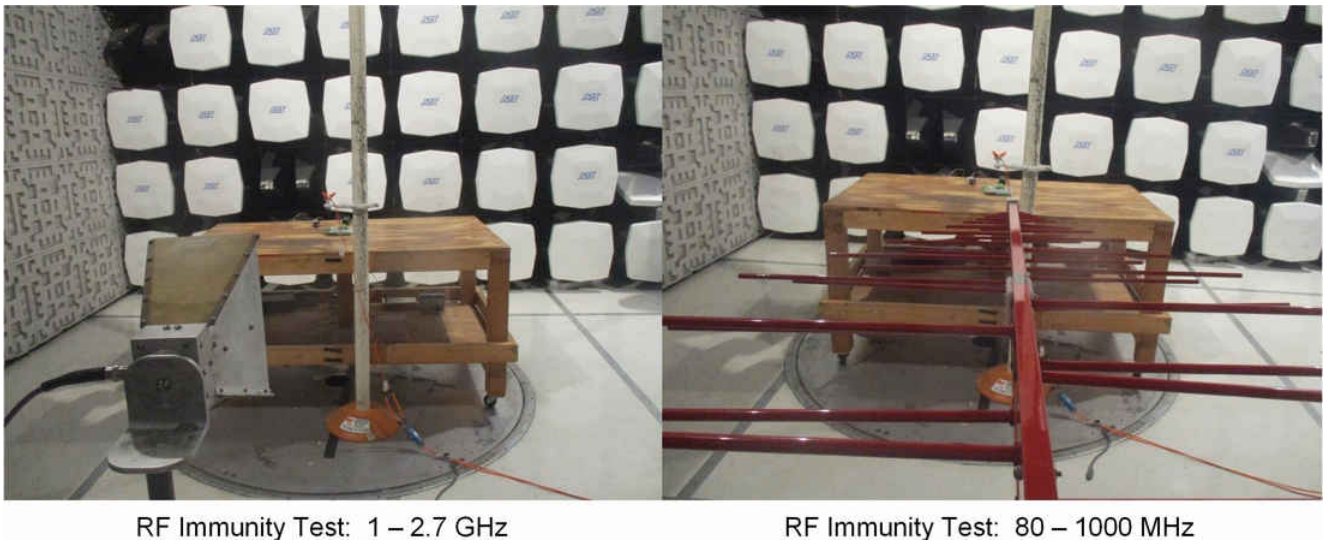

Figure 3-11. Photograph of Laboratory Setup for Radiated Immunity Test

Table 3-5 shows the results of the radiated immunity test.

Table 3-5. Radiated Immunity Test Result

Test	IEC Standard	Test Signal			Test Level	Criterion	Test Result
		Field Strength	Frequency	Antenna Polarization			
Radiated Immunity (RI)	IEC 61000-4-3	10 V/m	80–1000 MHz	Horizontal	3	A	Pass
				Vertical		A	Pass
			1–2.7 GHz	Horizontal		A	Pass
				Vertical		A	Pass
		18 V/m	80–1000 MHz	Horizontal	> 3	A	Pass
				Vertical		A	Pass
			1–2.7 GHz	Horizontal		A	Pass
				Vertical		A	Pass

3.6 Radiated Emissions (RE)

The CISPR 11 standard defines requirements, test procedures, and limits for radiated disturbances from industrial, scientific, and medical (ISM) equipment. The purpose of this test is to measure and evaluate the radiated emissions that are generated by the EUT. The test is performed in a semi-anechoic chamber and the EUT is placed on a nonconductive table at 0.8-m height. The table with the EUT is intended to be rotated from 0° to 360° to find the direction of maximum radiated emission. The height of the receiving antenna is varied between 1 m and 4 m to find the maximum field strength. The measurement distance between the EUT and the receiving antenna is 3 m. An alternative measurement distance is 10 m, which has a different limit. The EUT is scanned in the frequency band between 30 MHz and 1 GHz. The radiation from the EUT is received by the receiving antenna, which is set to a horizontal or vertical polarization position for each testing. The signal from the antenna is connected to the input of an EMI test receiver and spectrum analyzer for signal acquisition and analysis with a specified resolution bandwidth and detector type. A pre-amplifier can be used if necessary. The test system for the EUT is configured in quasi peak detection mode, which is effectively weighed by the repetition rate of energy in the band.

Table 3-6 shows the CISPR 11 quasi - peak (QP) limits for Group 1 ISM equipment which includes all ISM equipment that uses RF energy only for internal functioning of the equipment.

Table 3-6. CISPR 11 Electromagnetic Radiation Disturbance Limits (Quasi - Peak)

Frequency Range (MHz)	3-m Distance		10-m Distance	
	Class A (dBµV/m)	Class B (dBµV/m)	Class A (dBµV/m)	Class B (dBµV/m)
30–230	50.5	40.5	40	30
230–1000	57.5	47.5	47	37

Note

The equipment intended primarily for use in a residential environment must meet Class B limits, while all other equipment comply with Class A.

Figure 3-12 plots the relevant limit lines for Class A and Class B at 3-m and 10-m distance between the antenna and EUT when using a QP detector.

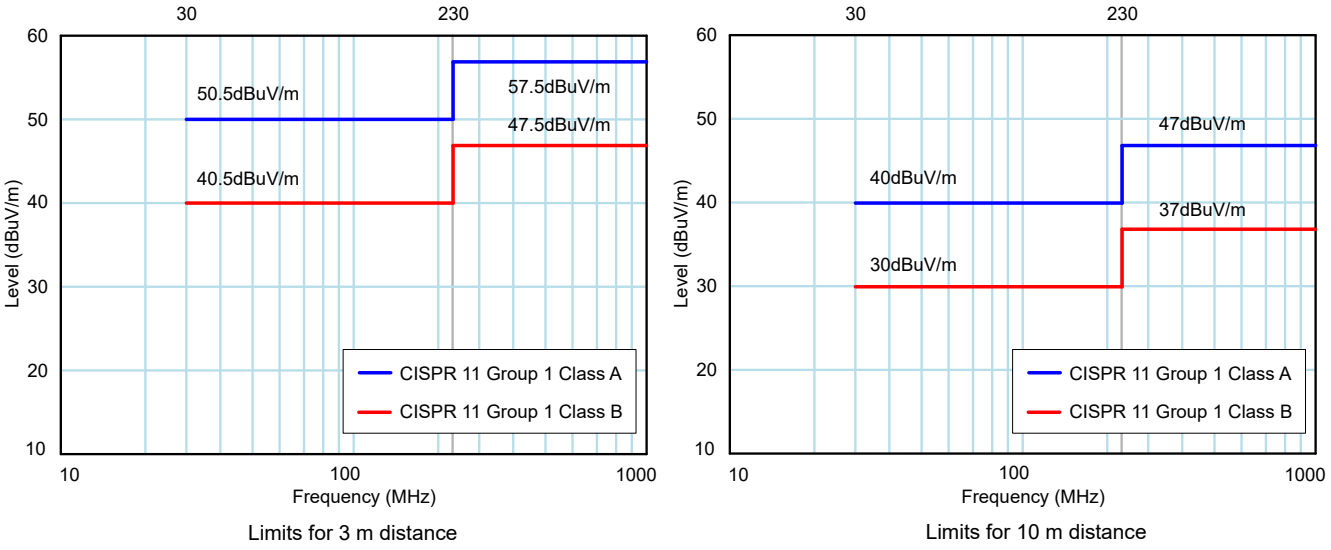

Figure 3-12. CISPR 11 Radiated Emission Limits for Class A and B Group 1 Equipment

The industrial systems designed with ADS8686S usually belong to Class A Group 1 equipment category. The measurement distance between the ADS8686S EUT and the receiving antenna is 3 m.

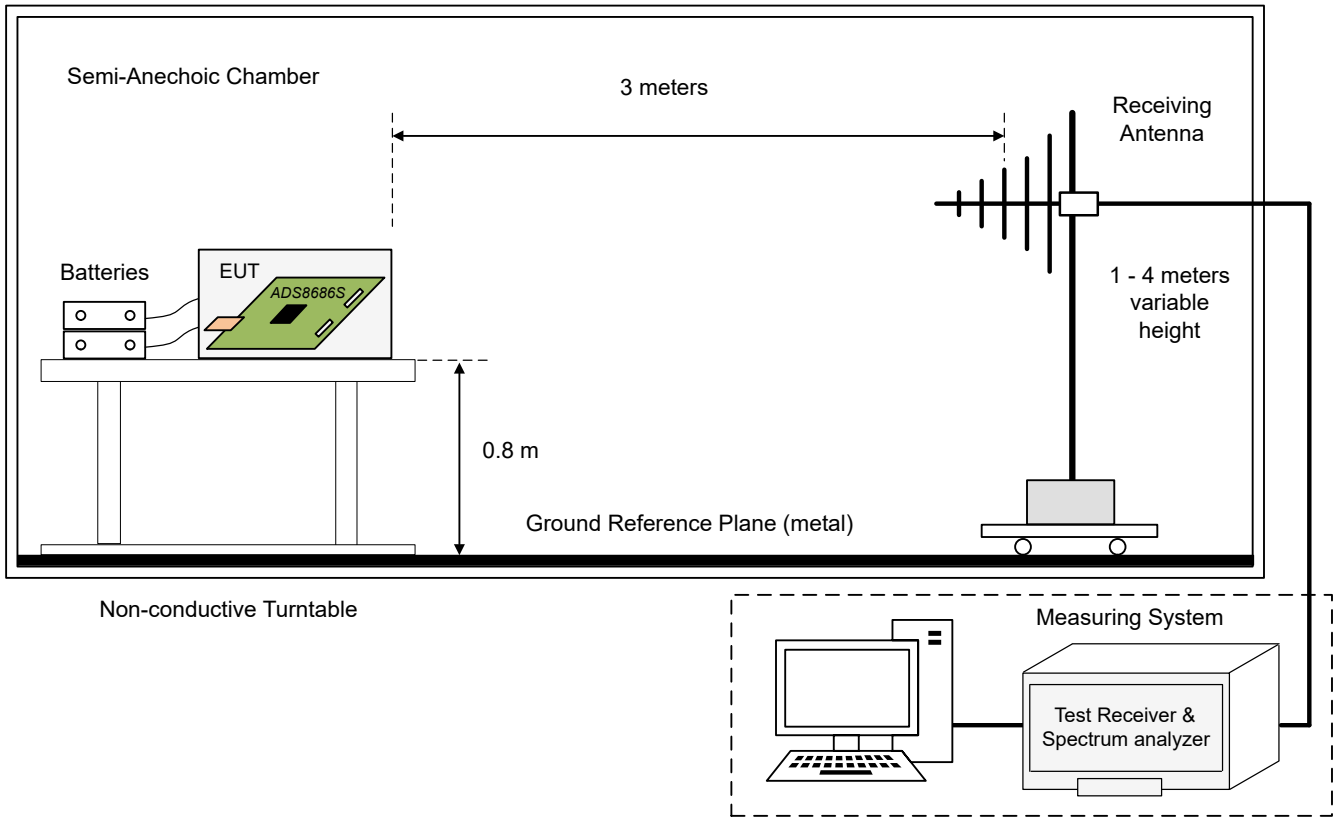

Figure 3-13. Diagram of Laboratory Setup for Radiated Emission Test

Figure 3-14 shows a photograph of the actual setup for the radiated emission test.

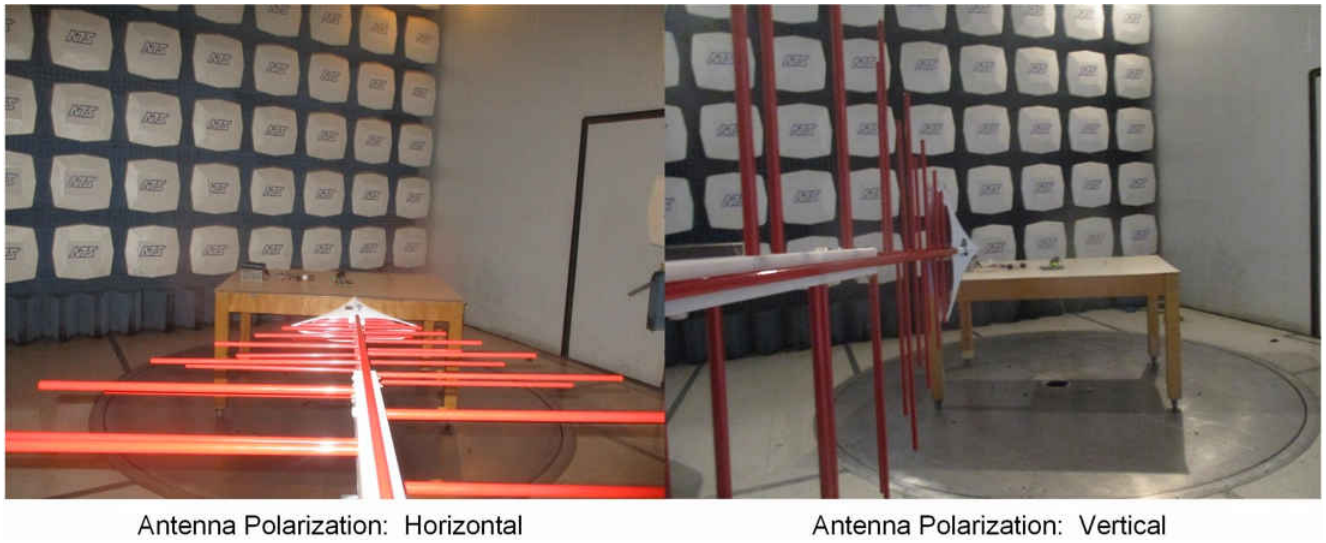

Figure 3-14. Photograph of Laboratory Setup for Radiated Emission Test

Figure 3-15, Figure 3-16, and Figure 3-17 show measured radiated emissions from the ADS8686S EMC test board with the PHI controller card at different serial clock (SCLK) frequencies and sampling rates.

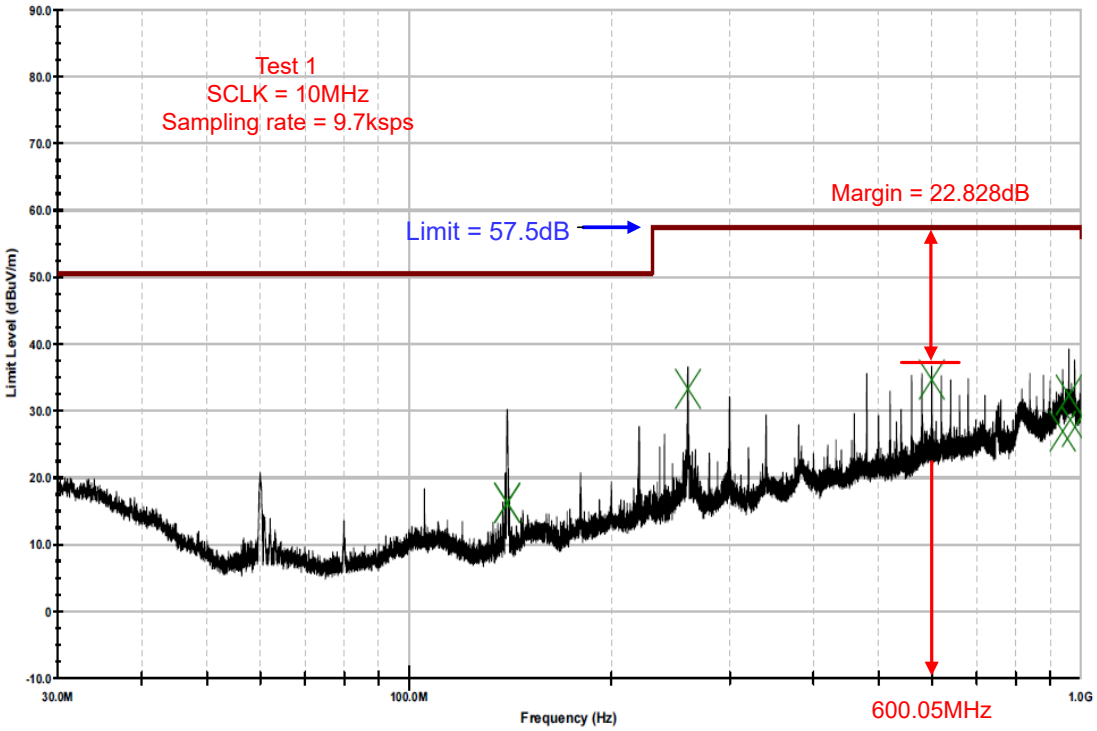

Figure 3-15. Test 1 - Measured Radiated Emission, Horizontal Antenna Polarization

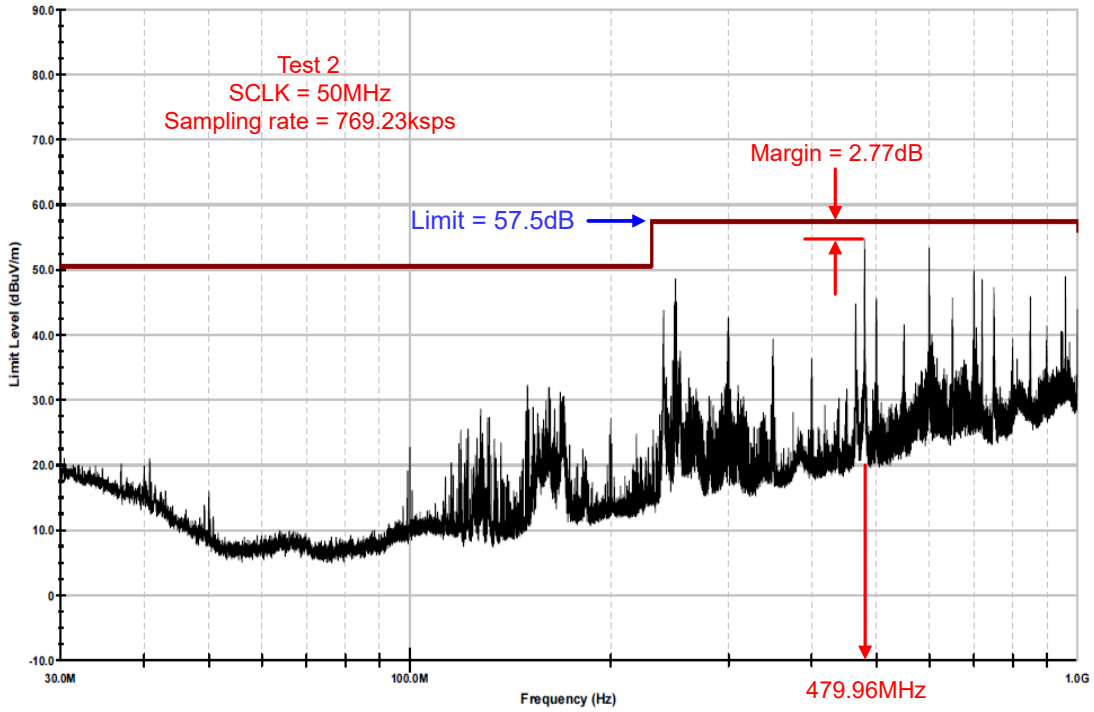

Figure 3-16. Test 2 - Measured Radiated Emission, Horizontal Antenna Polarization

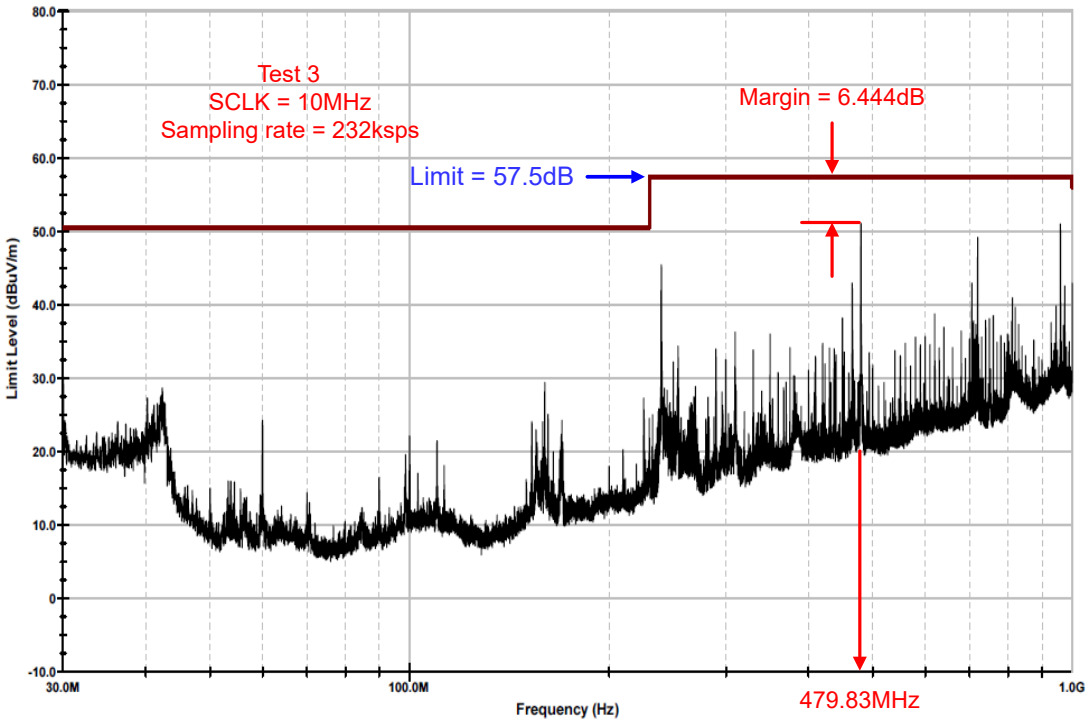

Figure 3-17. Test 3 - Measured Radiated Emission, Vertical Antenna Polarization

Table 3-7 shows the results of the radiated emission test.

Table 3-7. Radiated Emission Test Result

Test	IEC Standard	Test Condition			Quasi-Peak Limit (QP) dBµV/m	Criterion	Test Result (Pass in a Margin)
		Antenna Distance	Frequency	Antenna Polarization			
Radiated Emission (RE)	CISPR 11 for ISM	Test 1: SCLK = 10 MHz; Sampling rate = 9.7 kSPS	30–1000 MHz	Horizontal	50.5 (30–230 MHz)	A	–34.247 dB at 139.92 MHz
					57.5 (230–1000 MHz)	A	–22.828 dB at 600.05 MHz
				Vertical	50.5 (30–230 MHz)	A	–30.477 dB at 54.93 MHz
					57.5 (230–1000 MHz)	A	–28.297 dB at 679.95 MHz
		Test 2: SCLK = 50 MHz; Sampling rate = 769.23 kSPS	30–1000 MHz	Horizontal	50.5 (30–230 MHz)	A	–18.188 dB at 149.998 MHz
					57.5 (230–1000 MHz)	A	–2.77 dB at 479.96 MHz
				Vertical	50.5 (30–230 MHz)	A	–16.985 dB at 40.78 MHz
					57.5 (230–1000 MHz)	A	–5.645 dB at 479.789 MHz
		Test 3: SCLK = 10 MHz; Sampling rate = 232 kSPS	30–1000 MHz	Horizontal	50.5 (30–230 MHz)	A	–12.589 dB at 160 MHz
					57.5 (230–1000 MHz)	A	–10.823 dB at 239.94 MHz
				Vertical	50.5 (30–230 MHz)	A	–19.099 dB at 30 MHz
					57.5 (230–1000 MHz)	A	–6.444 dB at 479.83 MHz

Note: A yellow box in the table shows the less margin to pass the test.

4 Schematics

Figure 4-1 through Figure 4-6 show the schematics.

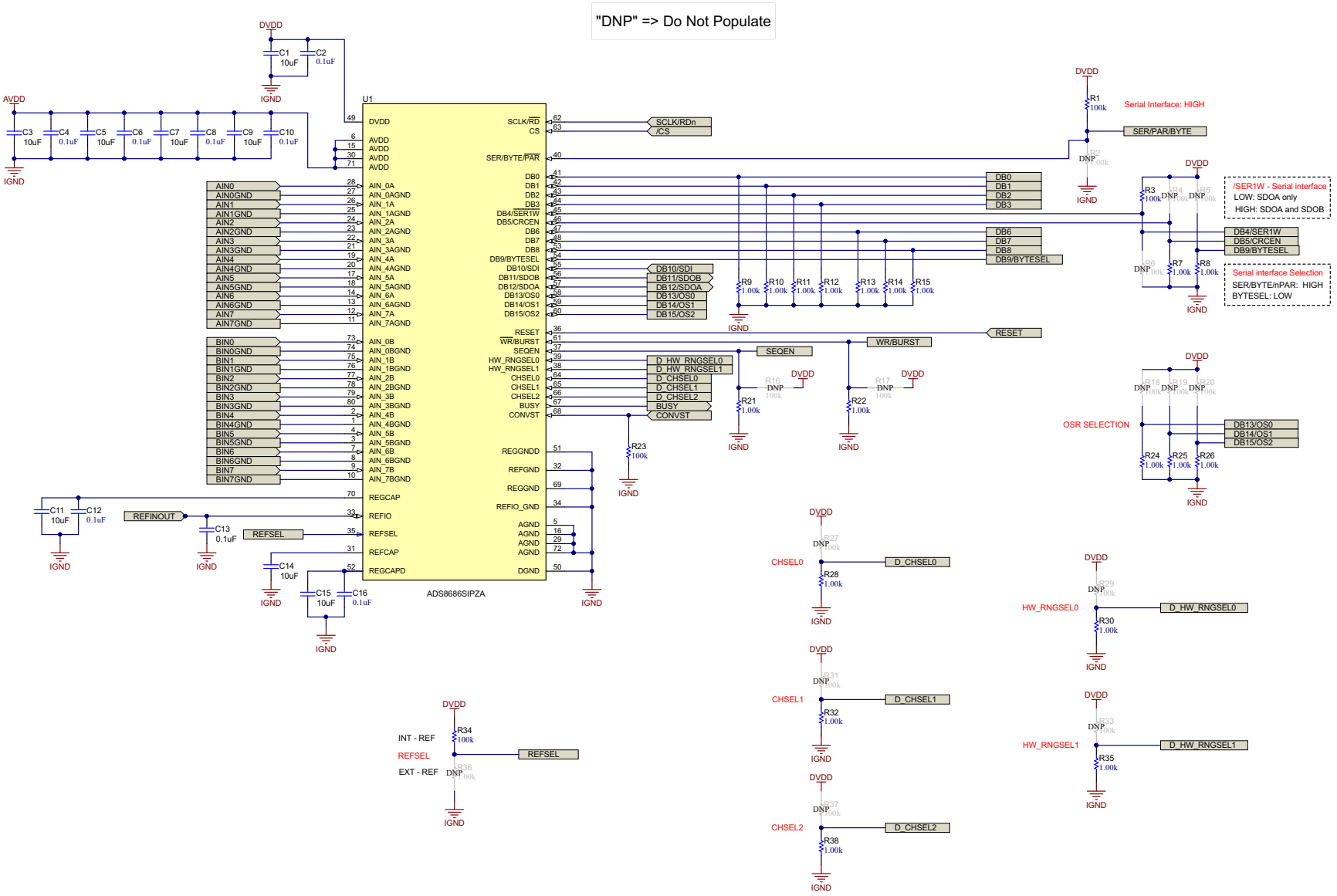

Figure 4-1. Schematic – ADC

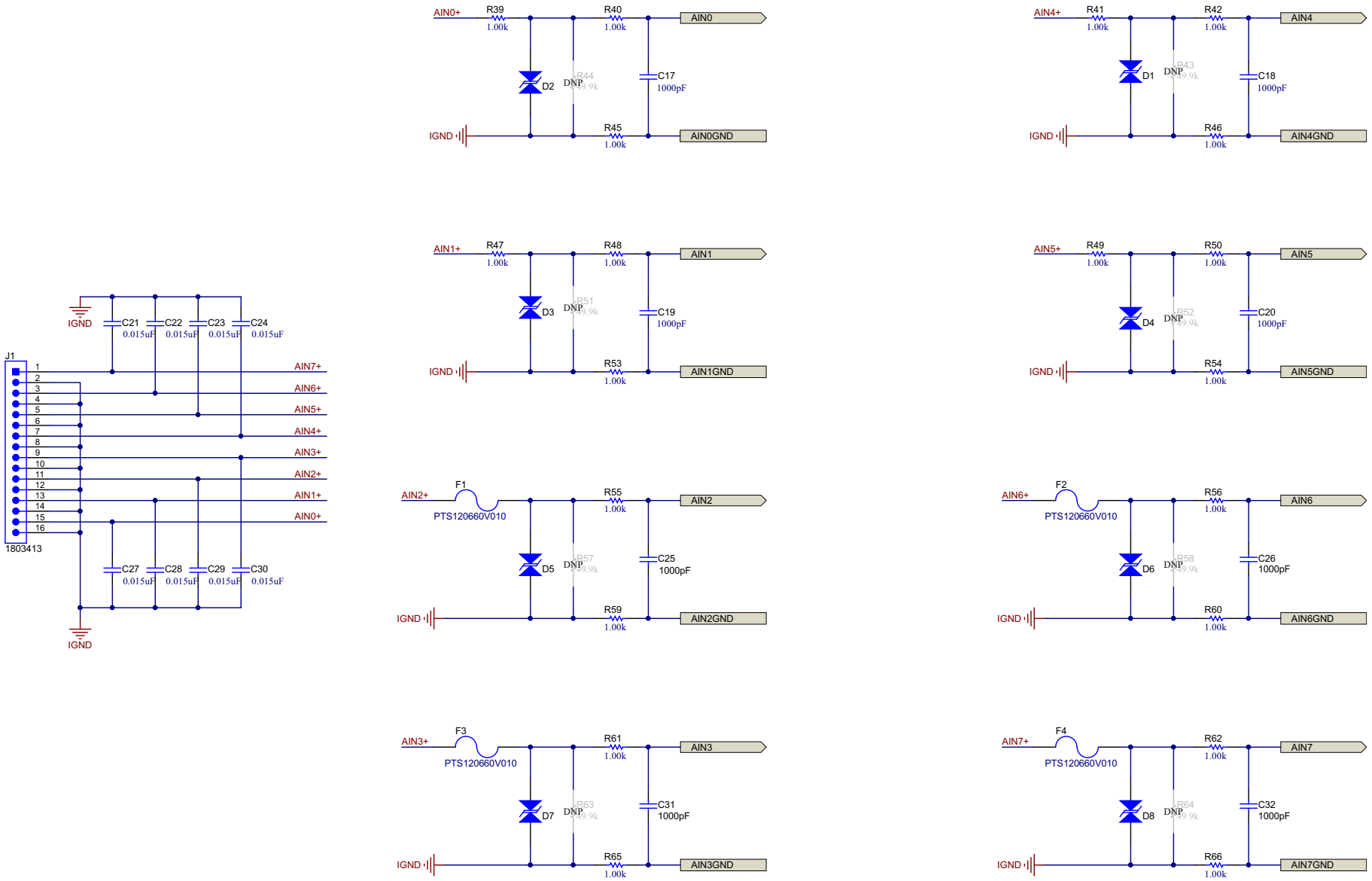

Figure 4-2. Schematic – Input of ADC - A

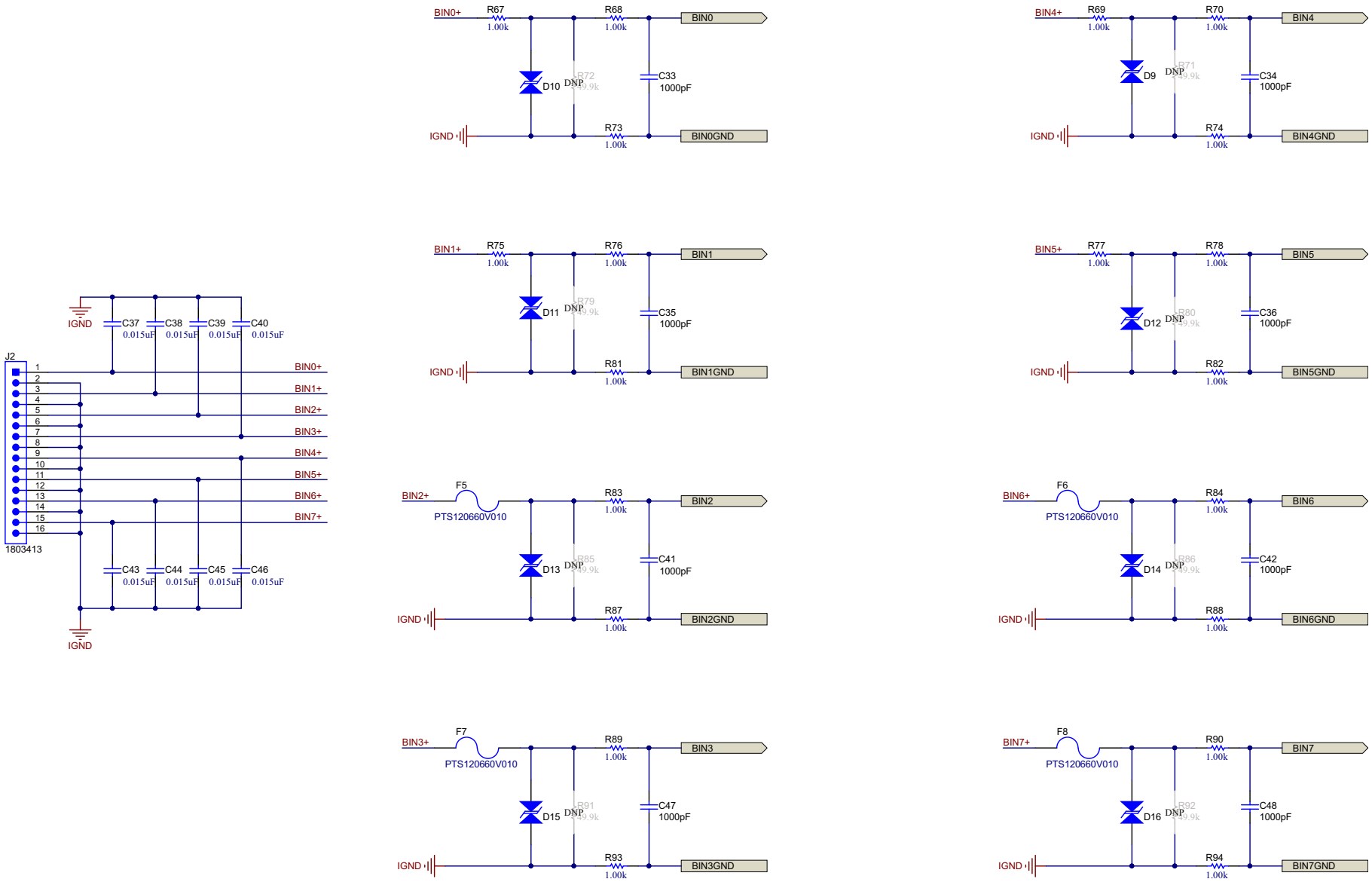

Figure 4-3. Schematic – Input of ADC - B

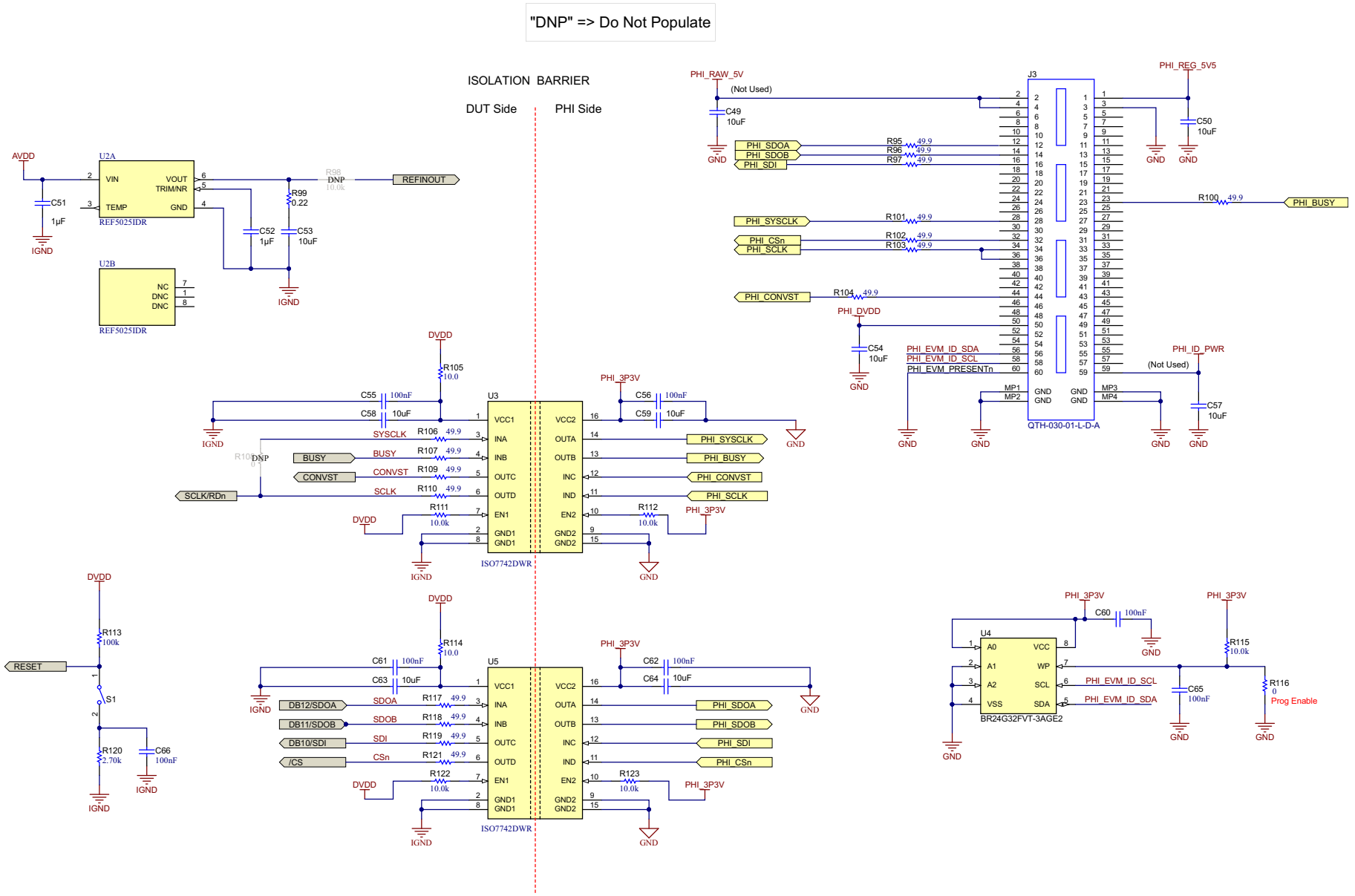

Figure 4-4. Schematic – Digital Isolation

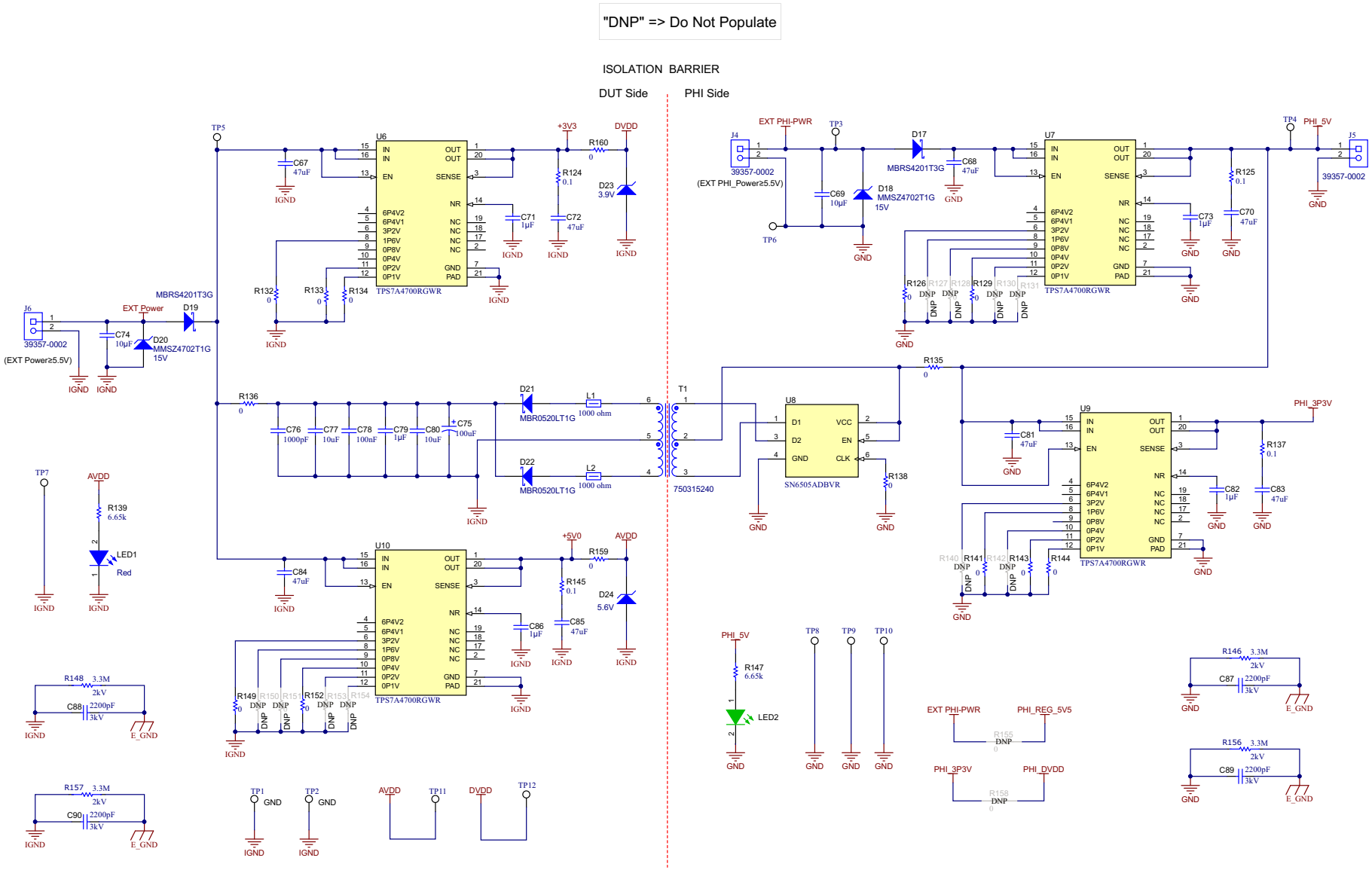

Figure 4-5. Schematic – Power Supply

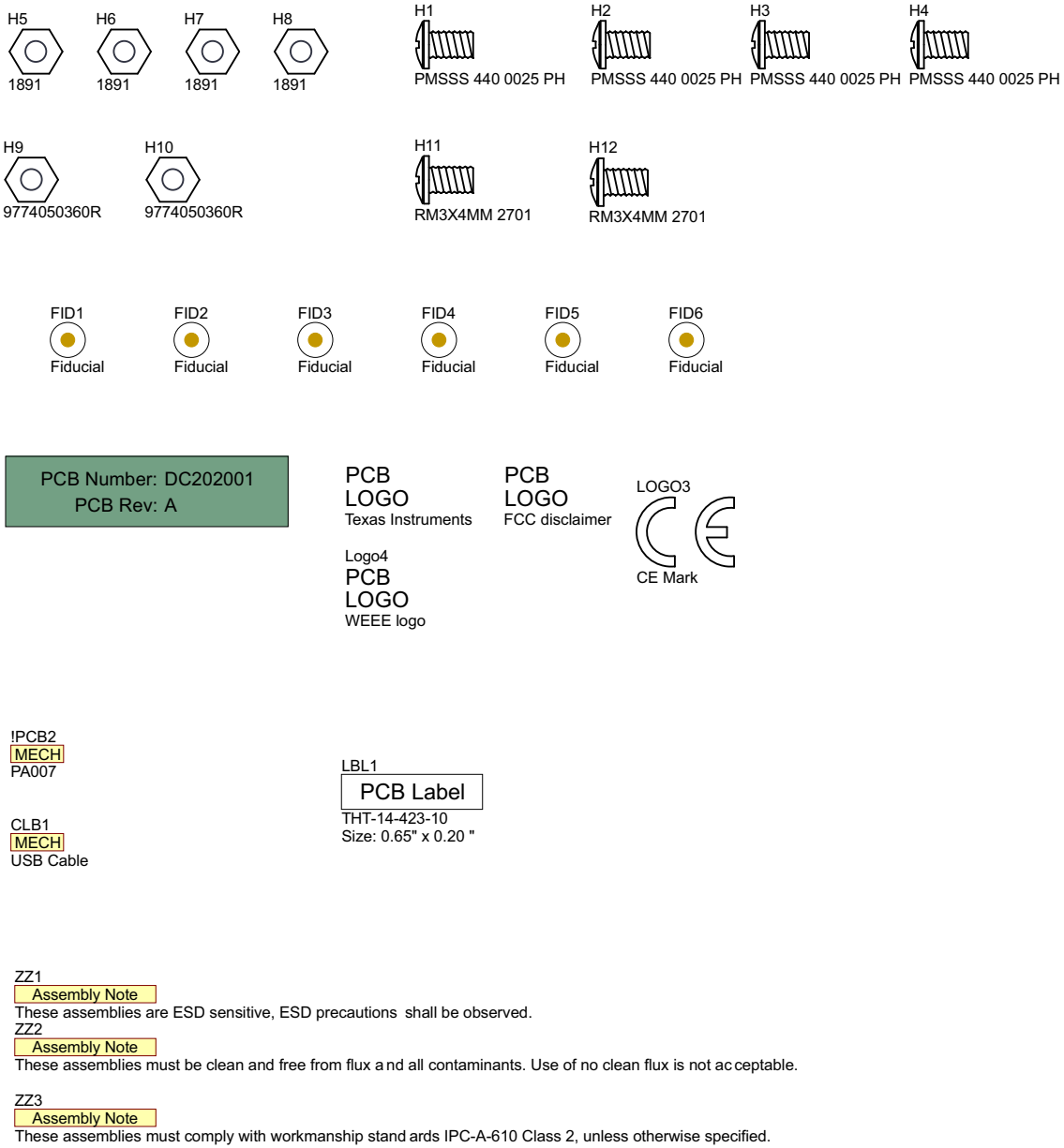

Figure 4-6. Schematic – Hardware

5 PCB Layouts

Figure 5-1 through Figure 5-6 illustrate the PCB layout images.

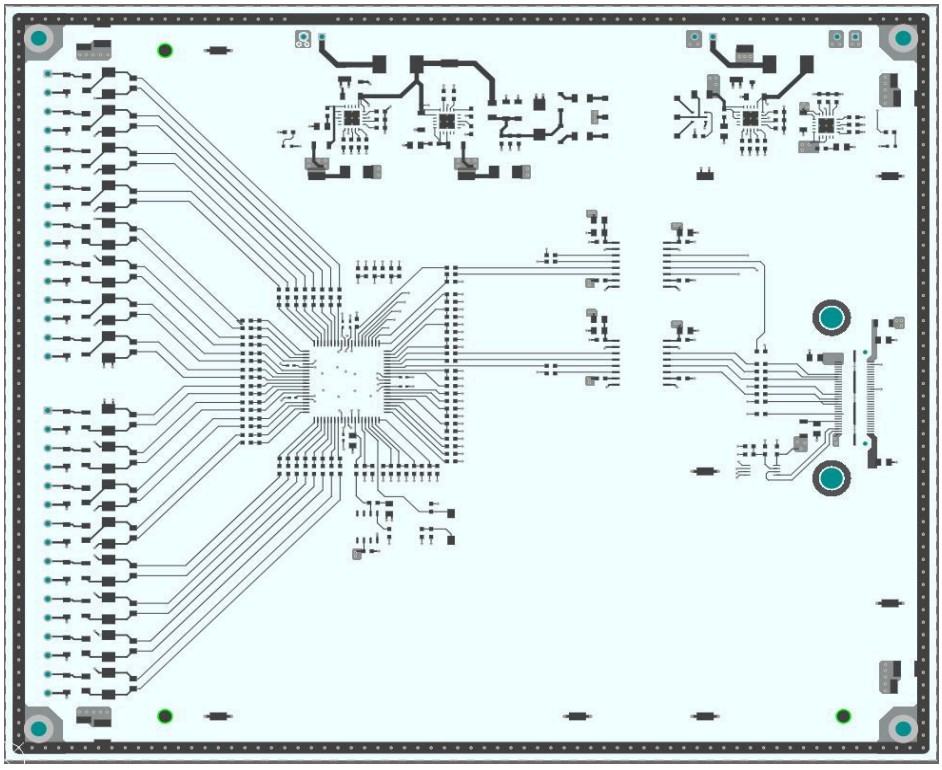

Figure 5-1. Layout – Top Layer

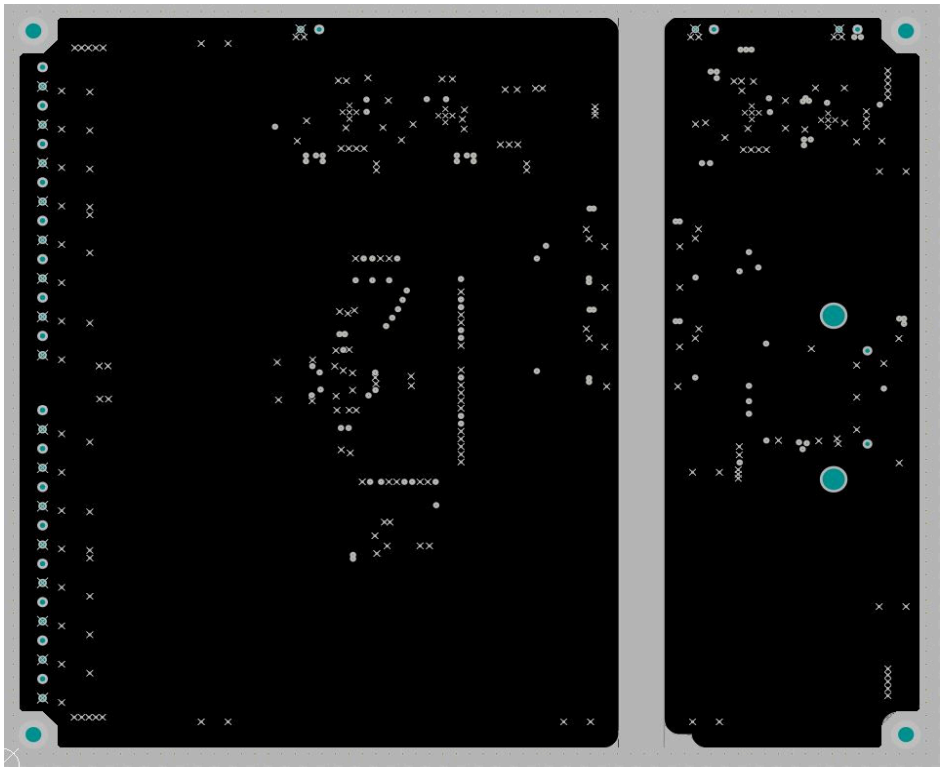

Figure 5-2. Layout – Inner Ground Layer

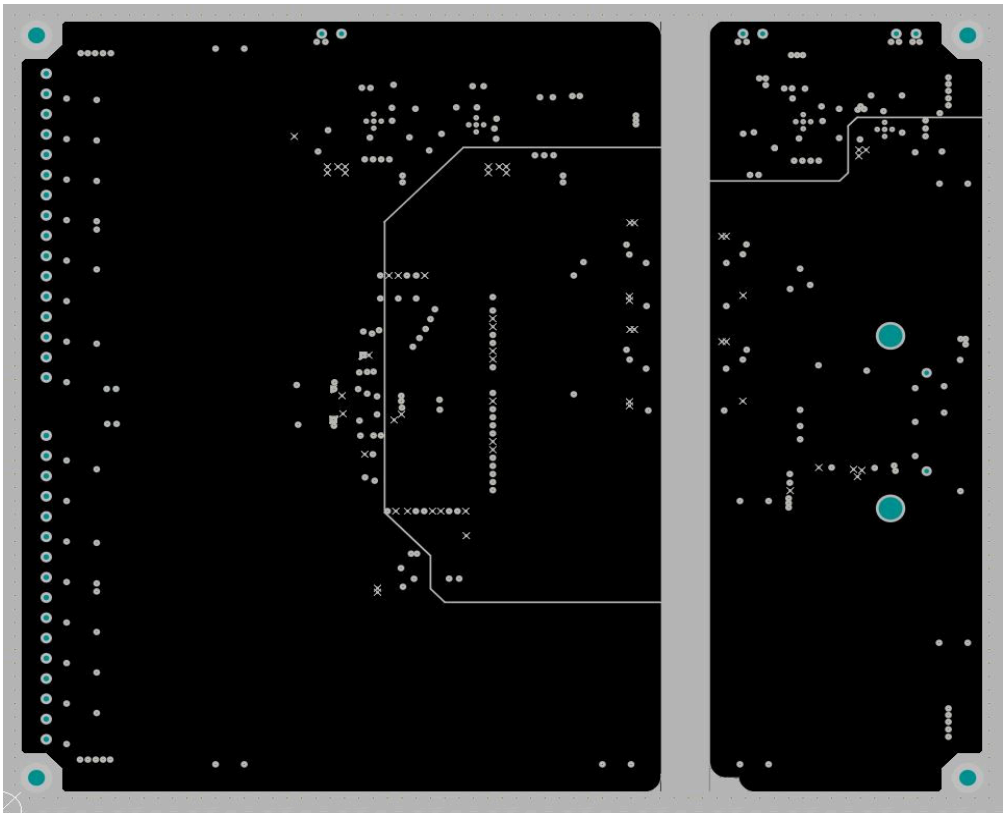

Figure 5-3. Layout – Inner Power Layer

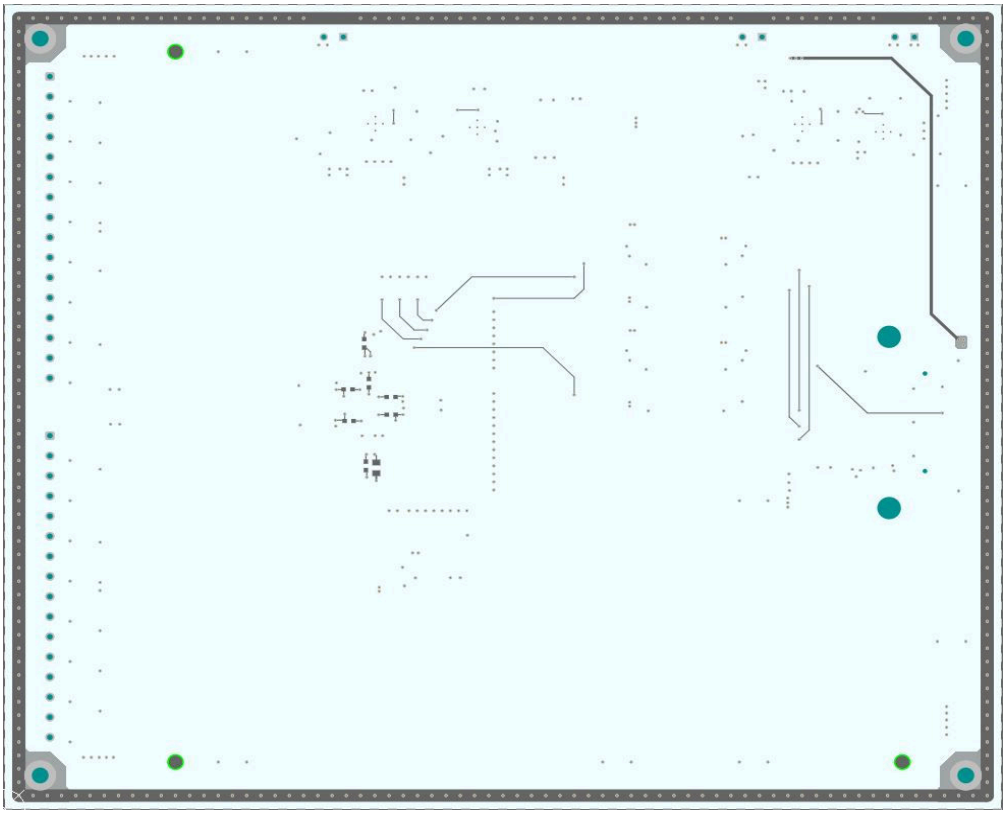

Figure 5-4. Layout – Bottom Layer

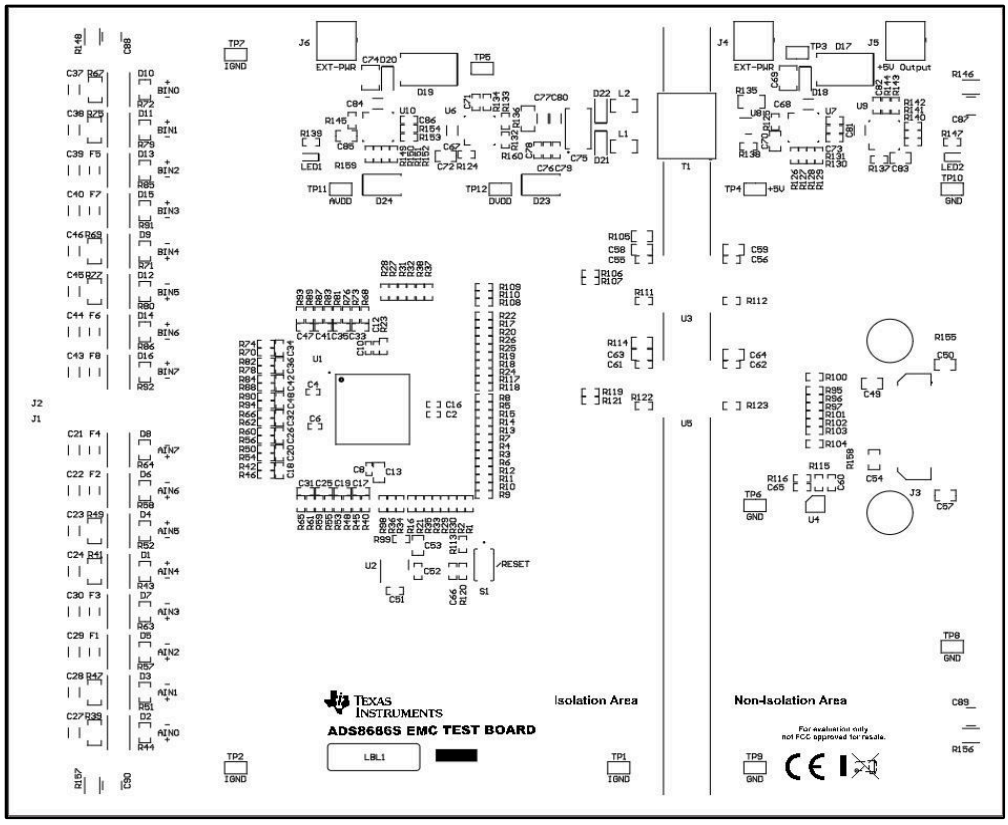

Figure 5-5. Top Silkscreen

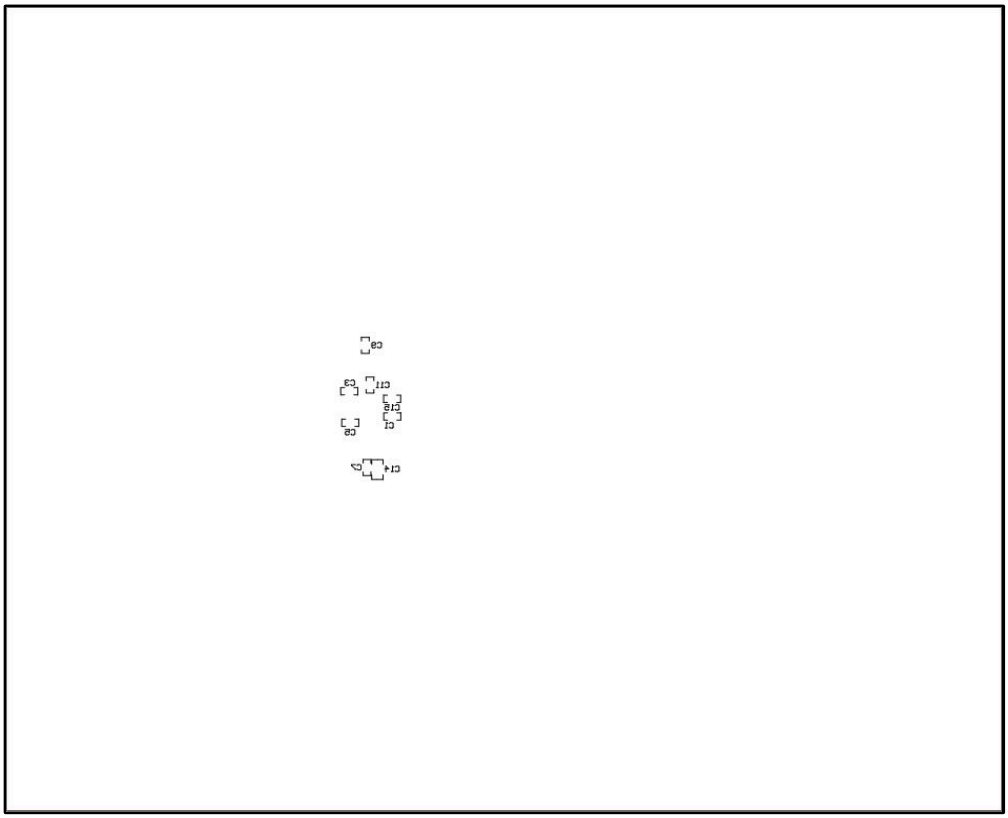

Figure 5-6. Bottom Silkscreen

6 Bill of Materials

Table 6-1 lists the BOM for this circuit design.

Table 6-1. Bill of Materials

Designator	Part Number	Manufacturer	Description
C1, C3, C5, C7, C9, C11, C15	GRM188R60J106ME84	MuRata	CAP, CERM, 10 µF, 6.3 V, ±±20%, X5R, 0603
C2, C4, C6, C8, C10, C12, C16	GRM155R71C104KA88D	MuRata	CAP, CERM, 0.1 µF, 16 V, ±10%, X7R, 0402
C13	C0805C104K4RACTU	Kemet	CAP, CERM, 0.1 µF, 16 V, ±10%, X7R, 0805
C14, C49, C50, C53, C54, C57, C58, C59, C63, C64	C0805C106K8PACTU	Kemet	CAP, CERM, 10 µF, 10 V, ±10%, X5R, 0805
C17, C18, C19, C20, C25, C26, C31, C32, C33, C34, C35, C36, C41, C42, C47, C48, C76	GRM1885C1H102FA01J	MuRata	CAP, CERM, 1000 pF, 50 V, ±1%, C0G/NP0, 0603
C21, C22, C23, C24, C27, C28, C29, C30, C37, C38, C39, C40, C43, C44, C45, C46	C3216C0G2E153J160AA	TDK	CAP, CERM, 0.015 µF, 250 V, ±5%, C0G/NP0, 1206_190
C51, C52, C71, C73, C79, C82, C86	TMK107BJ105KA-T	Taiyo Yuden	CAP, CERM, 1 µF, 25 V,±10%, X5R, 0603
C55, C56, C60, C61, C62, C65, C66, C78	C0603C104K5RACTU	Kemet	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603
C67, C68, C81, C84	C3216X5R1E476M160AC	TDK	CAP, CERM, 47 µF, 25 V, ±20%, X5R, 1206_190
C69, C74	CL32B106KBJNNWE	Samsung Electro-Mechanics	CAP, CERM, 10 µF, 50 V,±10%, X7R, 1210
C70, C72, C83, C85	C2012X5R1A476M125AC	TDK	CAP, CERM, 47 µF, 10 V, ±20%, X5R, 0805
C75	293D107X9020E2TE3	Vishay-Sprague	CAP, TA, 100 µF, 20 V, ±10%, 0.5 ohm, SMD
C77, C80	CL31A106KBHNNNE	Samsung Electro-Mechanics	CAP, CERM, 10 µF, 50 V, ±10%, X5R, 1206_190
C87, C88, C89, C90	1812HC222KAT1A	AVX	CAP, CERM, 2200 pF, 3000 V, ±10%, X7R, 1812
CLB1	6607652	CNC Teck	102-1092-BL-00100; Cable, USB, A Male - B Micro Male, 1M; 6607652 Kitting Item
D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16	SMBJ10CA	Littelfuse	Diode, TVS, Bi, 10 V, SMB
D17, D19	MBRS4201T3G	ON Semiconductor	Diode, Schottky, 200 V, 4 A, SMC
D18, D20	MMSZ4702T1G	ON Semiconductor	Diode, Zener, 15 V, 500 mW, SOD-123
D21, D22	MBR0520LT1G	ON Semiconductor	Diode, Schottky, 20 V, 0.5 A, SOD-123
D23	1SMB5915BT3G	ON Semiconductor	Diode, Zener, 3.9 V, 550 mW, SMB
D24	1SMB5919BT3G	ON Semiconductor	Diode, Zener, 5.6 V, 550 mW, SMB
F1, F2, F3, F4, F5, F6, F7, F8	PTS120660V010	Eaton	Fuse, 0.1 A, 60 VDC, SMD
FID1, FID2, FID3, FID4, FID5, FID6	N/A	N/A	Fiducial mark. There is nothing to buy or mount.
H1, H2, H3, H4	PMSSS 440 0025 PH	B&F Fastener Supply	MACHINE SCREW PAN PHILLIPS 4-40
H5, H6, H7, H8	1891	Keystone	Hex Standoff, #4-40, Aluminum, 1/4"
H9, H10	9774050360R	Wurth Elektronik	ROUND STANDOFF M3 STEEL 5MM
H11, H12	RM3X4MM 2701	APM HEXSEAL	Machine Screw Pan PHILLIPS M3
J1, J2	1803413	Phoenix Contact	Terminal Block, 3.81 mm, 16 × 1, R/A, TH
J3	QTH-030-01-L-D-A	Samtec	Header(Shrouded), 19.7 mil, 30 × 2, Gold, SMT

Table 6-1. Bill of Materials (continued)

Designator	Part Number	Manufacturer	Description
J4, J5, J6	39357-0002	Molex	Terminal Block, 3.5 mm, 2 × 1, Tin, TH
L1, L2	HZ1206D102R-10	Laird-Signal Integrity Products	Ferrite Bead, 1000 Ω @ 100 MHz, 0.4 A, 1206
LBL1	THT-14-423-10	Brady	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll
LED1	150060RS75000	Wurth Elektronik	LED, Red, SMD
LED2	LTST-C193TGKT-5A	Lite-On	LED, Green, SMD
R1, R3, R23, R34, R113	RC0603FR-07100KL	Yageo	RES, 100 k, 1%, 0.1 W, 0603
R7, R8, R9, R10, R11, R12, R13, R14, R15, R21, R22, R24, R25, R26, R28, R30, R32, R35, R38	RC0603FR-071KL	Yageo	RES, 1.00 k, 1%, 0.1 W, 0603
R39, R41, R47, R49, R67, R69, R75, R77	CRCW12061K00FKEA	Vishay-Dale	RES, 1.00 k, 1%, 0.25 W, 1206
R40, R42, R45, R46, R48, R50, R53, R54, R55, R56, R59, R60, R61, R62, R65, R66, R68, R70, R73, R74, R76, R78, R81, R82, R83, R84, R87, R88, R89, R90, R93, R94	RT0603BRD071KL	Yageo America	RES, 1.00 k, 0.1%, 0.1 W, 0603
R95, R96, R97, R100, R101, R102, R103, R104, R106, R107, R109, R110, R117, R118, R119, R121	RC0603FR-0749R9L	Yageo	RES, 49.9, 1%, 0.1 W, 0603
R99	ERJ-3RQFR22V	Panasonic	RES, 0.22, 1%, 0.1 W, 0603
R105, R114	ERJ-P06F10R0V	Panasonic	RES, 10.0, 1%, 0.5 W, AEC-Q200 Grade 0, 0805
R111, R112, R115, R122, R123	RC0603FR-0710KL	Yageo	RES, 10.0 k, 1%, 0.1 W, 0603
R116, R126, R129, R132, R133, R134, R138, R141, R143, R144, R149, R152	CRCW06030000Z0EA	Vishay-Dale	RES, 0, 5%, 0.1 W, 0603
R120	RC0603FR-072K7L	Yageo	RES, 2.70 k, 1%, 0.1 W, 0603
R124, R125, R137, R145	ERJ-3RSFR10V	Panasonic	RES, 0.1, 1%, 0.1 W, 0603
R135, R136	CRCW12060000Z0EAHP	Vishay-Dale	RES, 0, 0.75 W, AEC-Q200 Grade 0, 1206
R139, R147	RC0603FR-076K65L	Yageo	RES, 6.65 k, 1%, 0.1 W, 0603
R146, R148, R156, R157	CHV2010-FX-3304ELF	Bourns	RES SMD 3.3M OHM 1% 1/2W 2010
R159, R160	5108	Keystone	RES, 0, 1%, 0.5 W, 1206
S1	EVQPNF04M	Panasonic	Switch, Tactile, SPST-NO, 0.05A, 12 V, SMD
T1	750315240	Wurth Elektronik	Transformer, 110 uH, SMT
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12	5015	Keystone	Test Point, Miniature, SMT
U1	ADS8686SIPZA	Texas Instruments	16-Channel, 16-Bit, 1-MSPS, Dual, Simultaneous Sampling ADC With Integrated Analog Front End, PZA0080A (LQFP-80)
U2	REF5025IDR	Texas Instruments	Low Noise, Very Low Drift, Precision Voltage Reference, -40 to 125 degC, 8-pin SOIC(D), Green (RoHS & no Sb/Br)
U3, U5	ISO7742DWR	Texas Instruments	High-Speed, Low-Power, Robust EMC Quad-Channel Digital Isolator, DW0016B (SOIC-16)
U4	BR24G32FVT-3AGE2	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8

Table 6-1. Bill of Materials (continued)

Designator	Part Number	Manufacturer	Description
U6, U7, U9, U10	TPS7A4700RGWR	Texas Instruments	36 V, 1 A, 4.17-μV_{RMS}, RF LDO Voltage Regulator, RGW0020A (VQFN-20)
U8	SN6505ADBVR	Texas Instruments	Low-Noise 1-A Transformer Driver for Isolated Power Supplies, Internal Clock-160 kHz, DBV0006A (SOT-23-6)
R2, R6, R36	RC0603FR-071KL	Yageo	RES, 1.00 k, 1%, 0.1 W, 0603
R4, R5, R16, R17, R18, R19, R20, R27, R29, R31, R33, R37	RC0603FR-07100KL	Yageo	RES, 100 k, 1%, 0.1 W, 0603
R43, R44, R51, R52, R57, R58, R63, R64, R71, R72, R79, R80, R85, R86, R91, R92	CRCW080549K9FKEA	Vishay-Dale	RES, 49.9 k, 1%, 0.125 W, 0805
R98	RC0603FR-0710KL	Yageo	RES, 10.0 k, 1%, 0.1 W, 0603
R108, R127, R128, R130, R131, R140, R142, R150, R151, R153, R154	CRCW06030000Z0EA	Vishay-Dale	RES, 0, 5%, 0.1 W, 0603
R155, R158	5108	Keystone	RES, 0, 1%, 0.5 W, 1206

7 Acknowledgments

The author thanks Collin Wells, Applications Manager in precision ADCs at Texas Instruments, for his contributions to this design and his help with the test.

8 References

1. Texas Instruments, *ADS8686S 16-Channel, 16-Bit, 1-MSPS, Dual, Simultaneous-Sampling ADC With Integrated Analog Front-End* data sheet
2. Texas Instruments, *ADS8686SEVM-PDK* ADS8686S 16-channel 16-bit 1-MSPS dual simultaneous-sampling ADC performance demonstration kit (PDK)

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2022) to Revision A (May 2022) **Page**

- Changed *Document Title* and updated the *Abstract*....1
- Updated *Diagram of Laboratory Setup for EFT Test* image....9
- Updated *Radiated Emission Test Result* values....22

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265